2009/10 Advances in the mixed signal IC design group

Mattias Andersson, Dejan Radjen, Martin Liliebladh, Ping Lu, Daniele Mastantuono, Martin Anderson, Lars Sundström, Pietro Andreani

Mixed-Signal IC Design
Department for Electrical and Information Technology
Lund University

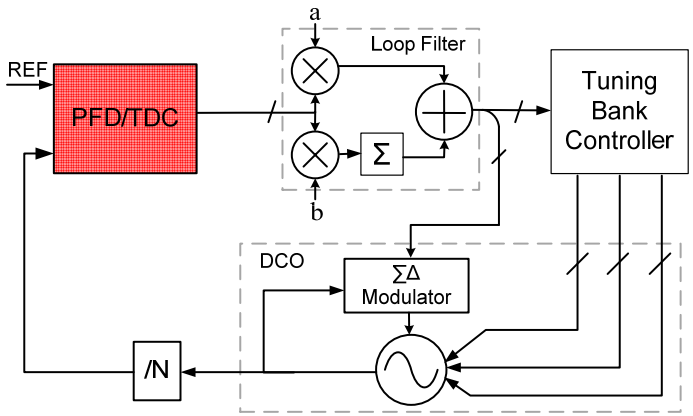
Mixed Signal IC Design Researchers

- Pietro Andreani, Associate Professor
- Ping Lu, Post-Doc (VR, april 2009)
- Daniele Mastantuono, Post-Doc (SoS, 2010)
- Dejan Radjen, Ph.D. Student (VR, feb. 2009)
- Mattias Andersson, Ph.D. Student (SoS and Dragon, feb. 2009)
- Martin Liliebladh, Ph.D. Student (Dragon, feb. 2010; co-supervised with Henrik Sjöland)

- Lars Sundström, Martin Anderson, Sven Mattisson (Ericsson Research)

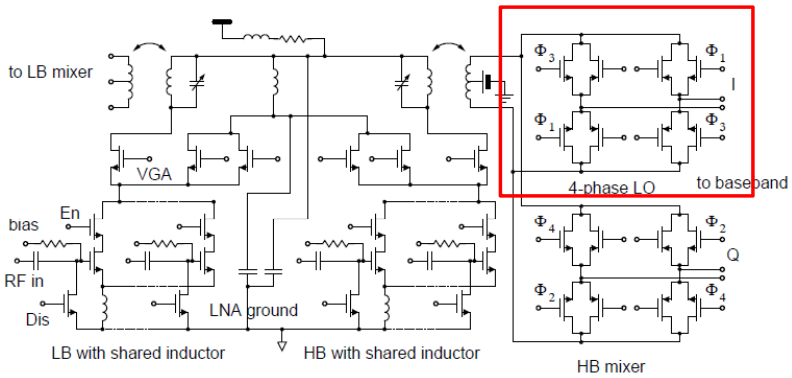
CAD support: Stefan Molund
Linux support: Erik Jonsson

Work in Progress – Ping Lu



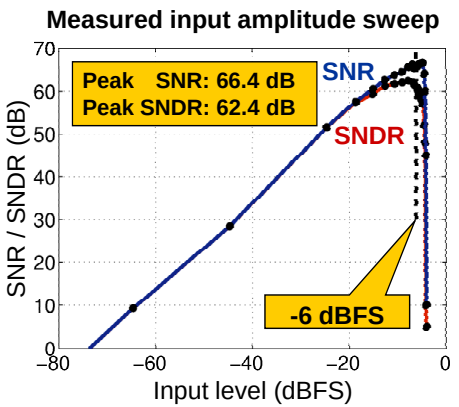
New Time-to-Digital Converter

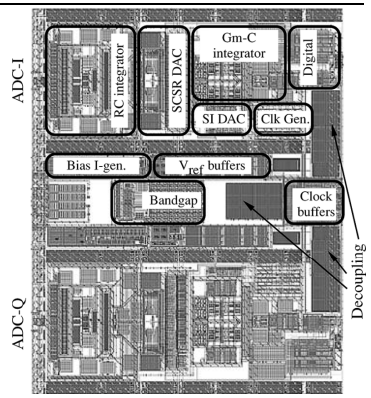
Work in Progress – Martin Liliebladh and Daniele Mastantuono



- Improve the IIP2 of a CMOS receiver – focus on passive mixer

Prior in-house art – ΔΣ modulator



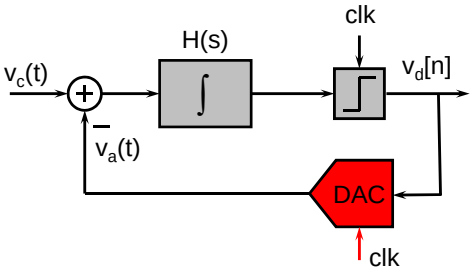


-1.2 / 1.8V, 5mW
- 90nm RF CMOS
- I & Q ΔΣ Modulators, BW=1.92MHz
- 0.48 x 0.62 = 0.3 mm²

M. Anderson and L. Sundström, " Design and Measurement of a CT ΔΣ ADC with Switched-Capacitor Switched-Resistor Feedback", JSSC Feb. 2009

Work in Progress – Mattias Andersson

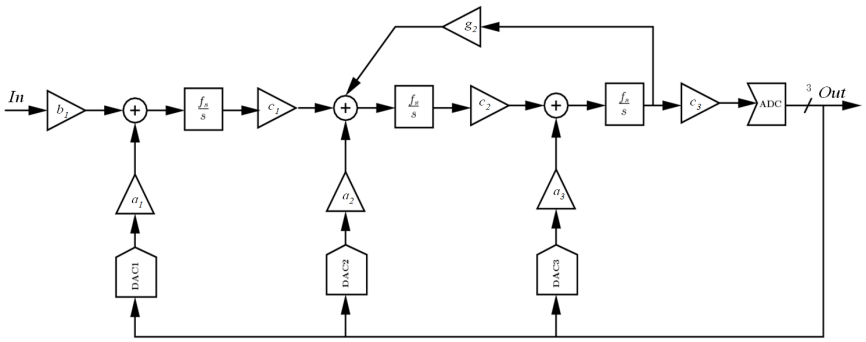
- CT ΔΣ ADC for LTE
  - 3rd order, f_s=288MHz, BW=9MHz



- Overload protection
- New clocking scheme (NRZ/RZ)
- Multi-bit DACs and DEM

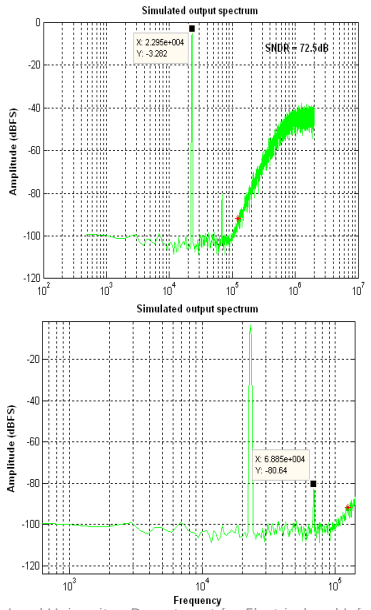
- Tapeout November 2010

Work in Progress – Dejan Radjen



- Ultra low power 3rd order, 3 bits CT ΔΣ converter with modified feedback pulses
- Tape-out November 2010

Work in Progress – Dejan Radjen



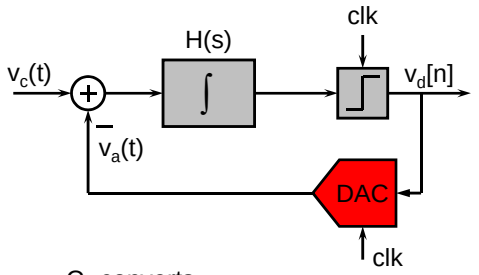
Performance summary	
Parameter	**Value**
Process	ST 65nm CMOS
Supply Voltage	900mV
Input Range	200mV Fully Differential
Bandwidth	125kHz
Sampling Frequency	4MHz
SNR	74dB
SNDR	72.5dB
Power Consumption	350μW

Impact of MOS Threshold-Voltage Mismatch in Current-Steering DACs for CT Delta-Sigma Modulators

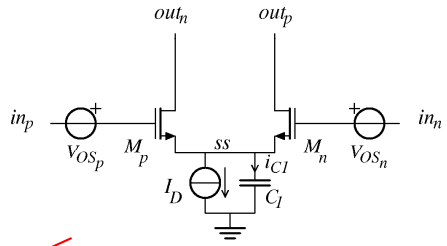
Mattias Anderson, Martin Anderson, Lars Sundström, Pietro Andreani

Proc. ISCAS, pp. 4021-4, May 2010

Delta-Sigma ADC with current-steering DAC

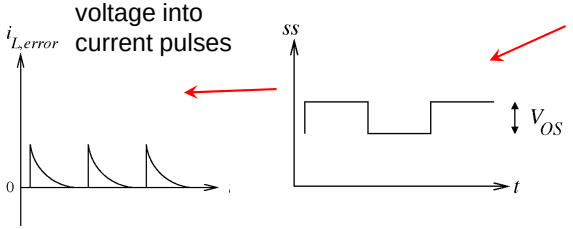


Mismatch between transistors causes nonlinearity!

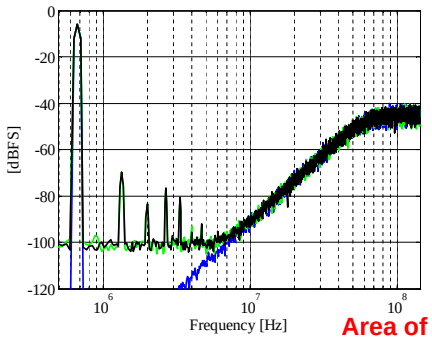


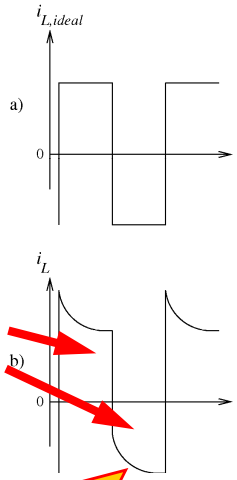
DAC unit-current cell

C_1 converts voltage into current pulses



V_{th} mismatch causes an asymmetric pulse





Area of '+1' pulse is not the same as area of '-1' pulse!

Simulations on implemented DAC and VerilogA model match within 1dB

Fast and accurate simulations

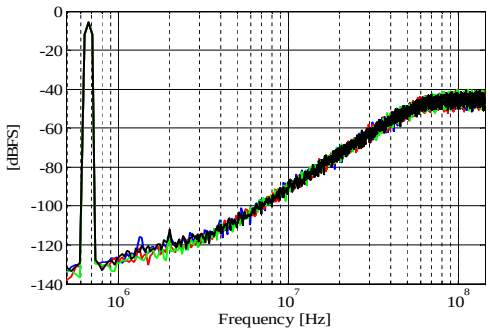
Asymmetric pulse degrades SNDR by 10dB

Injected charge error $Q=V_{OS}(C_1+C_{gs})$

Solution

Minimize the product $(C_1+C_{gs})V_{OS}$

The nonlinearity effects are removed by changing to a RZ DAC and employing DWA



RZ DAC with DWA recovers the performance

A transmitter CMOS VCO for WCDMA/EDGE

Pietro Andreani, Kirill Kozmin, Per Sandrup, Thomas Mattsson

Proc. ESSCIRC, pp. 146-149, Sept. 2010

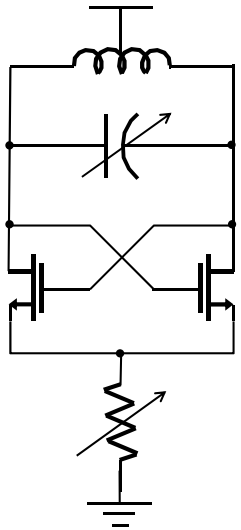
TX EDGE/WCDMA bands

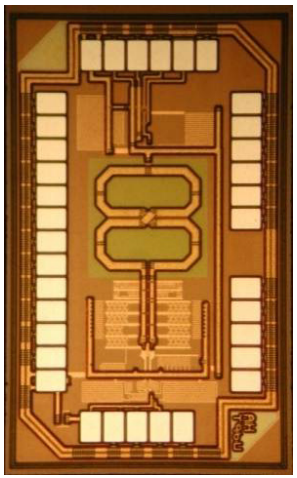
- Band I → 1920 – 1980 MHz
- Band XII → 698 – 716 MHz
- Band VII → 2500 – 2570 MHz

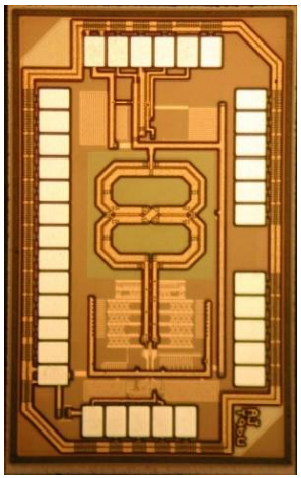
- All bands except VII →
  2.8 GHz < VCO < 4.0 GHz
  + frequency divider by 2 or 4

- PN < -163 dBc/Hz @ 20 MHz offset (GSM)
- PN < -166 dBc/Hz @ 45 MHz offset
  (SAW-less WCDMA)

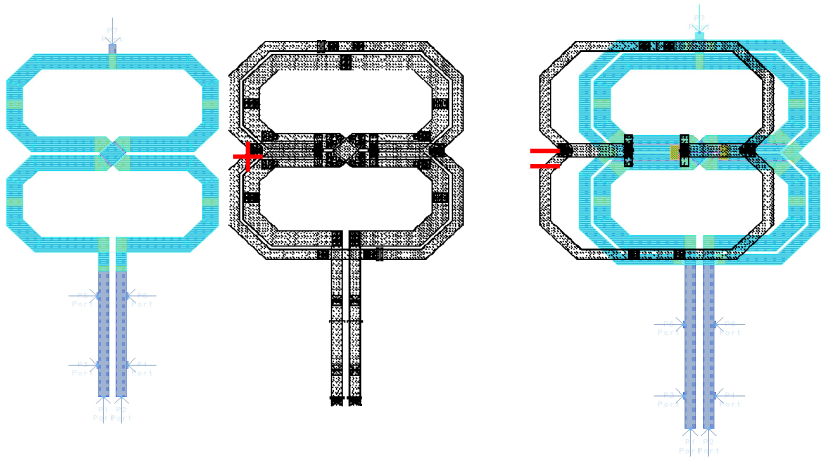
Design and die photos



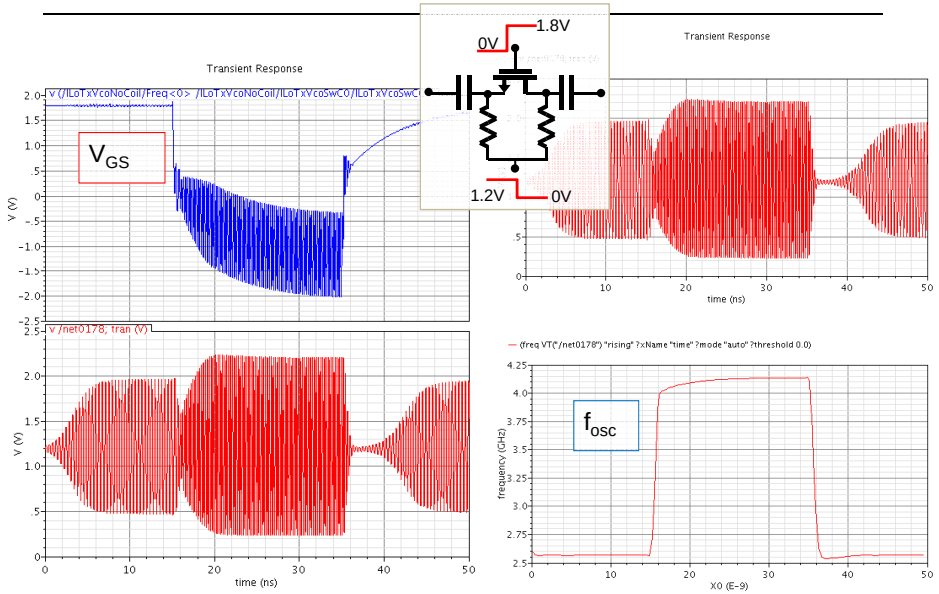




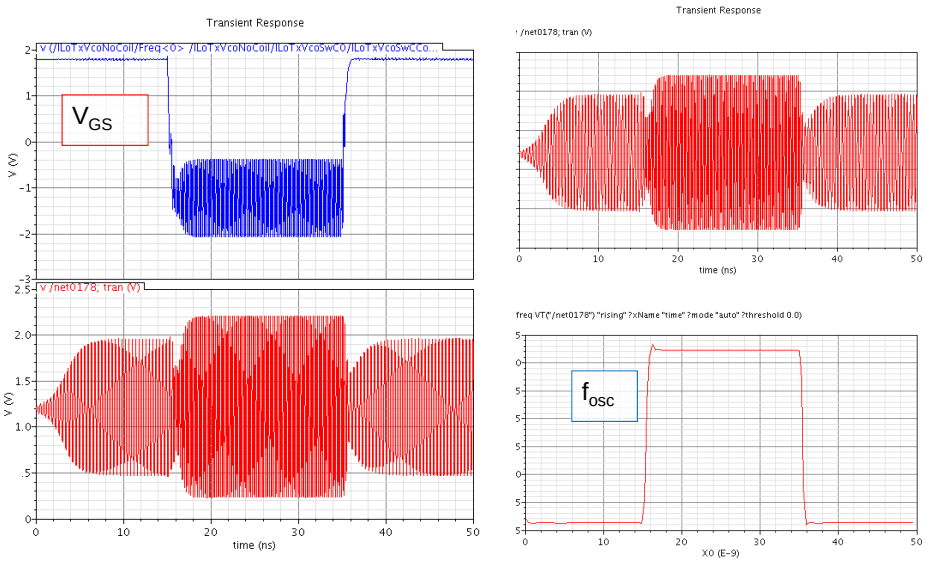
Variable inductor



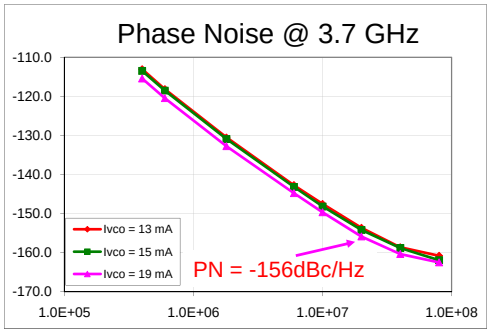
Slow oscillation settling



Much improved settling



Performance



- -156dBc/Hz becomes -168dBc/Hz at the GSM band (i.e. after division by 4)
- PN < -166dBc/Hz @ 45 MHz → SAW-less WCDMA transmitter ok
- Variable-inductor VCO: 4.90-5.75GHz, >10dB phase-noise penalty