Sensing Temperature with Heat

Kofi Makinwa

Electronic Instrumentation Laboratory/DIMES Delft University of Technology Delft, The Netherlands





Temperature Sensors are Everywhere!



On-Chip Temperature Sensors

- Most properties of silicon are temperature dependent!
 ⇒ resistors, diodes and transistors are all "sensors"
- But **good** temperature sensors require **two** signals:
 - a temperature dependent signal
 - a reference signal



The Band-Gap (BG) Principle



• substrate PNPs generate:

 ΔV_{BE} proportional to absolute temp. (PTAT)

- V_{BE} complementary to absolute temp. (CTAT)
- Combining these:

$$\mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}} = \frac{V_{PTAT}}{V_{REF}}$$

Dominant Error Sources



- process spread of $V_{BE} \Rightarrow$ errors of ~3°C
- offset in ΔV_{BE} read-out: $10\mu V \Rightarrow 0.1^{\circ}C$ error
- errors in $\ln(p)$ term and gain α : 0.1% \Rightarrow 0.2°C error

Single-Temperature Calibration

- process spread \Rightarrow PTAT error in V_{BE}
- So single-temperature trim is sufficient
 e.g. by trimming *I_C*
- But all other (circuit) errors must be made negligible ...



BG Temp Sensor: Block Diagram



- Bipolar core = two PNP transistors
- Bias circuit generates a programmable current I_{bias} \Rightarrow Room temperature V_{BE} trim
- ΣΔ modulator outputs a bitstream bs that is filtered and scaled by decimation filter
- Chopping, CDS and DEM minimize offset and errors in the current ratios and gain factor α

Measurement Results



The Calibration Problem

• Process spread $\Rightarrow V_{BE}$ must be trimmed



- Thermal time constant of package = several seconds
 ⇒ calibration and trimming takes several minutes
- BUT time = money!

So most commercial sensors are calibrated in <1s at one temperature \Rightarrow inaccuracies of ~ 0.5°C

Better Temperature Sensors?

- Should exploit the strengths of nanometer CMOS
 - Fast switches (tens of picoseconds)
 - Accurate lithography (nanometers)
 - Pure silicon substrate (10⁻⁸)
- But the **electrical** properties of silicon are strongly affected by doping variations
- Why not measure one of the **other** physical properties of the substrate?

Thermal Diffusivity of Silicon



Thermal Diffusivity Sensing



- Thermal diffusivity, *D*, is a function of T_{abs} \Rightarrow temperature-dependent *delay*
- Lithography \Rightarrow accurate spacing **s**
- Pure silicon substrate \Rightarrow *D* is well-defined

CMOS Implementation

- Heater
 = n⁺ resistor
- Temp. sensor
 = p⁺/Al thermopile
- Silicon is a good heat conductor
 ⇒ sub-mV output!
- Self-heating < 1°C $\Rightarrow P_{heat} < 10$ mW



Sensor Characteristics



• This is actually an **electrothermal** filter (ETF) with a *temperature-dependent* phase shift

$$\phi_{ETF} \propto s \sqrt{f/D}$$

• At room temp, s =20 μ m, f = 100kHz $\Rightarrow \phi_{ETF} \sim 90^{\circ}$

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CMOS Compatibility



 ETFs sense *local, AC* temperature signals and are well insulated from the chip's packaging

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ETF Phase Response

- $f_{drive} = \text{const}$ $\Rightarrow \phi_{ETF}(T)$ is **nearly linear**
- In the military range: $60^{\circ} < \phi_{ETF} < 100^{\circ}$
- Sensitivity: 0.2%
- So we need a precision phase detector ...



Phase-Domain $\Sigma \Delta$ **Modulator**



- Low ETF output (~ $1mV_{pp}$) \Rightarrow synchronous phase detector
- Accuracy \Rightarrow null balancing with digital feedback
- Slow sensor \Rightarrow Over-sampling \Rightarrow simple 1-bit ADC
- Phase detector offset? $10\mu V \Rightarrow \sim 10^{\circ}C$ error!

Chopped PD- $\Sigma\Delta$ **Modulator**



- Phase detector (chopper) offset $\propto f_{drive} \sim 100 kHz$
- Low frequency (20Hz) chopping of phase detector ⇒ 100nV offset ⇒ < 0.1°C error

Smart Thermal Diffusivity Sensor



- Quartz-crystal clock generates f_{drive} (its 100ppm inaccuracy \Rightarrow 0.05°C error)
- ϕ_{ETF} is digitized by a *phase-domain* $\Sigma\Delta$ modulator
- ETF's resolution is limited by thermal noise
- Decimation filter limits noise BW to < 1Hz ⇒ < 0.1°C resolution

Chip Photo



- 0.7µm CMOS, active area 0.5mm²
- P_{circuit} = 2.5mW, P_{ETF} = 2.5mW

Measurement Results (1)

- $f_{drive} = 85 \text{kHz}$
- Near-linear
 characteristic
- As predicted!



Measurement Results (2)

- 16 samples
- NO trimming!
- Spread is
 < 0.5°C (3σ)
- Comparable to batch-calibrated BG sensors



Van Vroonhoven, ISSCC08

But Does it Scale?

- Hypothesis: spread is lithography limited
- So spread in 0.18µm CMOS should be less ~ 0.15°C
- Showstoppers?
 - Spread in D?
 - Packaging stress?



Chip photo

- 0.18µm CMOS
- Active circuit area ~ 0.2mm²
- $P_{circuit} = 0.5 mW$
- P_{ETF} = 2.5mW
- Circuit power (5x) and area (3x) scale down



Yes it Does!



Untrimmed device-to-device spread ±0.2°C (3σ)
 ⇒ 3x improvement





16 devices in plastic TSSOPs (no stress coating)
 ⇒ Slightly more spread, but no shift!

The Killer Application?





Intel 45nm Xeon

Courtesy of S. Rusu Intel

- Multi-core processors ⇒ multiple hot spots
 ⇒ multiple temperature sensors!
- Key requirement = no trimming \Rightarrow TD sensors
- But they need to be faster and more robust ...

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Conclusions

- Thermal diffusivity-based temperature sensors:
 - Are fully CMOS-compatible
 - Performance (accuracy, speed) scales with process

- Achieve 0.2°C (3σ) inaccuracy without trimming
- Comparable to the best <u>trimmed</u> BG sensors

 Are thus well suited for temperature sensing in nanometer CMOS processes

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