A 90-nm CMOS All Digital Phase-Locked Loop

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Outline

- ✓ Introduction
- ✓ Circuit descriptions
- ✓ Measurement Results
- ✓ Conclusions

Introduction

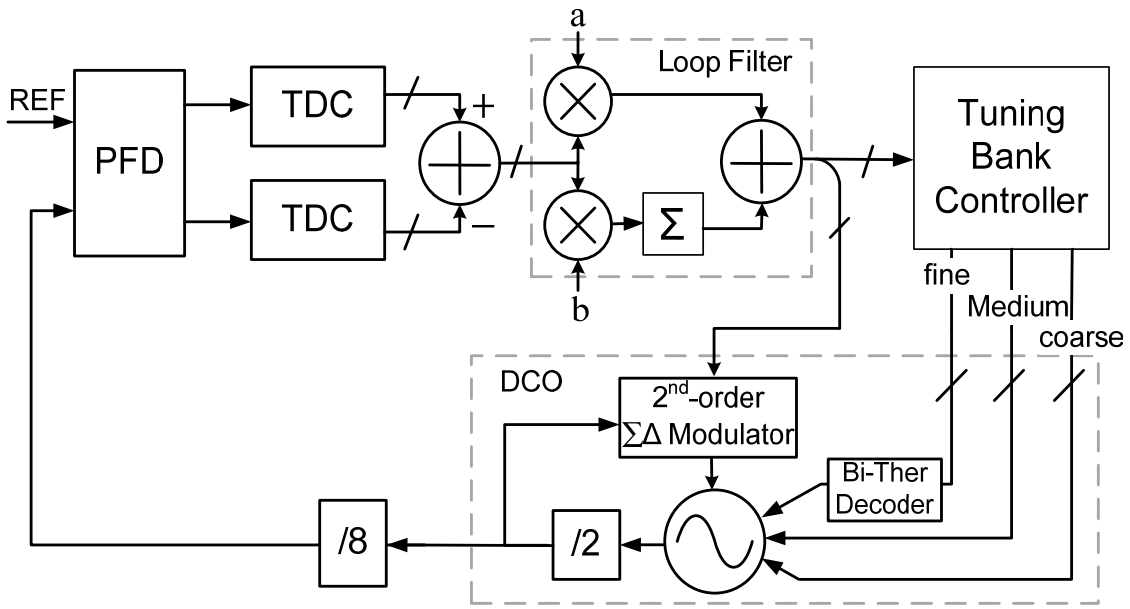
- Good quantization noise requires a small unit delay time in TDC line. A large number of cells of TDC are required considering an wide cover range (period of reference clock).

- Only a small number of TDC cells will be used when the loop (structure.1) is in the locked state. The rest of the cells are used only at acquisition. The shortest-delay cells, resulting in the highest time resolution, are used only in the first part.

- A 5GHz ADPLL based on the uneven-cell TDC is implemented using 90-nm CMOS.

Circuit Description

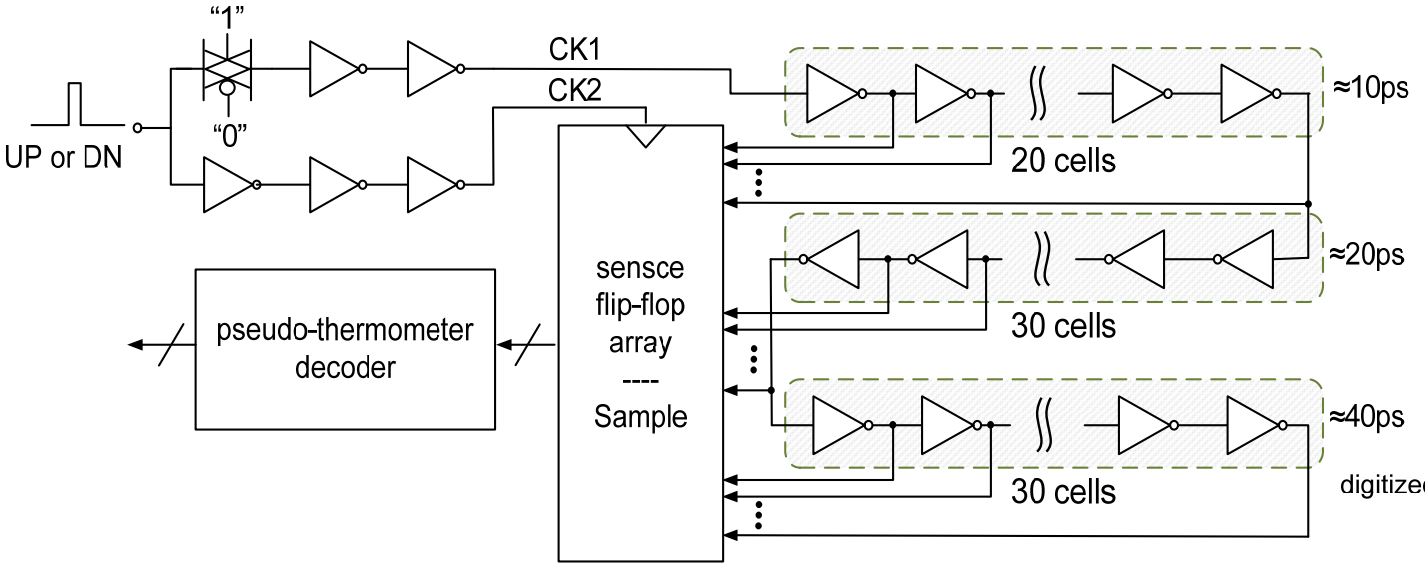
Loop Architecuture



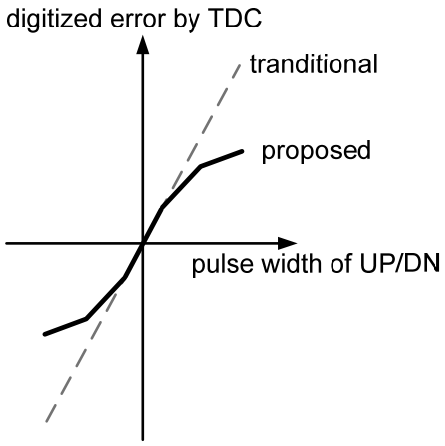
Architecture	ADPLL
Feature size	90-nm CMOS
Area	0.33mm^2
Frequency	(4.8~5.6)GHz
Current	30mA

Circuit Description

Uneven-Delay-Cell Time to Digital Converter

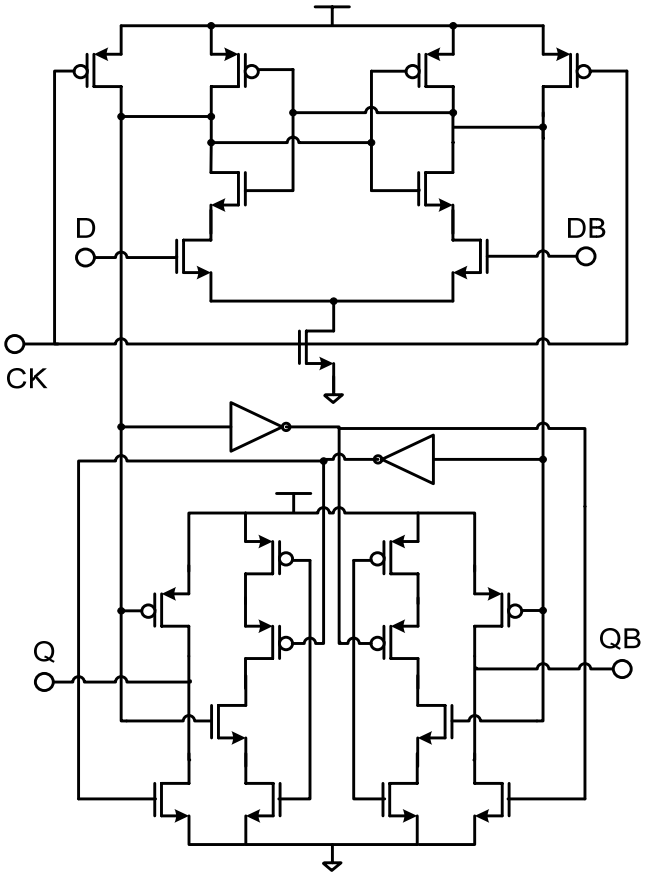


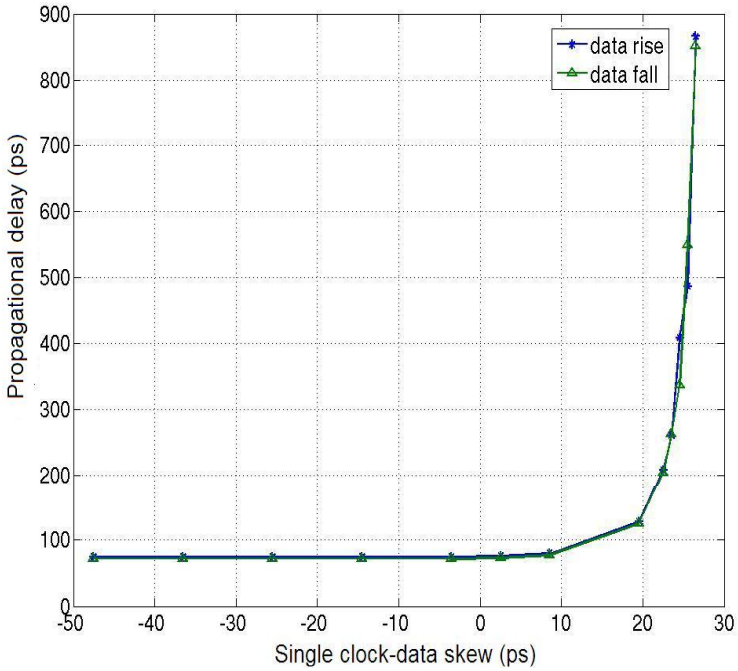
TDC with uneven delay cells



Circuit Description

Uneven-Delay-Cell Time to Digital Converter

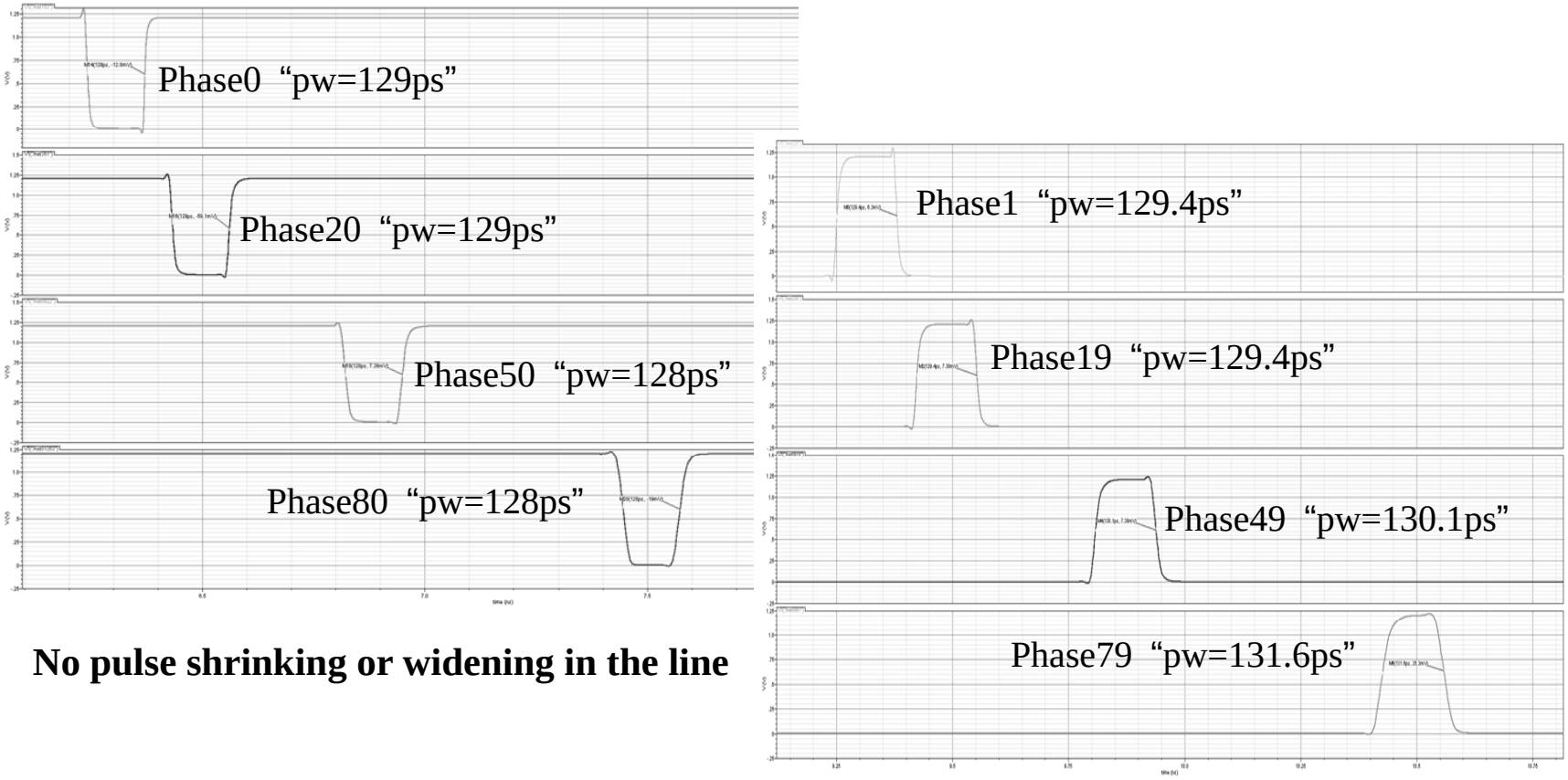




Sense-amplifier-based flip-flop
and its
Clock-Q delay as a function of data-clock skew

Circuit Description

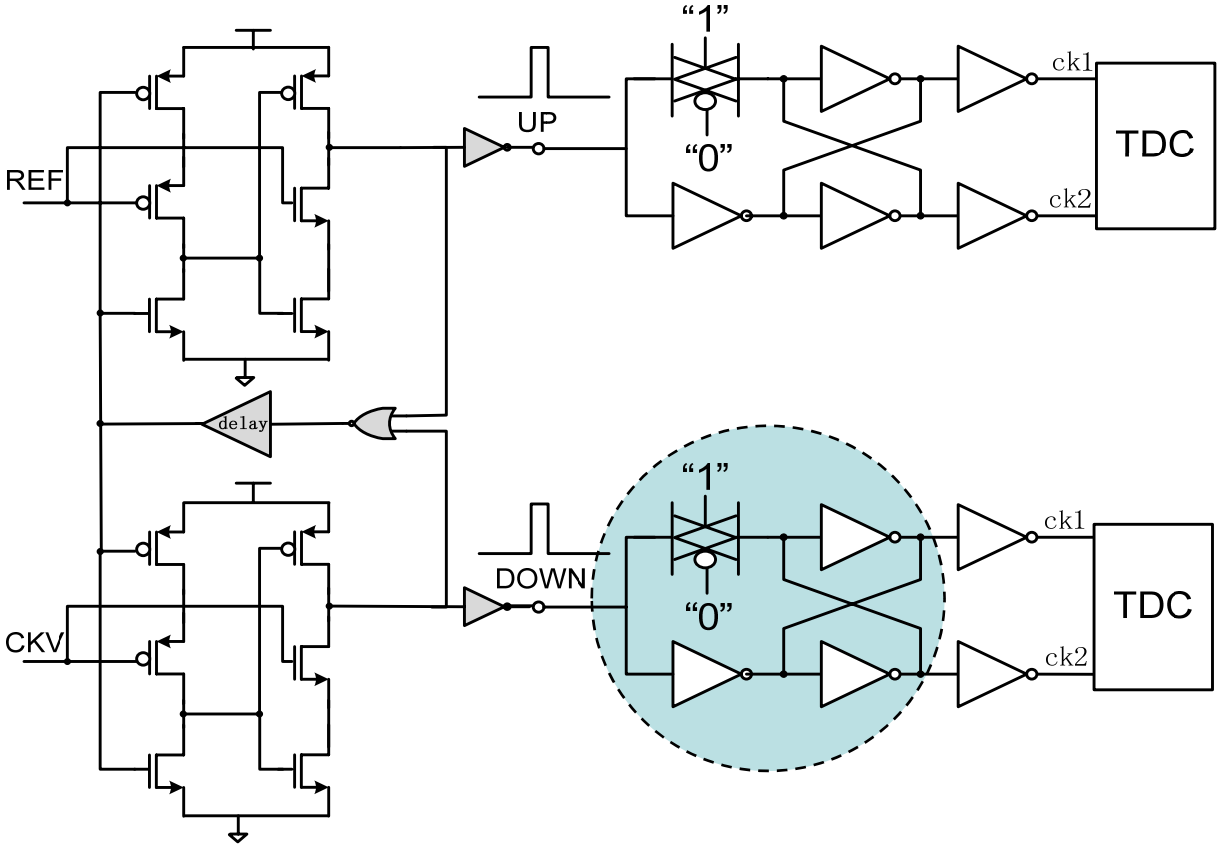
Uneven-Delay-Cell Time to Digital Converter



No pulse shrinking or widening in the line

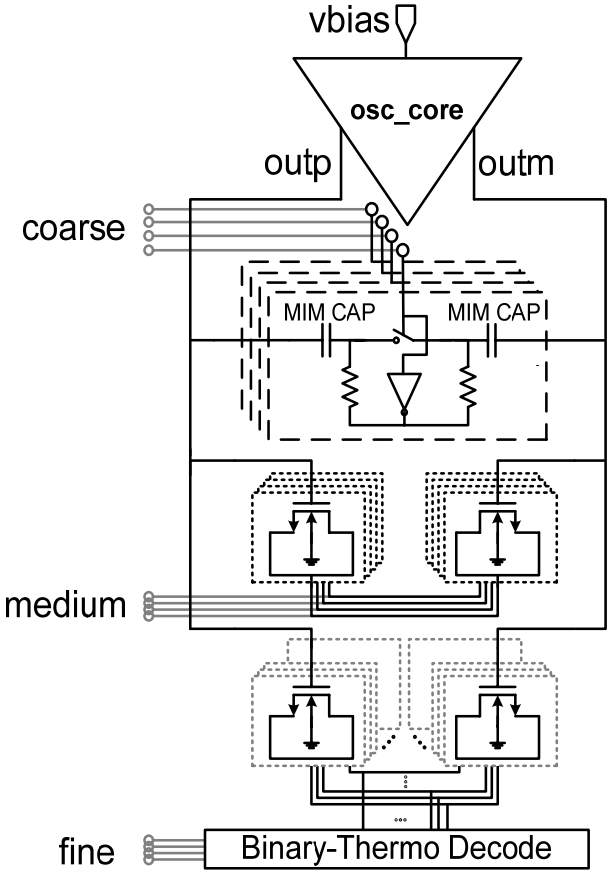
Circuit Description

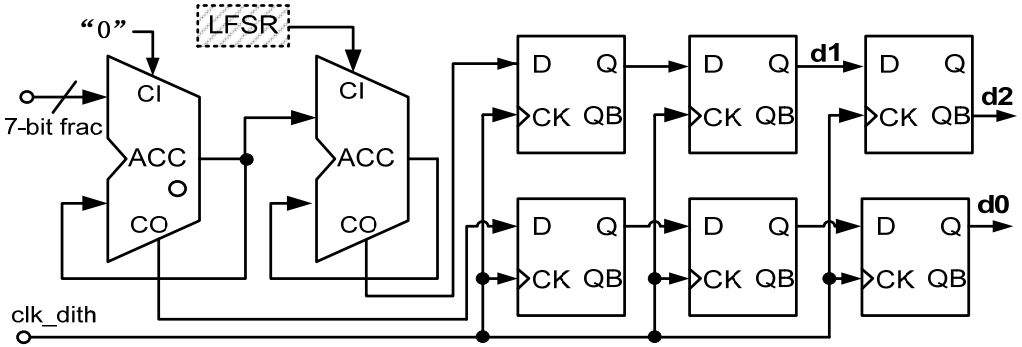
TSPC Phase and Frequency Detector

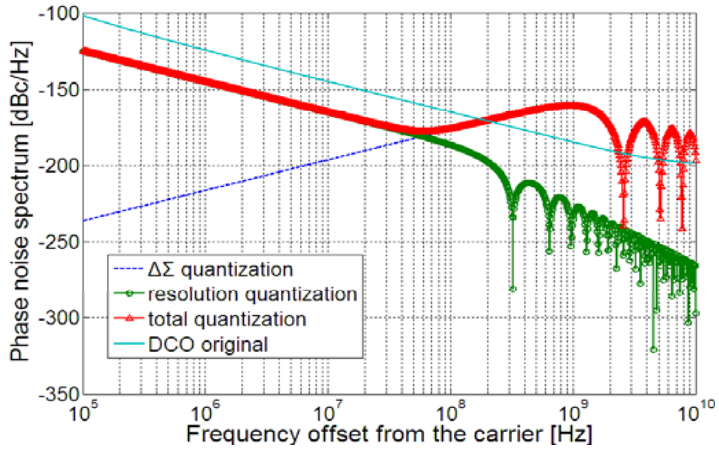


Circuit Description

Digitally-Controlled Oscillator with Sigma-Delta Fractional Modulator





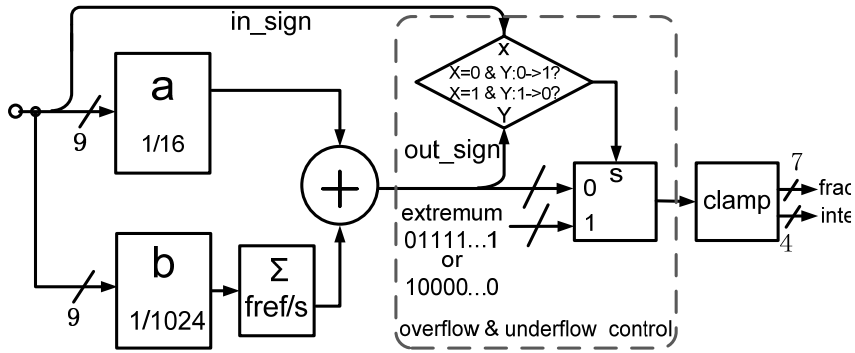


Circuit Description

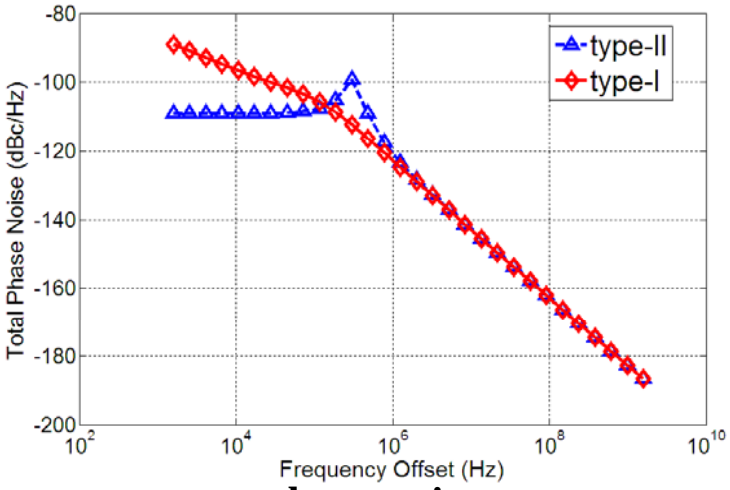
Digital Loop Filter

$$H_{close} = \frac{K_{TDC}K_{DCO}\cdot a\cdot s + K_{TDC}K_{DCO}\cdot b\cdot f_{REF}}{s^2 + K_{TDC}K_{DCO}\cdot a\cdot s/N + K_{TDC}K_{DCO}\cdot b\cdot f_{REF}/N}$$

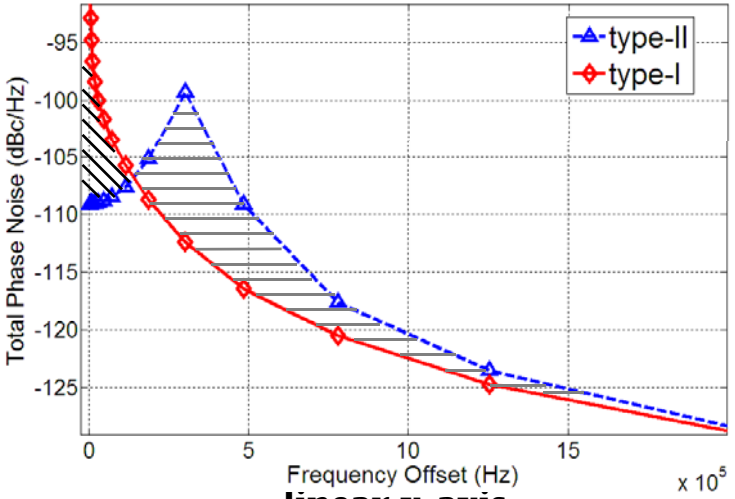
$$H_{TDC,noise} = \frac{(a\cdot s + b\cdot f_{ref})K_{DCO}}{s^2 + K_{TDC}K_{DCO}\cdot a\cdot s/N + K_{TDC}K_{DCO}\cdot b\cdot f_{ref}/N}$$



$$H_{DCO,noise} = \frac{s^2}{s^2 + K_{TDC}K_{DCO}\cdot a\cdot s/N + K_{TDC}K_{DCO}\cdot b\cdot f_{ref}/N}$$



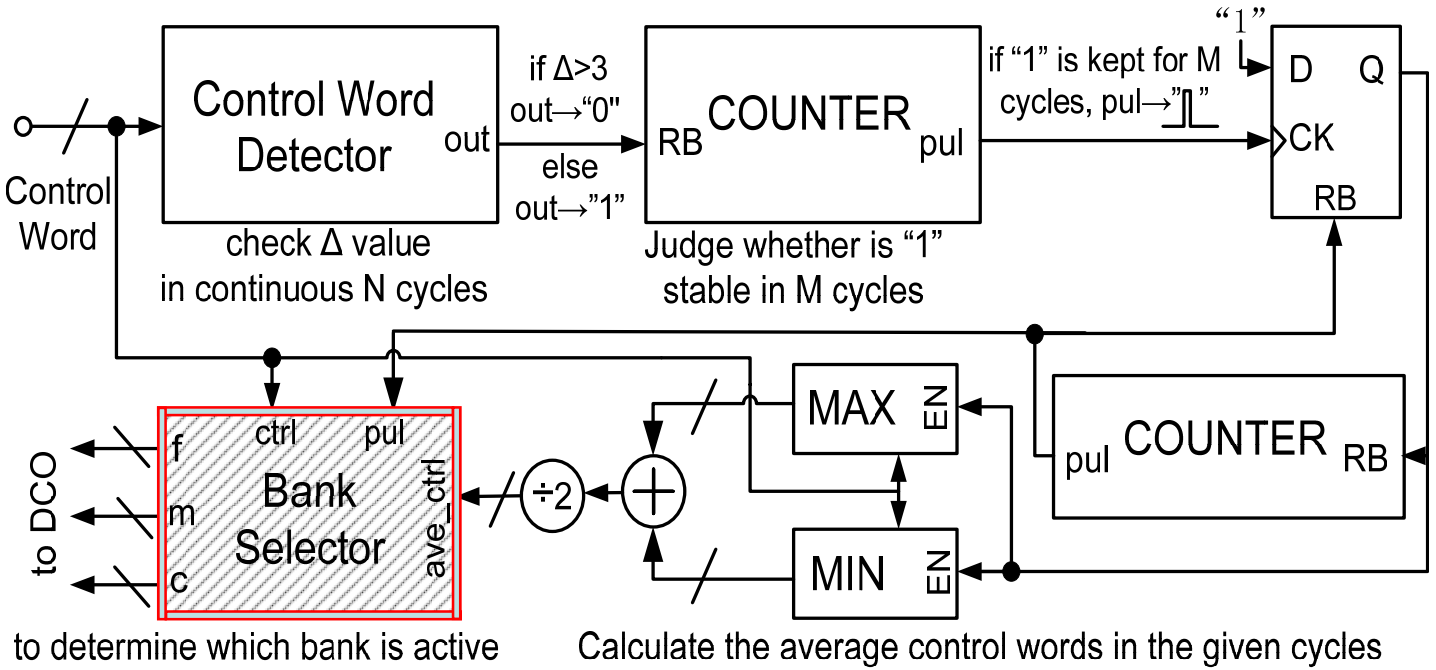
log x-axis



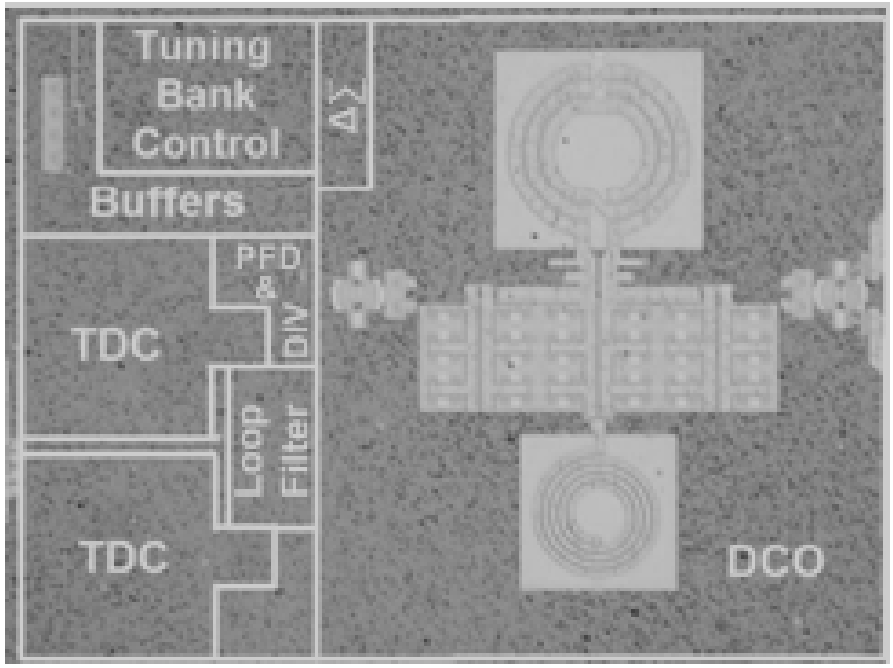
linear x-axis

Circuit Description

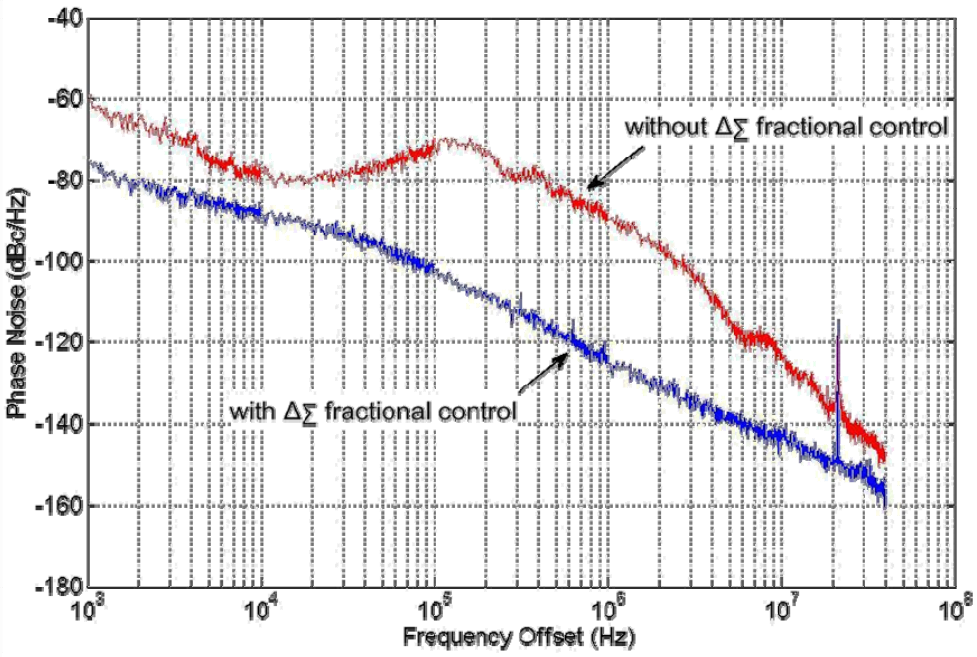
Tuning Bank Controller



Measurement Results

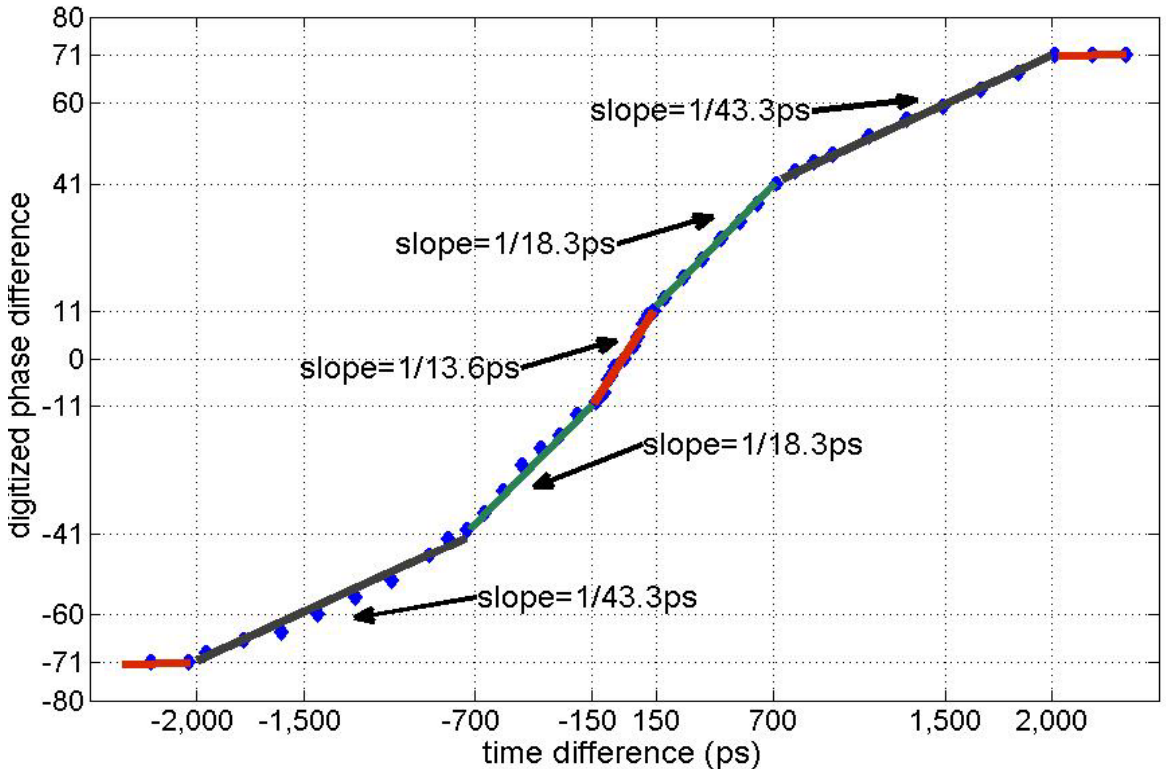


Die photo



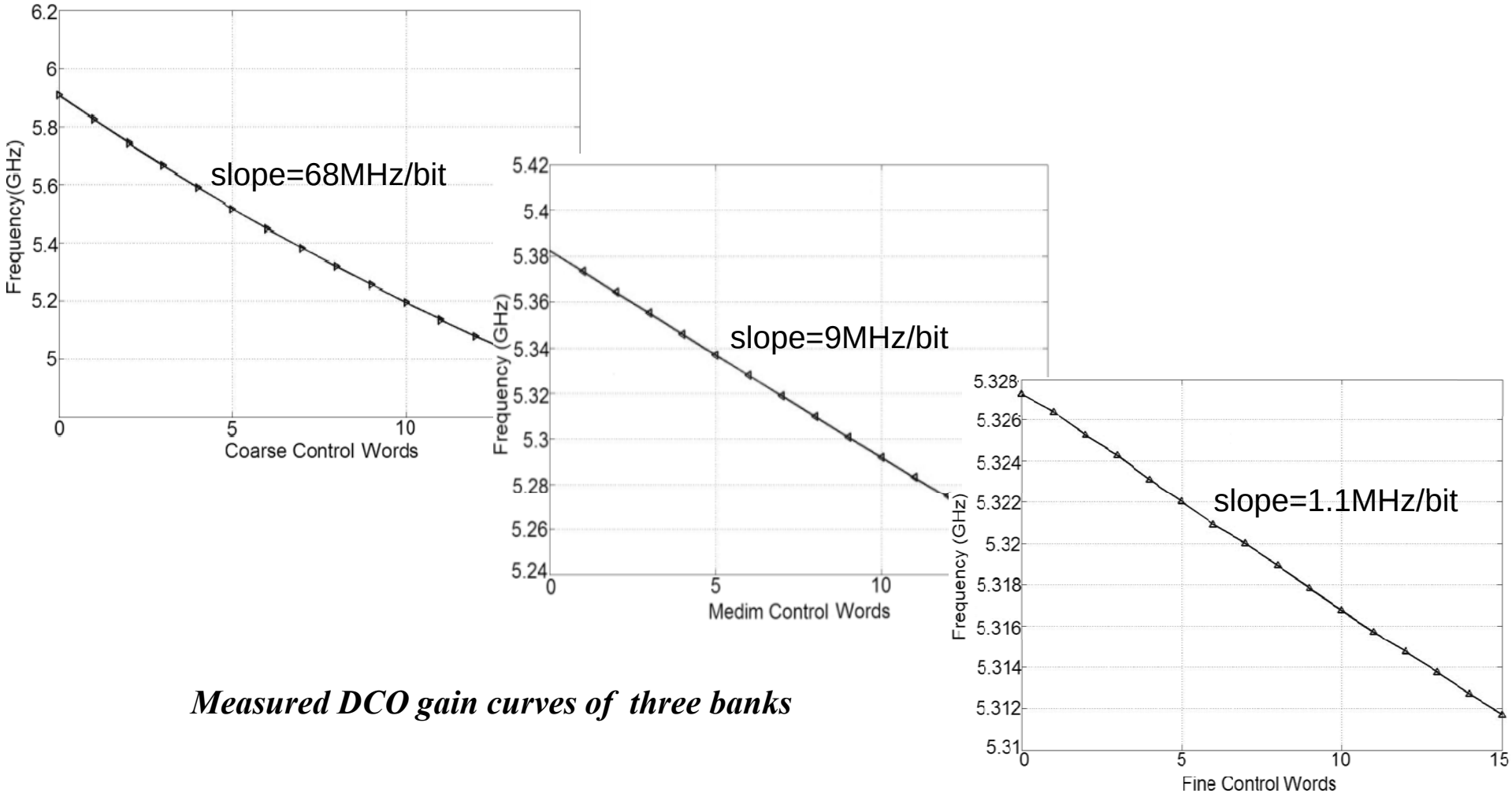
Closed-loop phase noise

Measurement Results



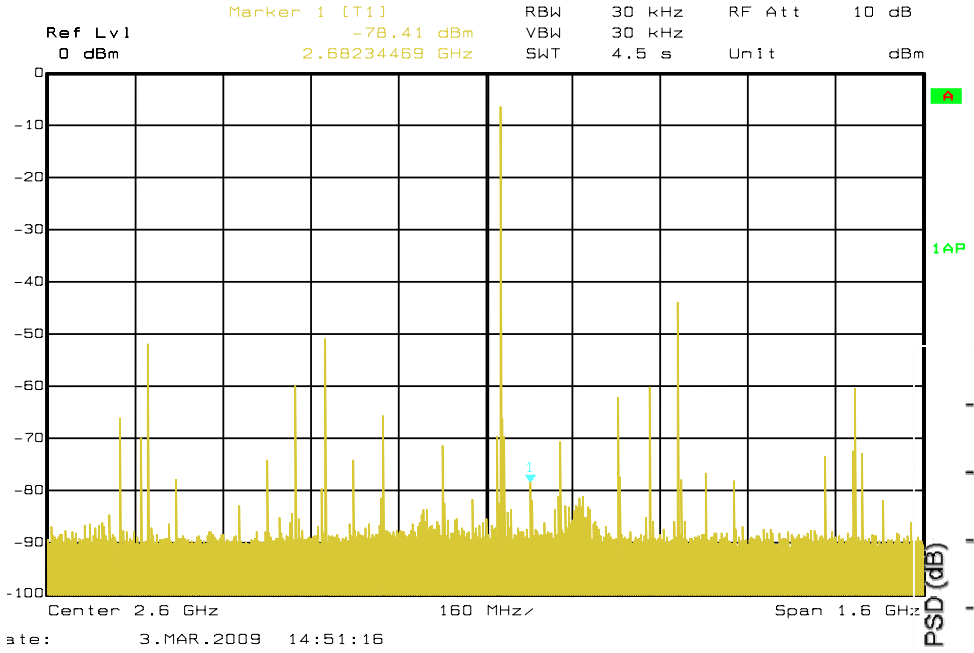
Measured characteristic of Uneven-cell TDC

Measurement Results

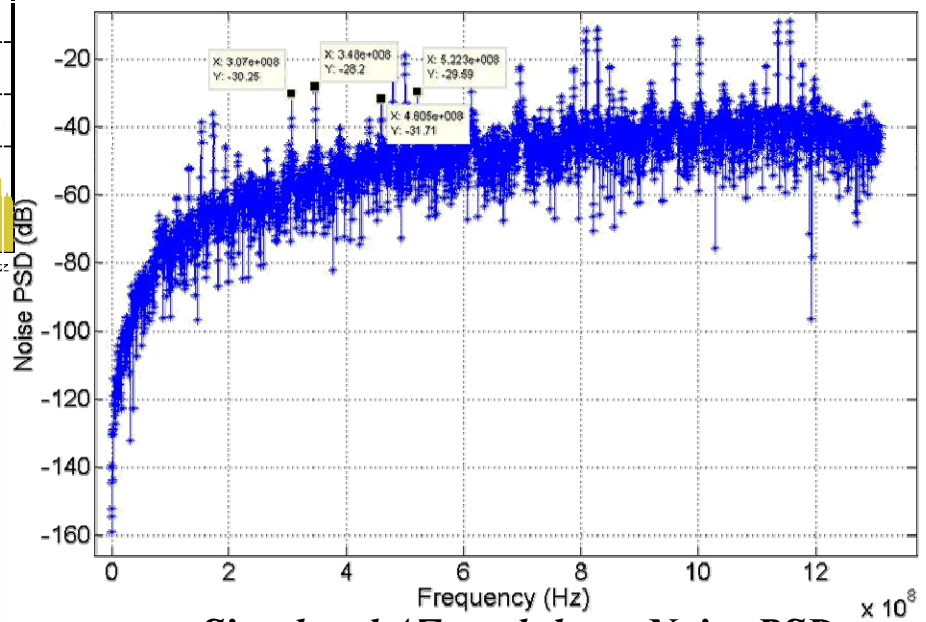


Measured DCO gain curves of three banks

Measurement Results



Measured spectrum



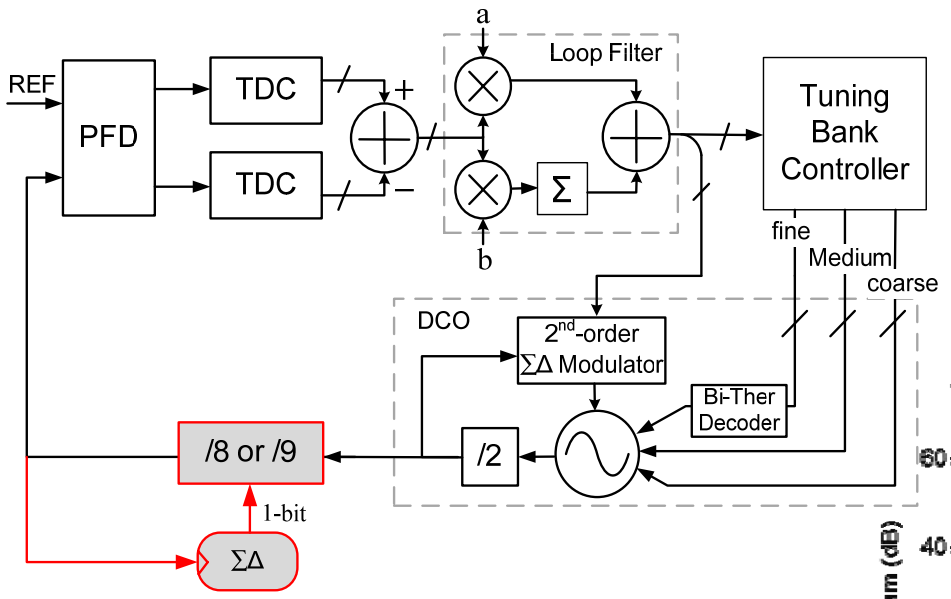
Simulated ΔΣ modulator Noise PSD

Measurement Results

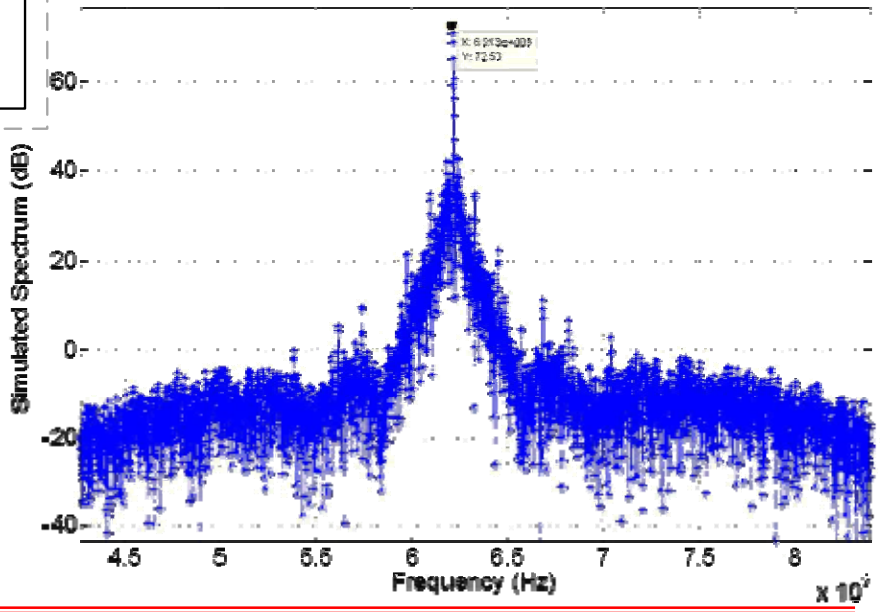
	[17]	[6]	[9]	[18]	This Work
Technology (nm)	65	130	130	130	90
Reference Frequency (MHz)	25	50	26	185.5	322
Carrier (GHz)	3	3.67	3.6	2.2	5.16/2
Phase Noise (dBc/Hz@400kHz)	-101	-108	-117	-100	-115
Phase Noise (dBc/Hz @20MHz)	NA	-150	-152	NA	-152
Power Consumption	<10mW	46.7 mW	40mA	14 mW	36mW
Active Area (mm^2)	0.4	0.95	0.86	0.7	0.33

Performance comparison

Fractional-N ADPLL modification



Simulated fraction-ADPLL spectrum
(output=***8.68*358M***=6.213GHz)



Conclusion

- An uneven-cell TDC based all-digital PLL is designed to reduce the design complexity without sacrificing phase noise performance.

- The loop works self-adaptively thanks to an automatic tuning bank controller which tunes three DCO tuning banks one by one.

- A 1-bit truncation in the loop filter makes the ADPLL achieve a type-I noise characteristic, and track the reference like a type-II PLL.

- The work can also be improved to be a fraction-N ADPLL using a fractional divider.

Thanks!

Q&A