Power Management for Cellular Devices

overview and opportunities

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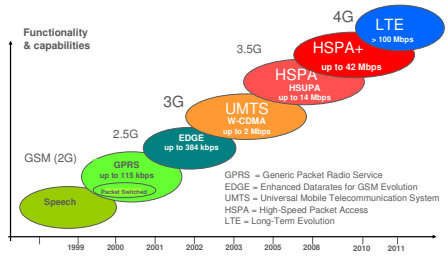
Outline

- **Introduction**
- Power management – basics
- Power management – design approach using dataflow
- Power management – system perspective
  - partitioning
  - interfaces
  - DVFS/GALS
  - analog part
  - Power regulator (DC/DC)
- Towards 50 billion connected devices
- Conclusions

Mobile data evolution

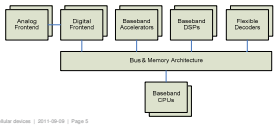


Challenges - multiple standards makes design more complex

- Increasing number of standards to support in mobile devices
- Need efficient computation platform that can be reconfigured by software (Software Defined Radio)

SDR – Digital baseband

- SDR for digital baseband?
  - Highly reconfigurable/programmable modem.
  - Can support standars not yet fully defined by standardization.
  - Increase lifetime of product and architecture due to high degree of reconfigurability
  - Performance scalability
    - Must scale efficiently from 0 to full bitrate
- Multicore architecture
  - Architectures of today are already multicore, but with more or less specialized cores.
  - In the long run too costly to support specialized subsystems.



Some challenges ahead

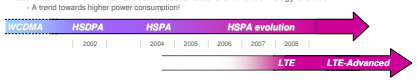
- Significant peak rate increase
  - Cell bandwidths up to ~100MHz needed

- Fragmented spectrum situation
  - Carrier aggregation

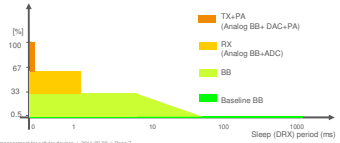
- How to handle these data-rates in portable devices
  - Battery, heat, cost etc
- Graceful scaling
  - Efficiency must be kept for lower bit-rates
  - The system should be "just good enough" at any given time

LTE-challenge and opportunity

- Data rates for LTE / LTE advanced increases faster than the technology evolution
  - A trend towards higher power consumption!



- However, higher data rata rates gives possibility for energy efficient scheduling
  - Energy per bit transmitted can be reduced significantly!



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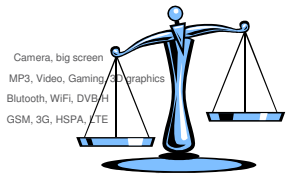
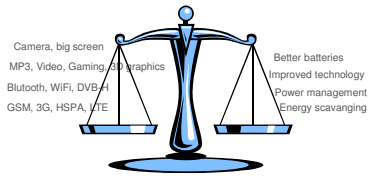
Acheiving energy balance

› One of the most difficult tasks today for design of hand-held devices



Acheiving energy balance

› One of the most difficult tasks for design of hand-held devices
› Finding this balance at the right time to a competitive price



Power management for portable devices - objectives

› Extend battery life
  – Not acceptable to recharge more than once/day for normal use
› Limit size
  – Cope with smaller battery
  – No cooling fan or heat sink
› Control heat
  – Keep the device from
    › shutting down due to overheat
    › rapit aging due to electromigration
    › feel unconfortable to have in hand or pocket

Fundamentals and commonly used techniques for power management at circuit level

› Power in digital domain:
  – $P = \alpha C \times f \times V^2 + I_{leak} \times V$
    α – switch probability
    C – switched capacitance
    f – clock frequency
    V – supply voltage
    I_{leak} – leakage current
› Clock gating
  – Only clock digital part when processing data
› Power gating
  – Power switches to disconnect unused parts from power rails
› Scaling clock frequency/supply voltage
  – For entire chip or for each subsystem
› Design choices
  – Parallel computing, memory architecture, ...
› Power in analog domain:
  – $P \sim DR \times BW \times T$
    DR – dynamic range
    BW – signal bandwidth
    T – duty cycle
› Scaling supply voltage, bias current
› Reconfigure filters, matching, ...

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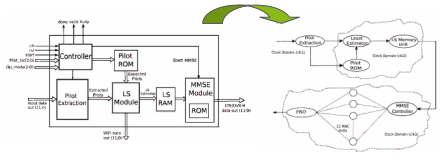
Design approach - Power management using Dataflow design

› Master thesis at ericsson research (Hemanth Prabhu, Sherine Thomas)
› OFDM Channel estimator for LTE, WLAN and DVB-H
  –Original RTL developed as Master's Thesis at ULUND
› Use high-level dataflow representation in CAL to optimize and the generate RTL



CAL dataflow

Design approach - Power management using Dataflow design

› Exploit parallelism to increase performance with minor area increase
› Performance may be traded for power
› Simplified GALS approach with data driven power control
  – GALS = Globally Asynchronous Locally Synchronous

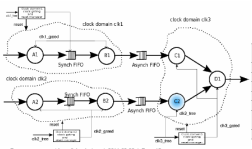


Table: Power Comparison at 200MHz.

	Reference Design	CAL	CAL Low Power
Area [mm²]	0.21	0.22	0.24
Number of clock domains	1	1	3
Power [mW]	24.5	18	10
Clock Freq [MHz]	200	200	200
Throughput [Samples/sec]	63 M	82 M	82 M
Normalized Power [mW/(M Samples/Sec)]	0.38	0.21	0.12
Design Time [Man weeks]	12	4	5

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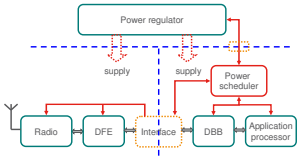
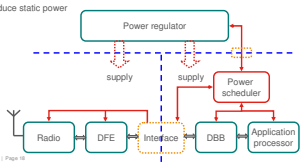
Power management, system perspective



- Example of typical relative power
  - PA power depends on transmitted power (from small to dominating)

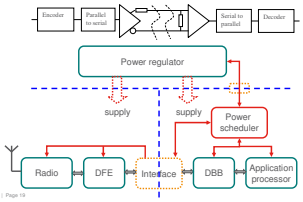
System partitioning and architecture

- Partition into analog/digital or modem/application processor or ?
- Number of subchips, if more than 1, why?
  - Complexity
  - Interference
  - Technology
  - Flexibility
- Memory
  - often 50-60% of design possibly up to 90% of digital part
  - Reducing memory access
  - Enabling memory retention
    - Power switches to reduce static power



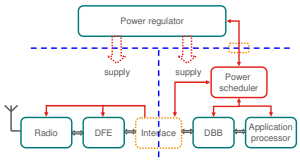
Interface circuits

- Memories, subchips
- Power consuming
  - switching large capacitance at high datarates
  - clock recovery and synchronization



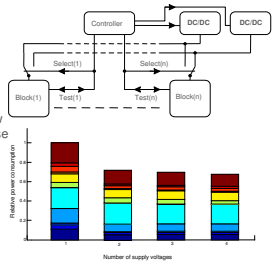
Design/Runtime DVFS (Dynamic Voltage and Frequency Scaling)

- Grouping the components for DVFS
  - Voltage islands with similar requirements on supply
  - Larger number of voltage islands give higher flexibility but also higher overhead
- Also applied on analog and interface components
  - Supply, bias



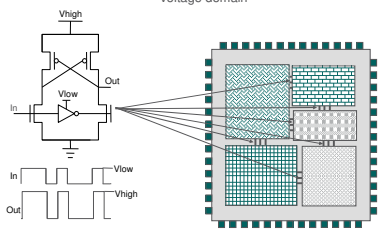
Dual supply – a good DVFS compromise

- Dual supply with local power switches at each subsystem
- Supply voltage levels are optimized for lowest possible power at system level
- Each subsystem select low supply if possible, otherwise high supply
- 2 supply voltages near optimum for many use-cases



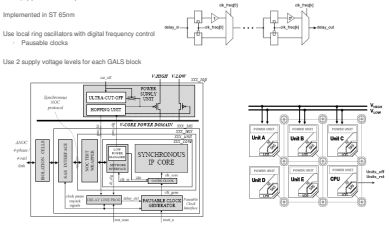
Signal level converter

- Feed-back to restore voltage.
- Needed when going from low to high voltage domain



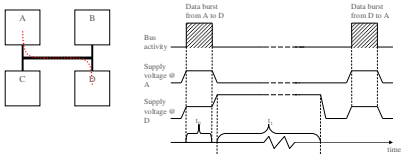
Ex: design using GALS with local oscillators and dual supply

- GALS = Globally Asynchronous Locally Synchronous
- E. Beigne, F. Clermidy, S. Miermont, P. Vivet, "Dynamic Voltage and Frequency Scaling Architecture for Units Integration within a GALS NoC", in Proceedings of the 2nd IEEE International Symposium on Networks-on-Chip (NOCS'08), pp 129-138, april 2008.
  - Implemented in ST 65nm
  - Use local ring oscillators with digital frequency control
    - Pausable clocks
  - Use 2 supply voltage levels for each GALS block



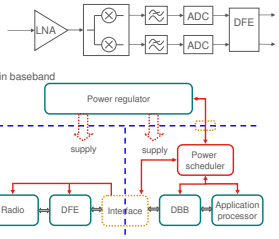
Level converters for multiple voltage domains

- Need to convert signal levels between voltage domains
- Ex: ~10 subsystems ~200 bus bits to each subsystem
- Problem: too many level converters
  - area, delay, power
- Possible solution: use scheduling to transfer data without level shifters
  - How should this be managed without damaging system performance?



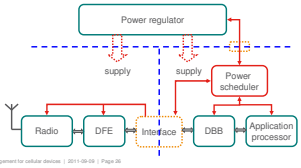
Control analog components to trade perfomance for power

- **Adaptive Radio**
  - Power consumption in the radio can be decreased by adaptation of Radio RX/TX based on knowledge of current radio conditions
- Adjusting
  - bias
  - supply
  - bandwidth
  - matching
  - Filters
  - ...
- based on parameters detected in baseband
  - standard
  - interference level
  - signal quality
  - ...



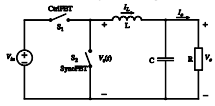
Power Scheduler - Sensing mechanisms

- Sensing
  - modulation, temperature, bitrate, error rate, ...
- Controlling/scheduling
  - supply voltage/current, clock frequency, bias currents, bandwidth, #bits, #iterations, ...
  - System level simulations for evaluation

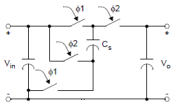


Power regulator - DC/DC converters

- Efficiency ~50-90%
- Buck converter
  - PWM + filter
  - Easy to control Vout using duty factor
  - Need external inductor
- Capacitive switching converters
  - Hard to control Vout
  - No inductor
- LDO (Low DropOut) regulator
  - Linear voltage regulator to stabilize supply
  - Not used for power saving



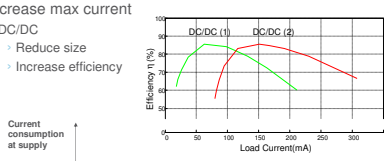
Buck converter

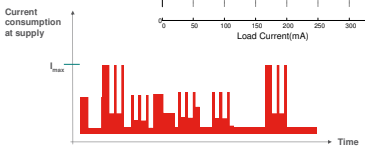


Capacitive switching converter

Runtime - Scheduling for low power in DC/DC converters

- Decrease max current
  - DC/DC
    - Reduce size
    - Increase efficiency





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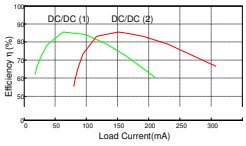

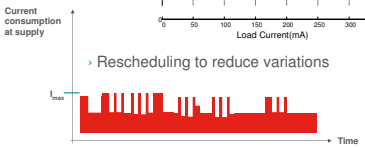

- Rescheduling to reduce variations

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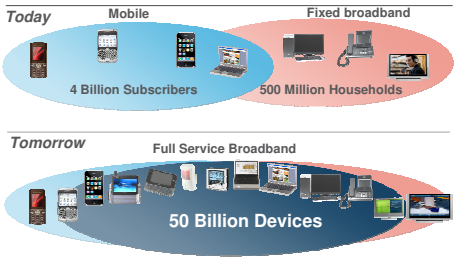
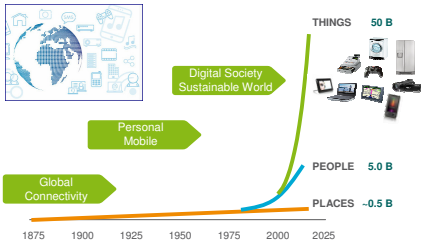
Towards 50 Billion Connected devices



Source: Ericsson

What will be connected?



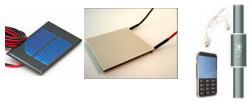
Source: Ericsson

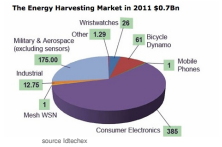
Machine to Machine type connections

- Large variation in performance requirements
- Many will be sensor-like with very limited power supply
  - Idle for long times (hours/days/weeks..?)
  - Able to transmit/receive very short burst of data, possibly at high peak rate
- A huge opportunity for energy scavanging techniqes together with advanced power management
  - Ultra low voltage (sub Vt?)

Energy scavanging

- Photoelectric
  - Light to power e.g. Solar cells
- Thermelectric/Peltier elements
  - Heat to power
  - May also be used for cooling
- Piezoelectric
  - Sound to power
- Electrodynamic
  - Movement to power
- Emerging market for mobile phones





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Conclusions – Power managemant has interesting topics for research

- Co-design of power domains and SW scheduling
  - The ability to re-schedule jobs heavily affects choise of optimum power architecture
  - System level simulations including DVFS strategies
  - Dataflow design
- Digital control of analog components
  - Ensure that no analog components overperform (to the cost of eccess power)
  - Combine with scheduling for global power management
  - Algorithms for sensing and control
- Interfaces
  - Chip-to chip and internal
  - High maximum bitrate at acceptable power level
  - Power should scale with bitrate down to 0.
- Disruptive technologies
  - Energy scavanging?
  - Ultra low voltage design?

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