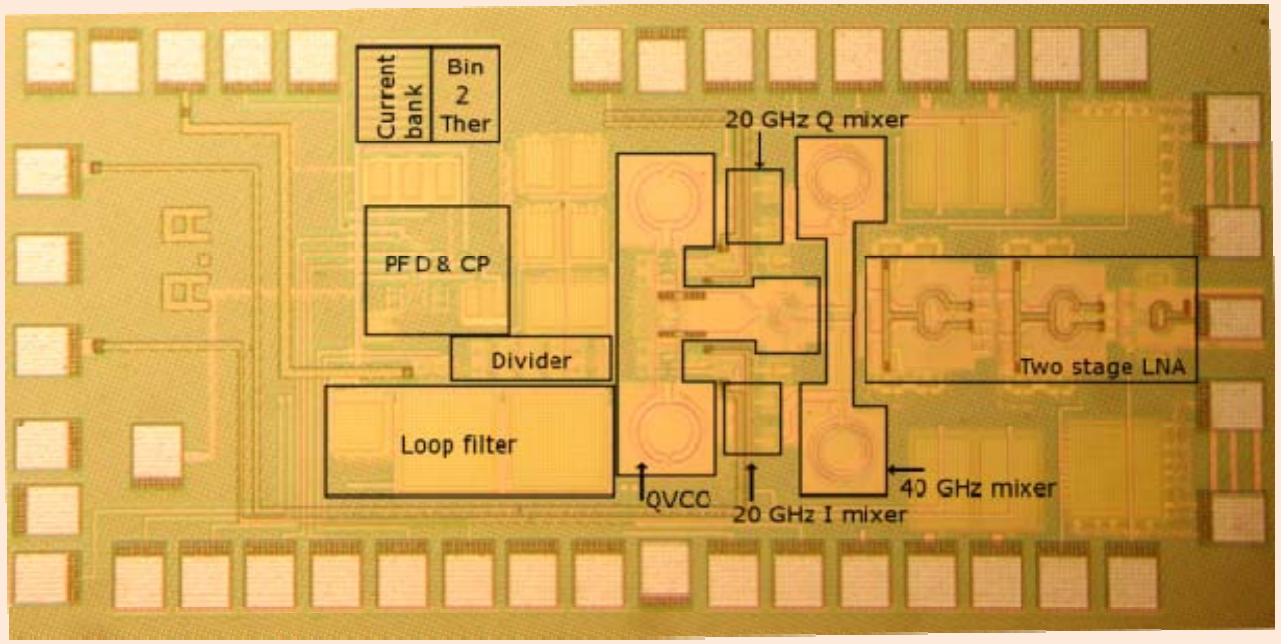
Posters from the 2011 Lund Circuit Design Workshop

September 8-9, 2011

mmWave Beamforming



Working and Measured

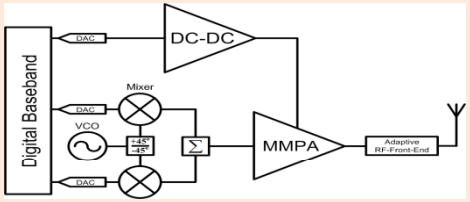
60 GHz, 20 GHz PLL, Transformers, Balun, Mixers, LNAs, QVCO, Binary-to-Thermometer decoder

Andreas Axholt, PhD September 7, 2011

Transmitters with Adaptive Impedance Matching

Jonas Lindstrand Markus Törmänen and Henrik Sjöland

Project Overview

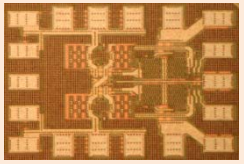


Transmitter System

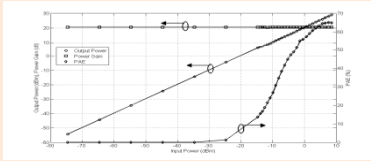
Project Goals:

1. Operation at ALL Relevant Cellular Standards
2. Stable Load Impedance for all Antenna Mismatches
3. Reduced Power Consumption in the Transmitter Chain

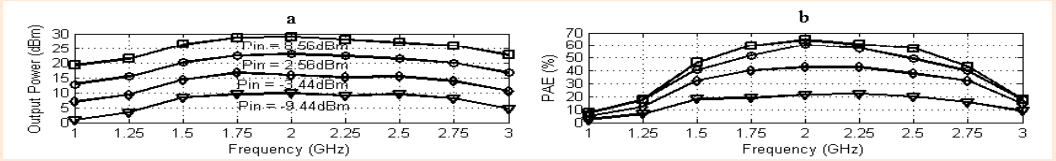
First Chip will be Presented at ESSIRC 2011 - Power Amplifier



PA Chip Photo

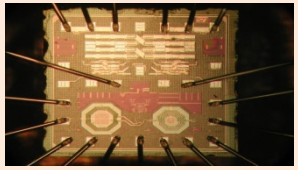


PA Performance @ 2GHz



PA Frequency Response, Output Power (a), Power-Added Efficiency (b)

Second Chip in Measurement – Single Chip Cellular Transmitter



Transmitter Chip Photo

- LO Generator with VCO, Active Poly-Phase Filter and Divider (Invited for Presentation at ISIC 2011)
- New Direct Up-Conversion Power Amplifier with an Output Power in the Range of 1W (30dBm)
- New System Approach Makes the VCO Resistant to Disturbances from the Power Amplifier

SoS System Design on Silicon

VINNOVA

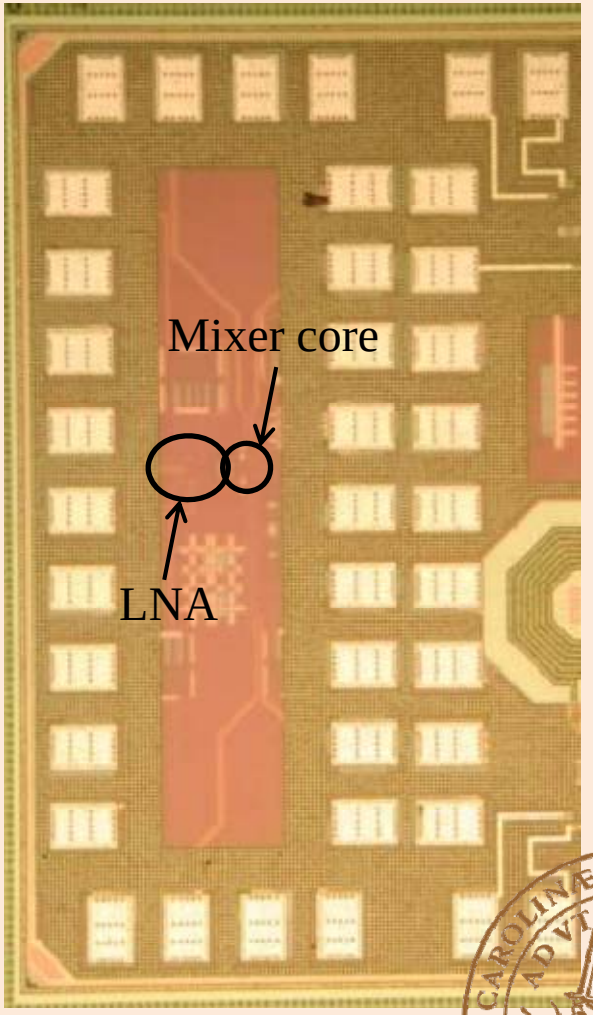
Improving the linearity of a passive down-conversion mixer

Chip under measurement

- Linearize the mixer devices
- Improving the IIP2
- LNA + mixer
- Conversion gain of 12 dB

Problems to be solved

- Make it robust against mismatch and process variation
- Increase the performance for the differential output



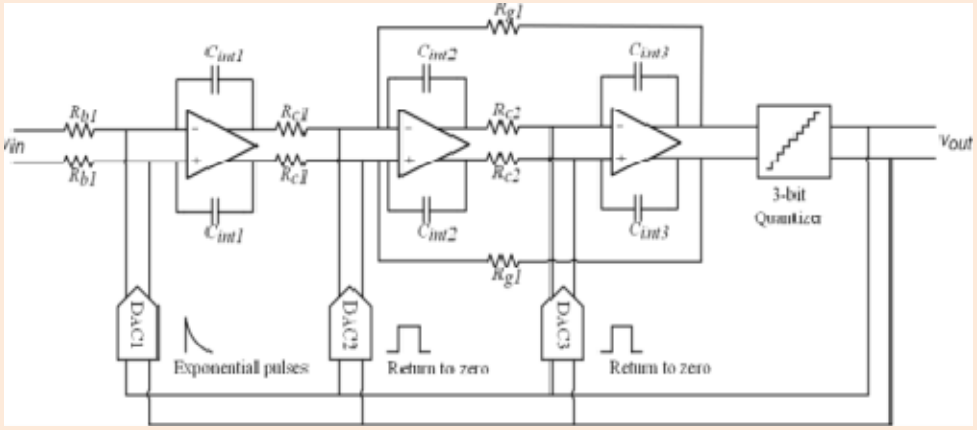
This project is financed by DRAGON

Martin Liliebladh, Henrik Sjöland, Pietro Andreani

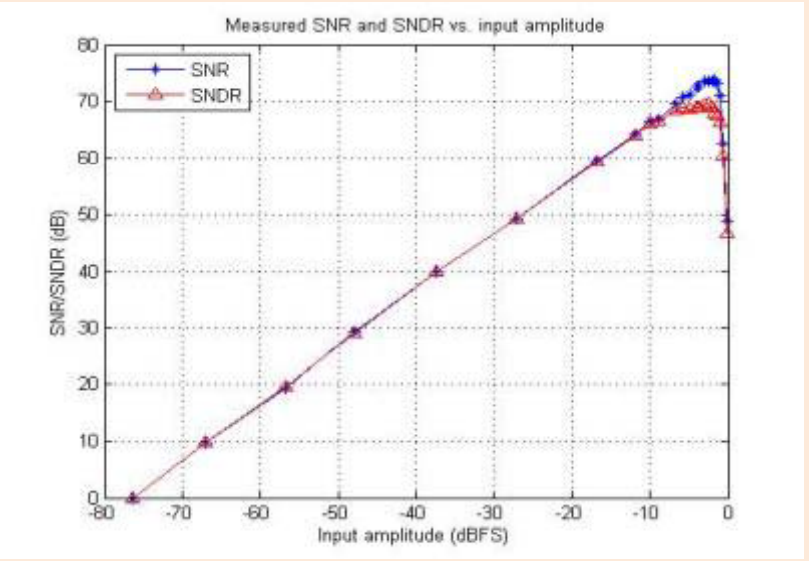
A CT ΔΣ Modulator for Low Power Radios

by Dejan Radjen

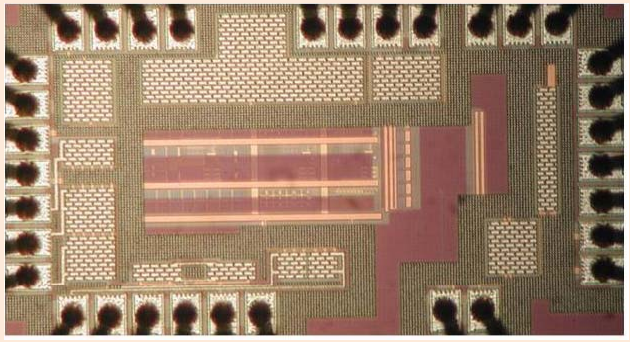
Modulator architecture



Measurement Results



Chip Photo

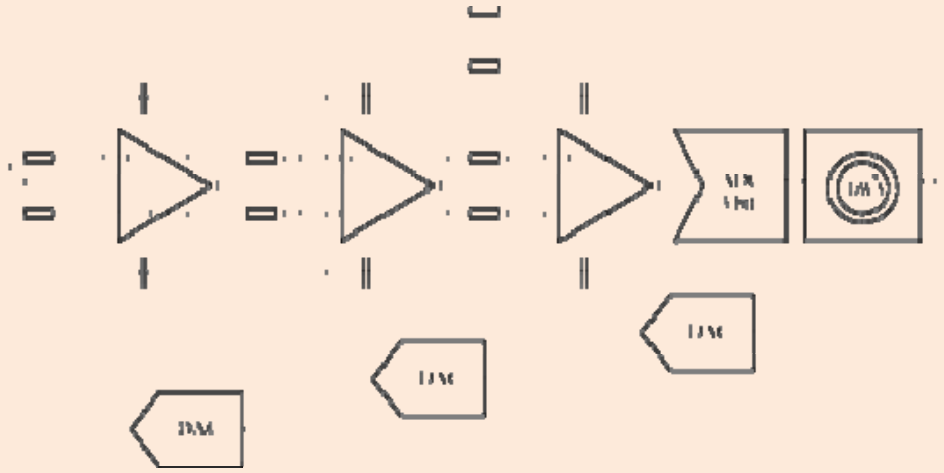


Swedish Foundation for Strategic Research

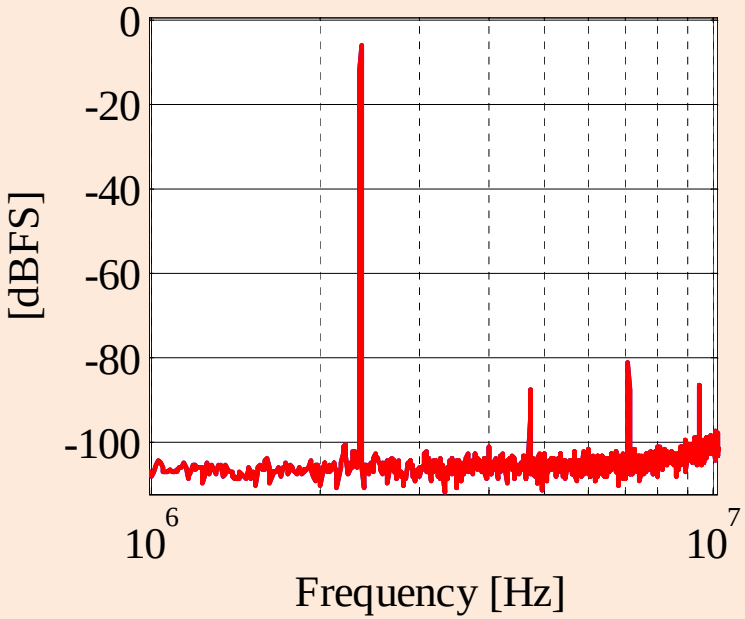
Continuous-Time ΔΣ ADC for LTE

Mattias Andersson

3rd order, 3 bits, 288MHz clock (OSR=16)

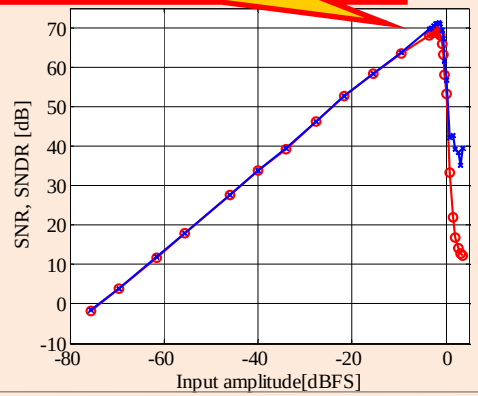


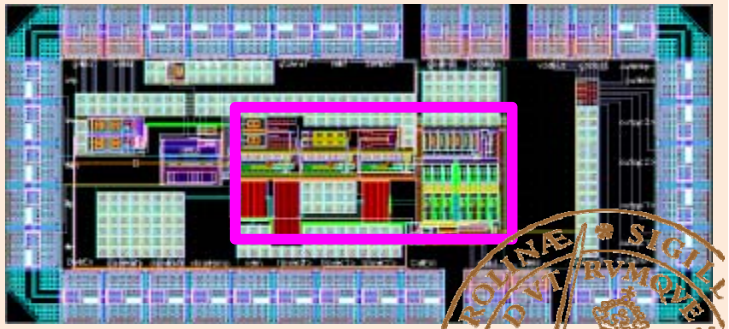
ADC output spectrum



SNDR	69dB
I_{vdd}	6.2mA
FOM	175fJ/conv step
Area	0.1mm²

Peak SNDR 69dB
Peak SNR 71dB



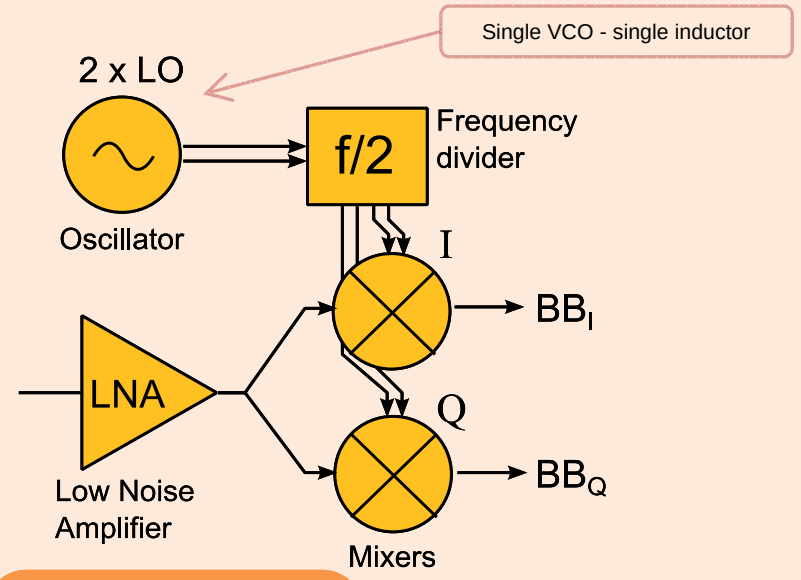


Ultra Portable Devices Front-End

Carl Bryant

Swedish Foundation for Strategic Research

Goals:
<< 1mW
<< 1mm^2 (few inductors)
2.4GHz



LNA+Mixer
175µW
100MHz-2GHz

Norchip 2010

LNA+Frequency Divider+Q. Mixer
282µW, 915MHz

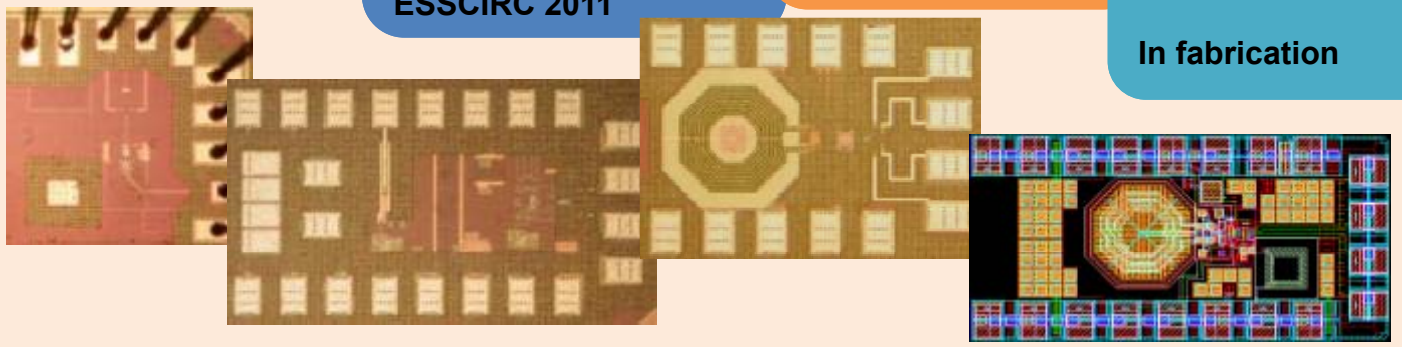
ESSCIRC 2011

VCO+Divider
>2GHz output <250µW

Measured

VCO+Divider+ LNA+Q. Mixer

In fabrication



LUND UNIVERSITY

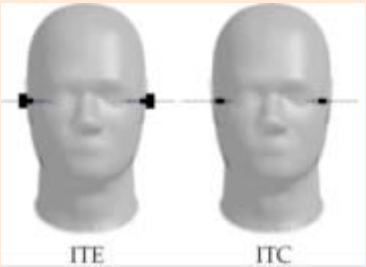
SWEDISH FOUNDATION for STRATEGIC RESEARCH

Antennas and Propagation for Binaural Hearing Aids

By: Rohit Chandra, PhD student, Lund University

OBJECTIVES

- Investigating the possibility of establishing a wireless link between the binaural hearing aids in 2.45 GHz ISM band using miniaturized antennas.
- Comparison between a homogeneous phantom (SAM) and a heterogeneous phantom (Duke) for estimating the ear-to-ear link loss.
- Investigating the effects of the pinnas (protruding part of the outer ear) and the lossy skin on the ear-to-ear link loss
- Measurements to verify the effect of the pinnas

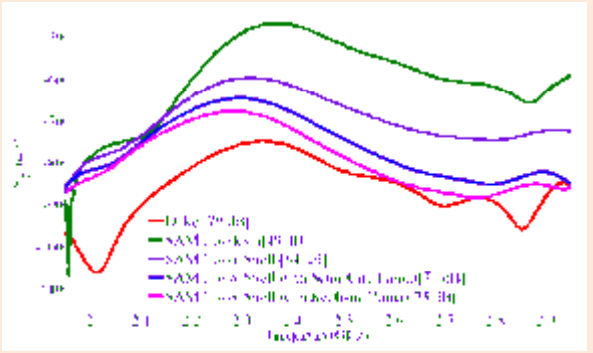


Antenna Placements

SAM with pinna

Duke

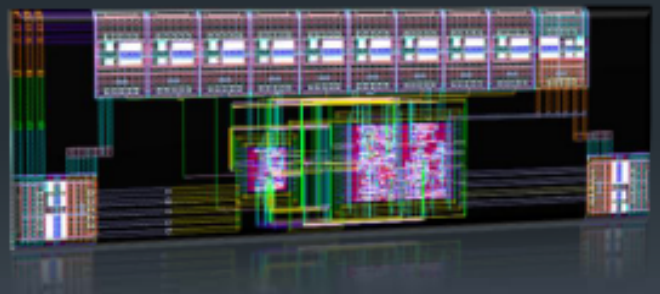
Measurements



Effect of lossy skin and pinna

Ultra Low Energy Digital Circuit

- Requirements
  - Low Energy Dissipation
  - Low Area
  - Satisfactory Throughput
  - Reliability



- Design Space?
  - Architectures?
  - Technology Selection?
  - Energy Min. Voltage?
  - Switching Activity?

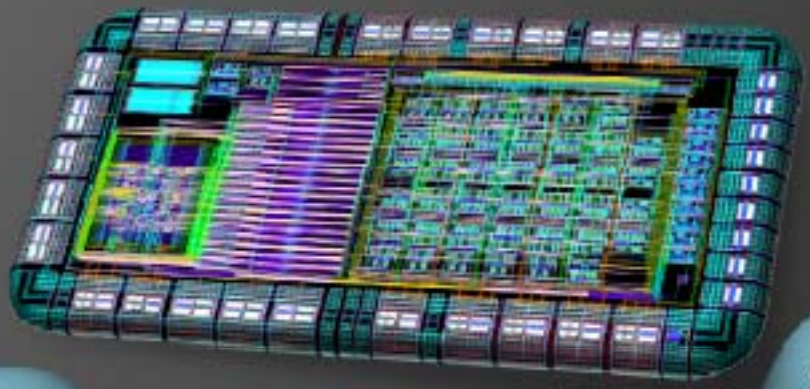
- S.M.Yasser Sherazi
- Joachim N. Rodrigues
- Henrik Sjöland
- Peter Nilsson

Analog Decoding

In 65-nm CMOS

Reza Meraji
John B. Anderson
Henrik Sjöland
Viktor Öwall

I Low Power



III High Speed

II Small Area

I Sub-threshold region

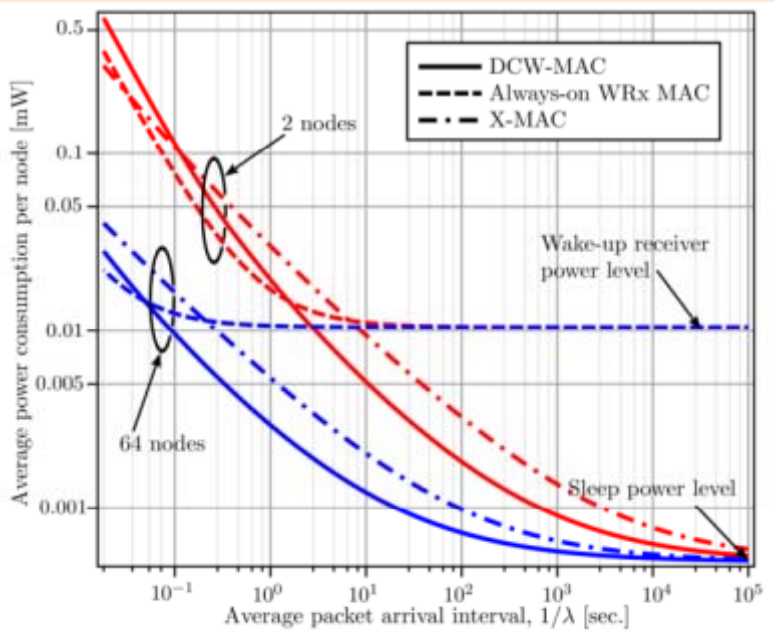
II Simple analog multipliers

III Parallel continious time processing

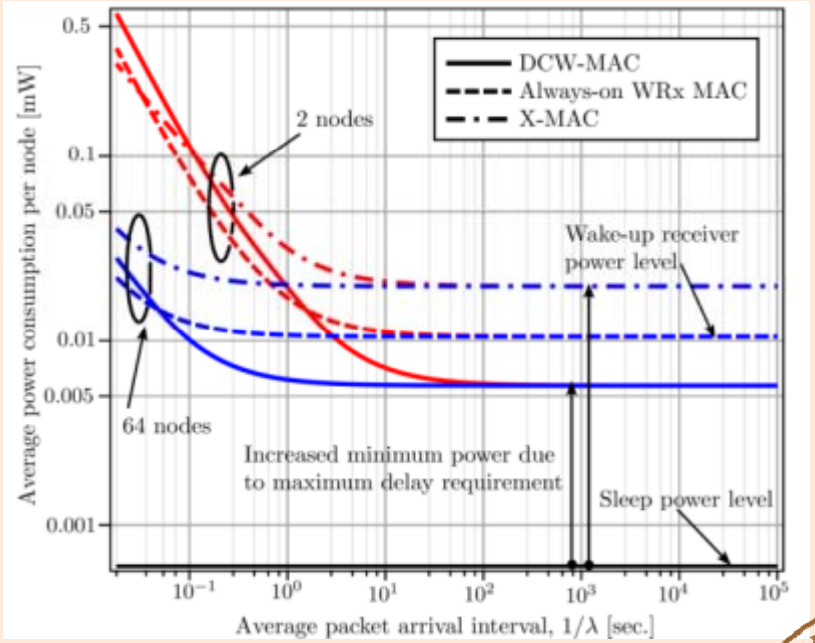
Energy efficient medium access scheme DCW-MAC scheme

by Nafiseh Seyed Mazloum

Duty-**C**ycled **W**ake-up receiver (WRx) **MAC** combines ultra low-power WRxs and optimal duty-cycled listening.

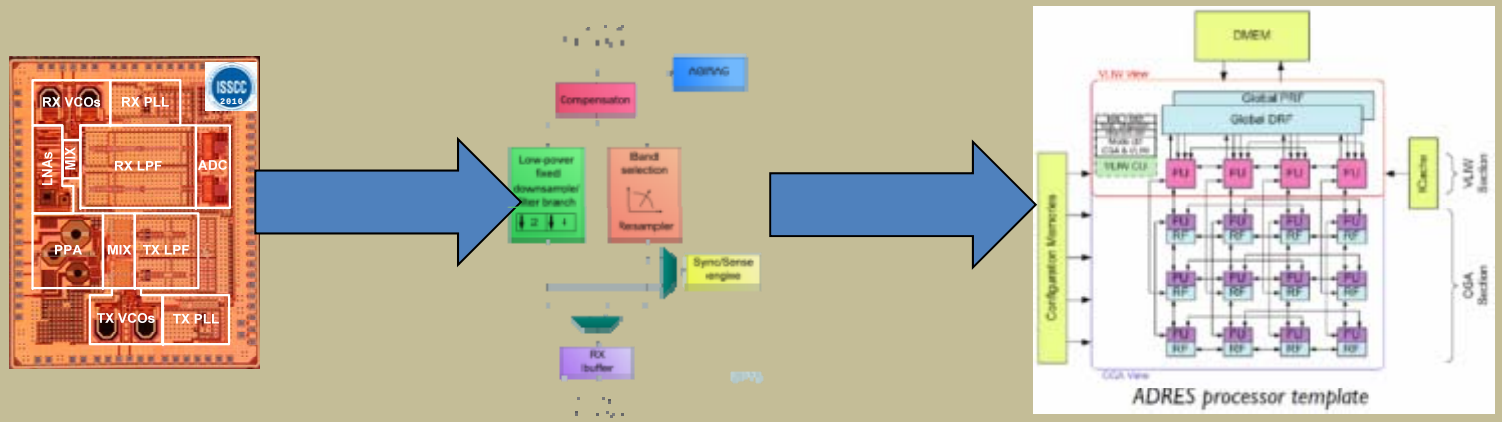


a) No delay requirement



b) With delay requirement

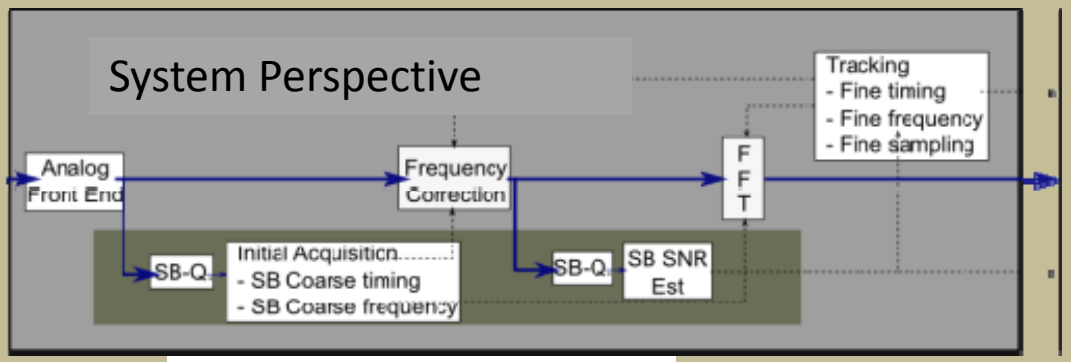
Optimal architectural partition for LTE-A @ IMEC by Isael Diaz

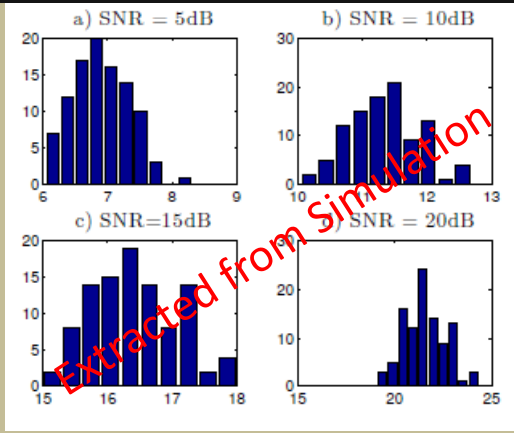


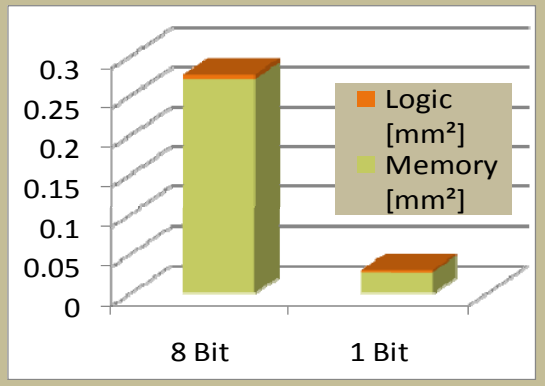
- **Maximizing Performance**
  - What operations are to be placed in the Front End and what on the Baseband engine for optimal performance?
    - Multi-band filtering, Re-sampling, Compensation, FFTs, etc...
- Minimizing Power Consumption under efficient area constraints
  - Characterization of power consumption under the various LTE-A scenarios.

Minimizing OFDM Receiver Complexity with Sign-Bit Estimation Techniques

by Isael Diaz







Standard	Fs	Current
LTE	31 MHz	0.52mA
DBV	10 MHz	0.18mA
WLAN [20MHz]	20 MHz	0.32 mA
WLAN [40MHz]	40 MHz	0.6 mA

Measured Results

SB-SNR Estimation:

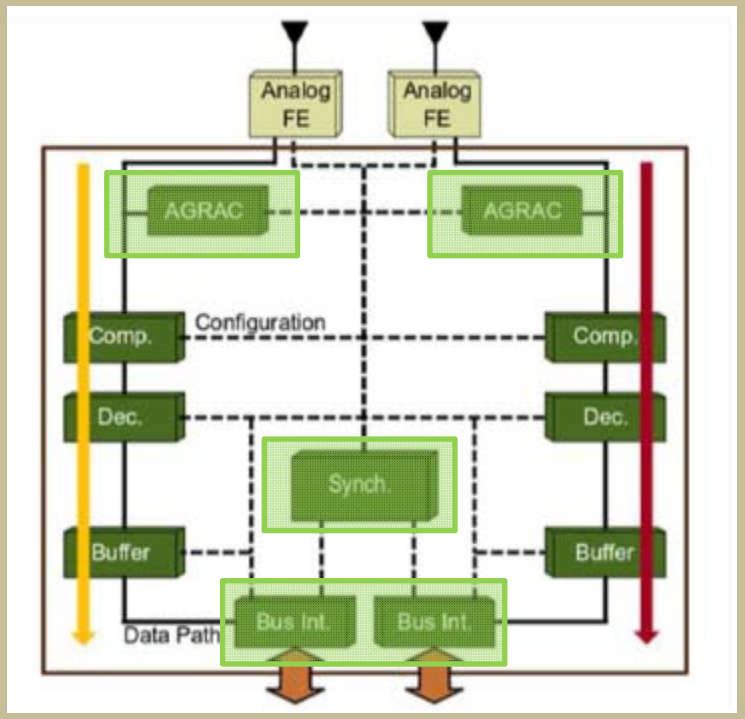
- Same architecture as SB-Synch.
- Capable to distinguish between coarse SNR.

SB-Synchronization:

- Up to 90% area reduction from an 8-bit implementation.
- Low Power consumption down to 0.18mA per symbol for DVB-H.

Multibase Closure

by Isael Diaz, Chenxin Zhang, Joachim Rodrigues and Viktor Öwall



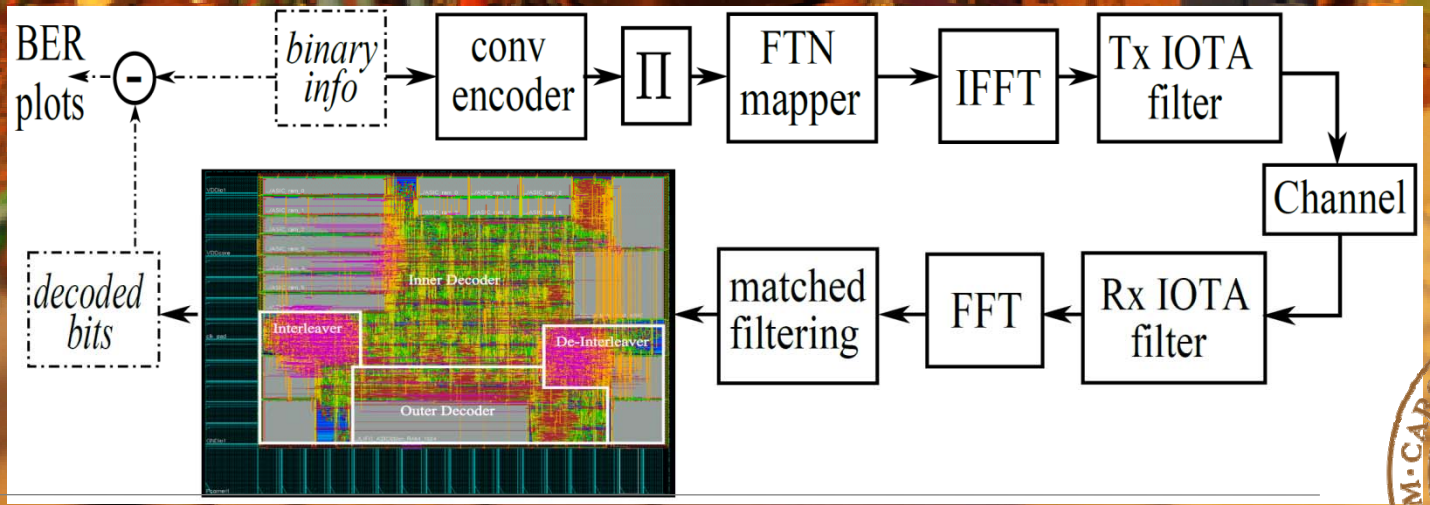
- 2 standard concurrently:LTE, WLAN and DVB-H
- Total area 5mm2, Infineon LP 65nm CMOS

- New transmitted concept presented for future multi standard terminals.
- Concepts have been proven by actual physical fabrication demonstrating the feasibility of the architecture.
- Functional verification of critical components is finalized, even though measurements of the entire architecture is still ongoing.

Faster-than-Nyquist signaling for improved bandwidth efficiency.

-Deepak Dasalukunte

Transmitter and receiver architectures of an FTN multicarrier system has been evaluated and a receiver has been implemented in ST 65nm CMOS.
FTN has been showed to be feasable from a hardware perspective.

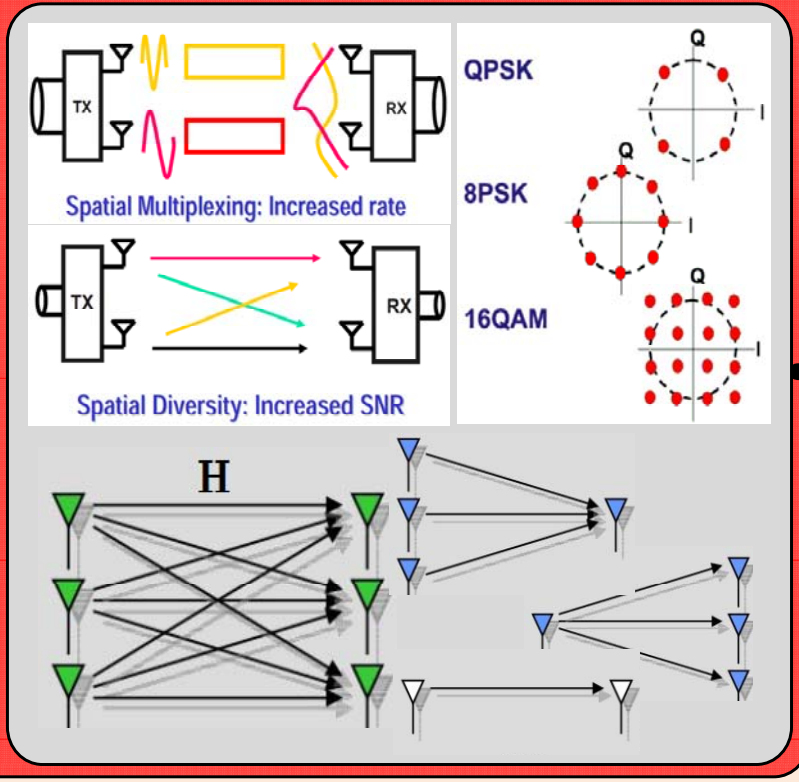


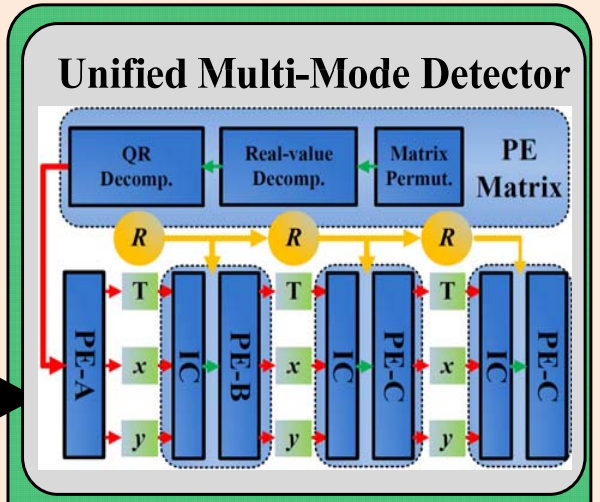
Unified multi-mode MIMO detector for LTE-A downlink

Liang Liu, Johan Löfgren, and Peter Nilsson
Department of Electrical and Information Technology, Lund University, Sweden

- *More Function*
- *Higher Speed*
- *Better Performance*
- *… …*

We want more





- *Smaller area*
- *Less power*

We pay less

Detect multi-mode MIMO signal with smaller area and less power

For LTE-A hand-held devices

Improved Matching Pursuit Algorithm and Architecture for LTE Channel Estimation

Johan Löfgren, Ove Edfors, and Peter Nilsson

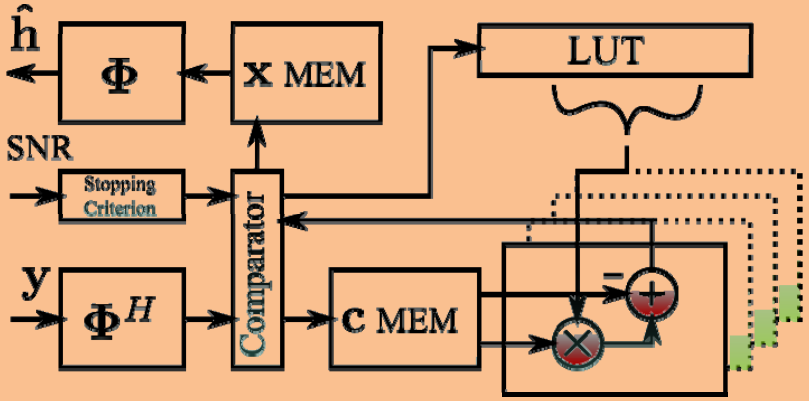


TABLE I
MULTIPLICATIONS IN DIFFERENT STAGES

Design	One Iteration	IDFT/DFT	IFFT/FFT	Full Estimate
Original	512	~614K	~22.5K	~96K
Proposed	300	720K	~27K	~84K

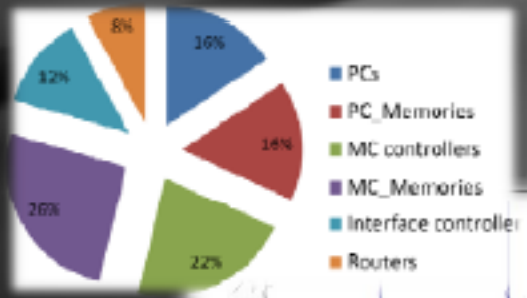
- Channel Estimation is important
  - Compressed Sensing and Matching Pursuit gives good estimate
- This work presents an improved Matching Pursuit algorithm
  - It is shown that large savings can be achieved by, counter-intuitively, increasing the resolution

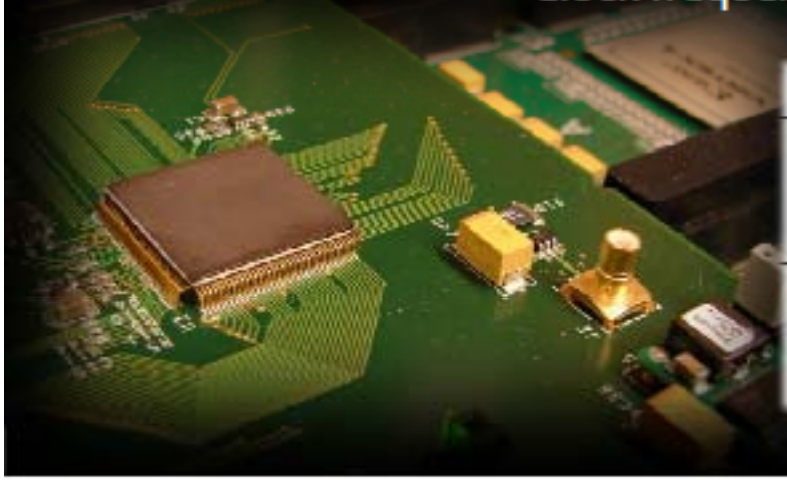
Reconfigurable cell array

by Chenxin Zhang

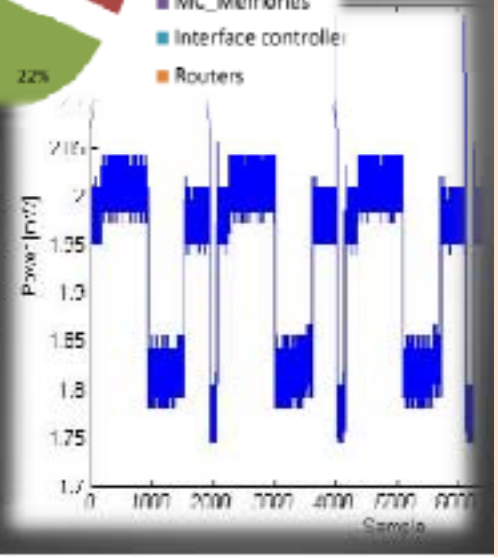
- Heterogeneous cell array
- Hierarchical routing network
- Centralized & Distributed cell configuration
- Task level hardware sharing
- A software-centric programming approach
- Algorithm-level exploration on one platform

- Multi-standard OFDM coarse synchronization
  - 2x2 Cell array
    - Area: 0.479 mm² in 65 nm CMOS
      - Clock frequency: 534 MHz





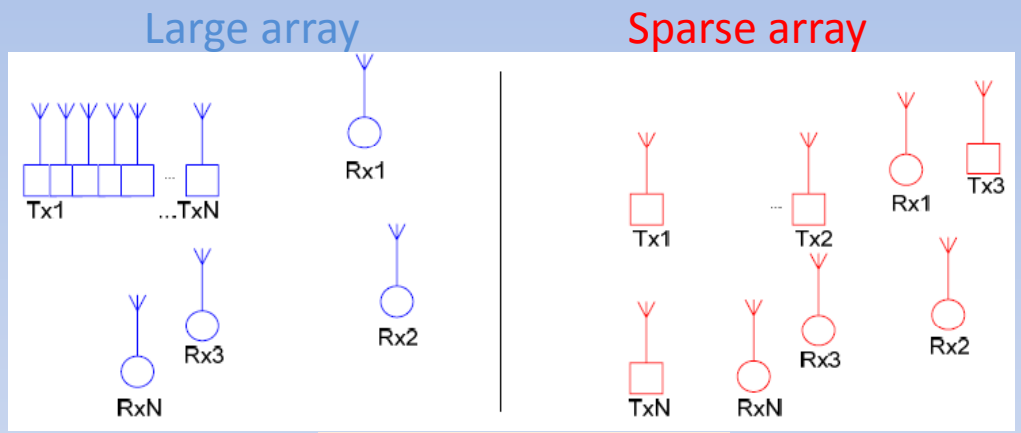
Concurrency	Standard	Quantization accuracy
Single-Stream	802.11n	4 bits
	LTE	4 bits
	DVB-H 2K	4 bits
	DVB-H 4K	2 or Sign bit
	DVB-H 8K	Sign bit
Dual-Stream	802.11n & 802.11n	4 or 2 bits
	802.11n & LTE	2 bits
	802.11n & DVB-H 2K	2 bits
	LTE & LTE	2 bits
	LTE & DVB-H 2K	2 bits



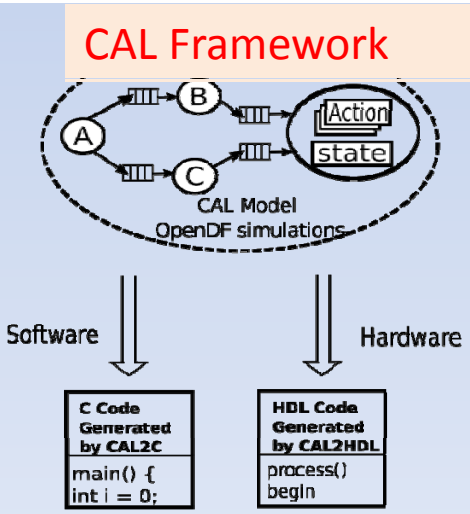
Distributed Antenna Systems

Hemanth Prabhu, Joachim Neves Rodrigues, and Ove Edfors

- **Antennas (~100) may be grouped to form large arrays, or distributed in the environment as a sparse array.**
- **A central processing unit performs joint processing.**



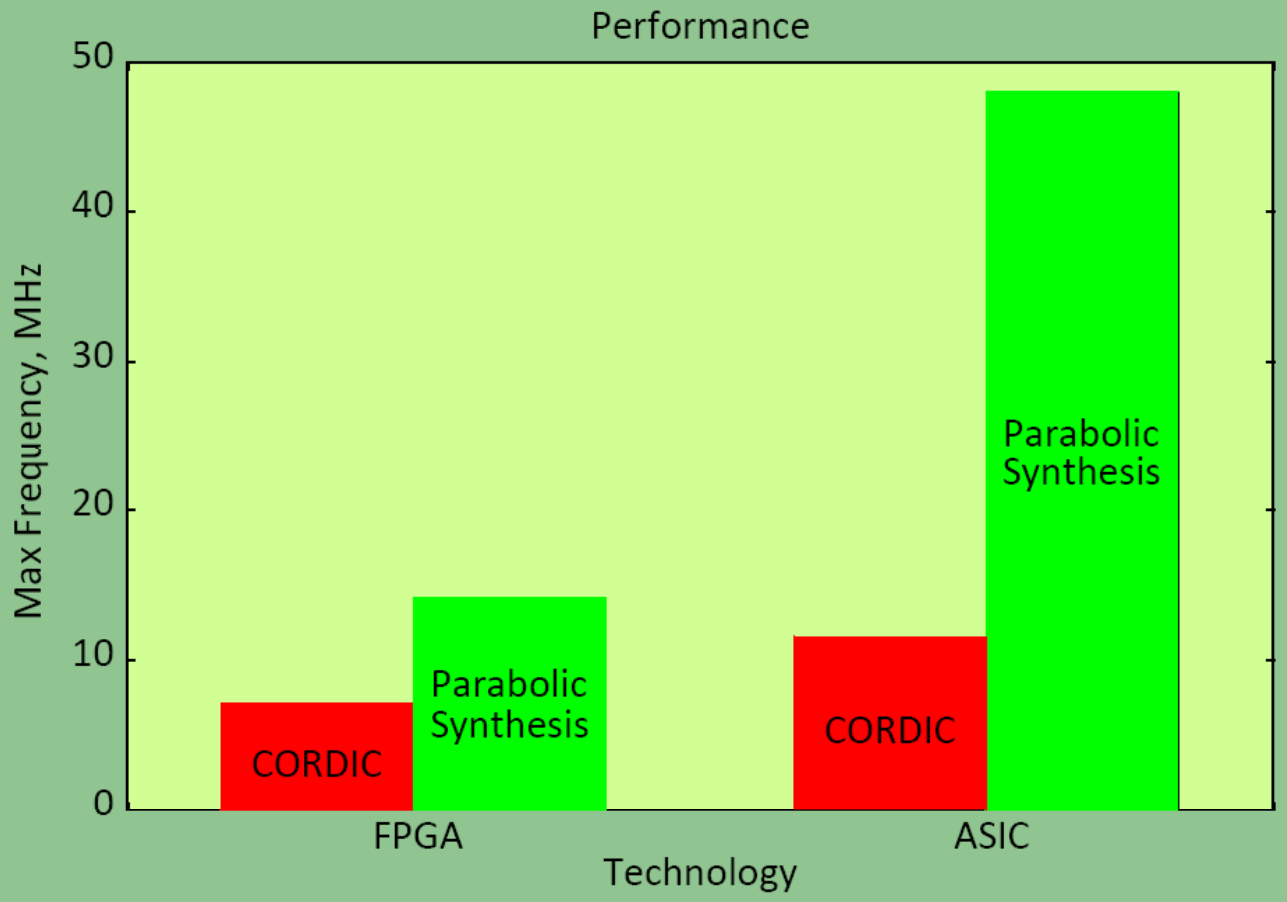
- Multiple FPGA´s for highly parallel processing is channels is required.
- Suitability of CAL data-flow language is evaluated in an initial case study.



Comparing Parabolic Synthesis with CORDIC

Erik Hertz and Peter Nilsson

Approximation of the logarithmic function with 15 bits accuracy



Synthesis Strategies in the Sub-V_T Region

Oskar Andersson*, S. M. Yasser Sherazi*, and Joachim Rodrigues*
Pascal Meinerhagen°, and Andreas Burg°

Design space exploration

Sub-V_T sign-off verification

Switching activity and energy minimum voltage

LUNDS UNIVERSITET
Lunds Tekniska Högskola

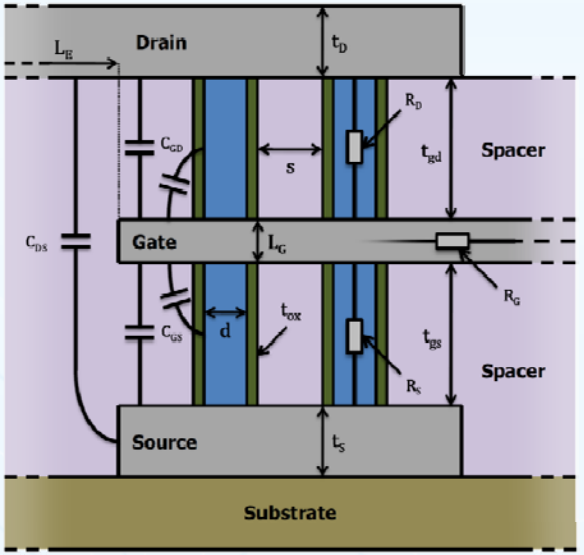
*Department of Electrical and Information Technology, Lund University, Sweden
°Institute of Electrical Engineering, EPFL, Switzerland

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Modelling of III-V Nanowire Transistors and Circuits

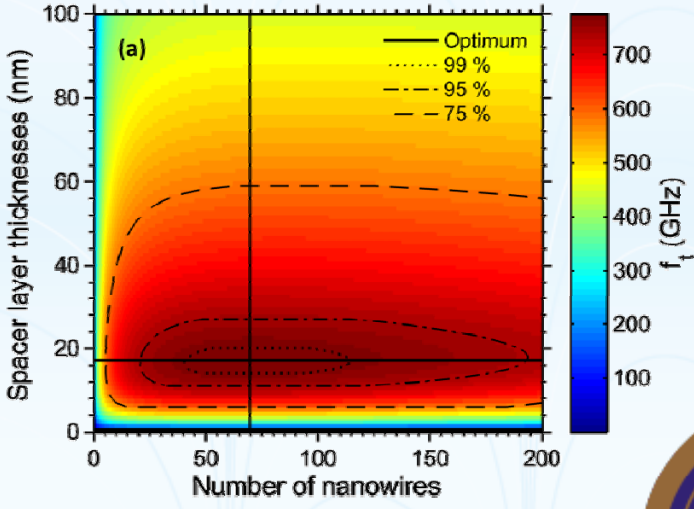
Goals

- Modelling of III-V nanowire transistors
- Evaluation of demonstrator circuits



Results

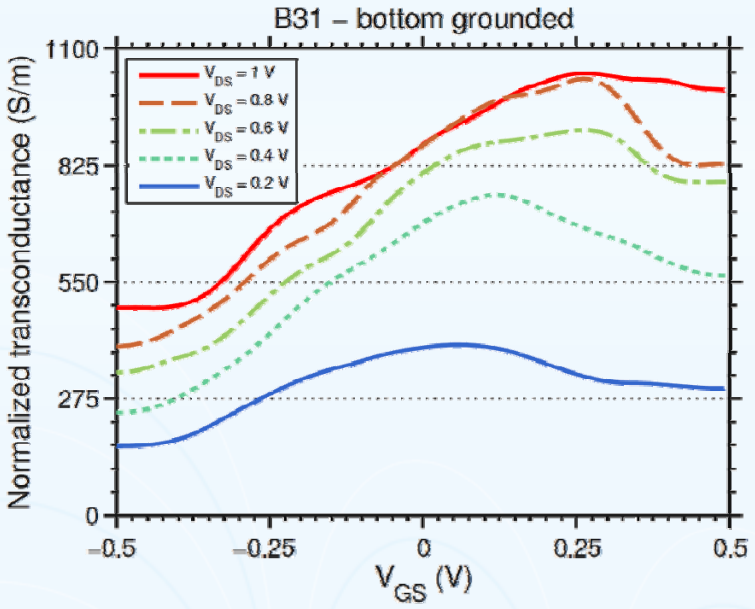
- Predictions of transistor and circuit performance
- Optimized nanowire transistor architecture



Nanowire transistors for RF implementation

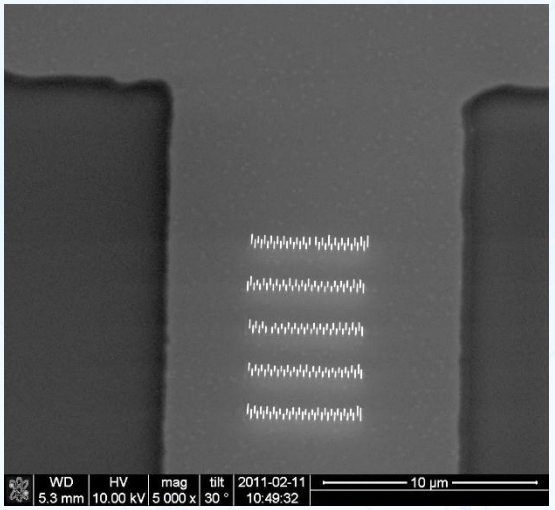
Goals

- Fabrication of III-V nanowire transistors on silicon
- Development of LNA using nanowire transistors



Results

- Successful integration of InAs nanowires on silicon
- High performance FETs with a g_m of above 1 S/mm



15 nm InAs Nanowire MOSFETs

Goal

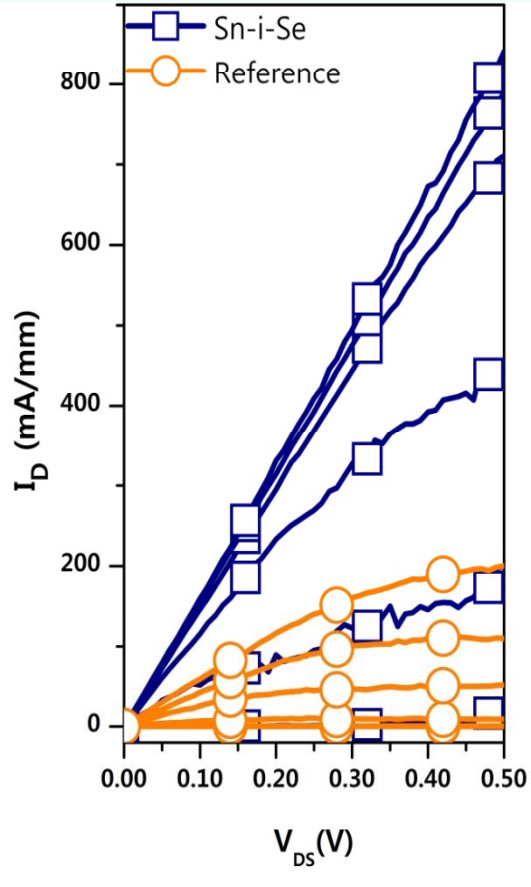
- Evaluate the scaling properties of InAs nanowires

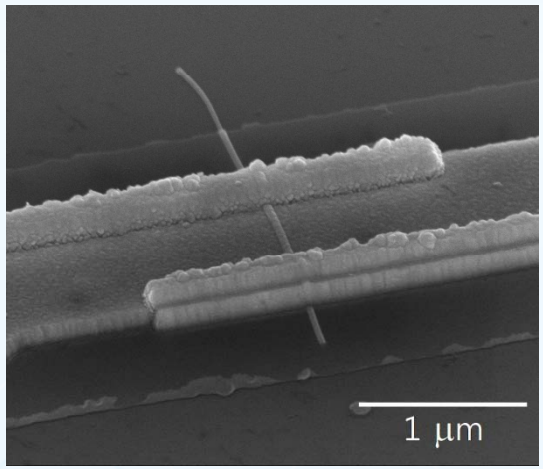
Results

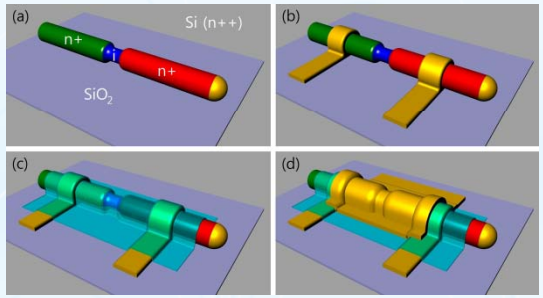
- J_{ON} = 33 MA/cm^2

(Comparable to modern HEMTs)

- g_m = 1.8 S/mm







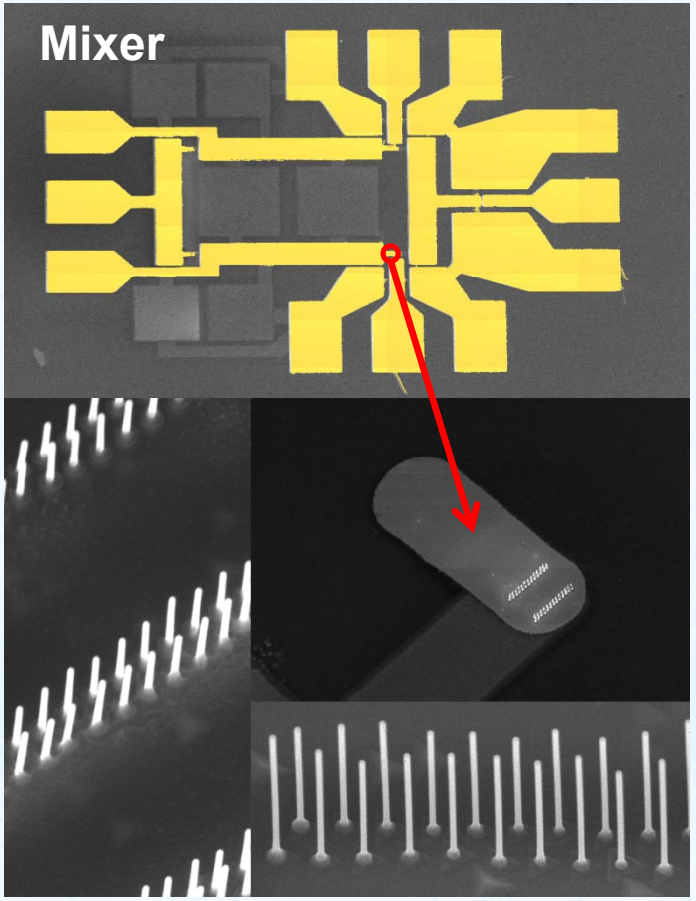
InAs Nanowire Mixer Circuit Integration

Goal

- Integration of InAs NW single balanced differential mixer circuit
- Demonstrating performance advantageous compared to similar Si technology

Results

- Single and Array Vertical NW Transistor Performance
  - **g_m - 1 S/mm**
  - **f_t - 20 GHz**
  - **f_{max} - 30 GHz**



Heterostructure nanowires for infrared photodetectors

Goals

- Fabricate InAs/InAsSb/GaSb p-i-n nanowires for photodetection up to 12 µm.
- Obtain better detectivity than planar devices due to low defect concentration as heterojunctions.

Results

- Photocurrent of a few hundred nA at 78K.
- Valence band offset between InAsSb and GaSb measured to be around 30 meV.