Digital Circuit Design in Weak-Inversion/Subthreshold

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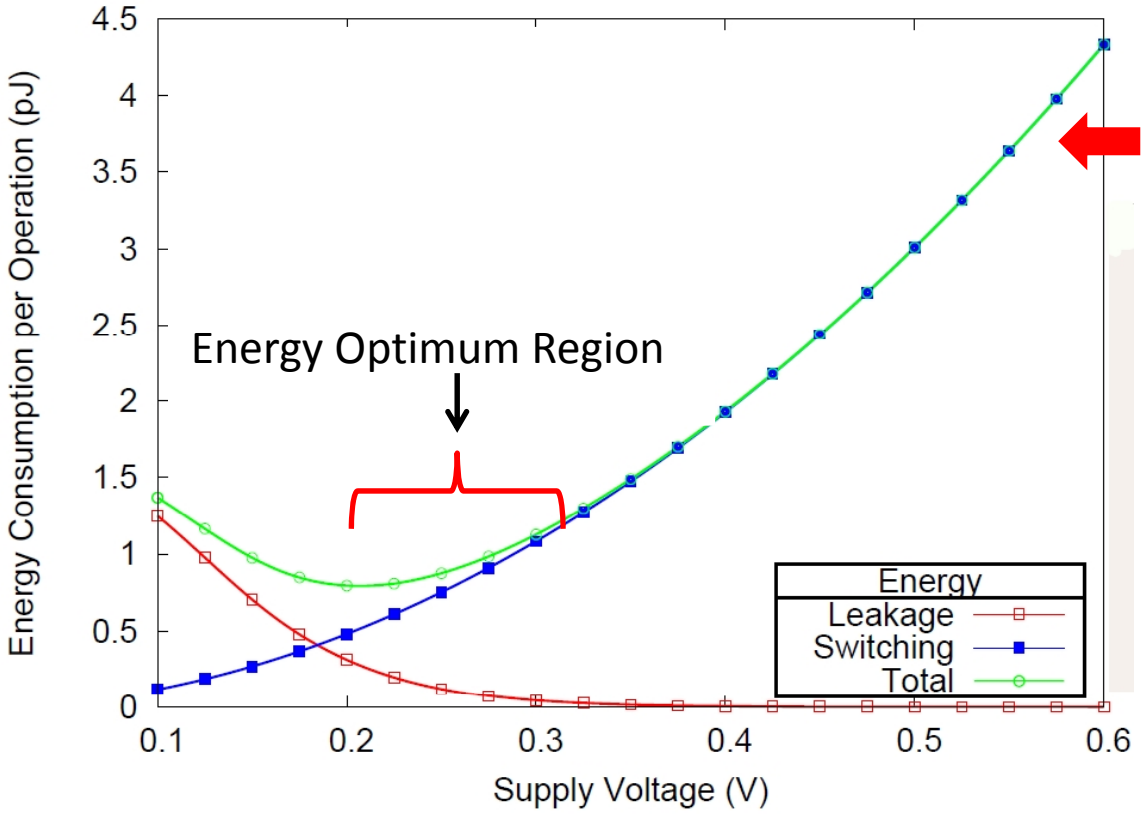
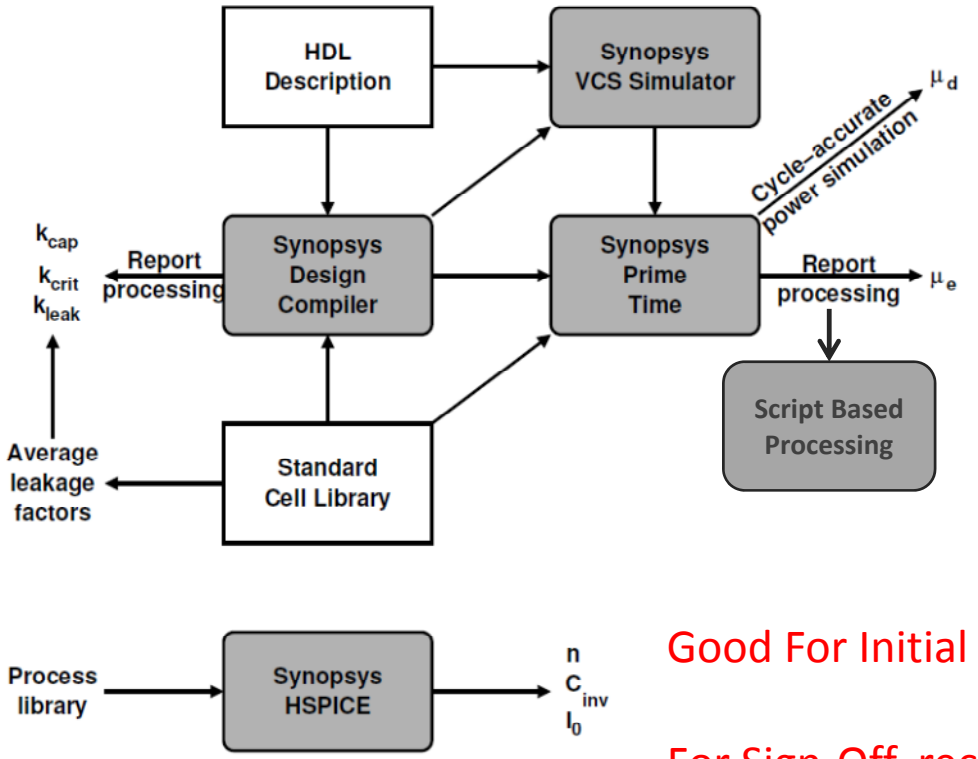
Motivation and Sub-V_T Basics



- **This is theory**
- **How about**
  - Charaterization?
  - Architectural flavors?
  - Throughput?
  - Technology options?
  - Process variations?
  - Switching acitivity?
  - Proper STA?

- Energy minimum operating voltage (EMV) in sub-V_T.
- Circuit operates at critical path speed, idle time is minimized.
- Delay increases exponentially.

High-level Modeling in the Sub-V_T Domain [1]



- No standard/commercial flow available which simply characterizes designs with $V_{DD} \leq 400$ mV.
- High-level Energy Model
  - Conventional EDA tools.
  - SPICE-accurate in a fraction of SPICE simulation time.
  - Any RTL design.
  - Standard- and full-custom based designs.

Good For Initial Charaterization

For Sign-Off, recharaterized Sub-V_T lib flow is used to get better timing information [2]

[1] O. Akgun, J. Rodrigues, Y. Leblebici, and V. Owall, "High-level energy estimation in the sub-V_T domain: Simulation and measurement of a cardiac event detector," *in IEEE TBIOCAS*.
[2] Pascal Meinerzhagen, Oskar Andersson, Yasser Sherazi, Andreas Burg, and Joachim Rodrigues, " Synthesis Strategies for Sub-V_T Systems" *ECCTD 2011.*

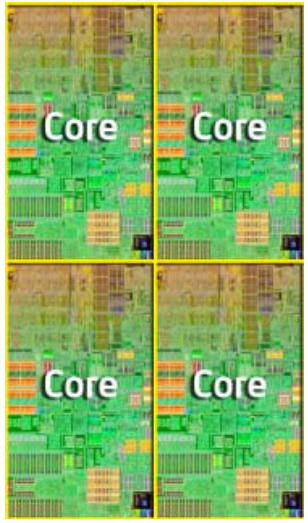
Energy Model Application

- Decimation Filter Chain [4,5]
  - Requirements
    - Minimum energy per sample operation.
    - Decimate data from 8-Msamples/s to 0.25-Msamples/s.
  - Questions:
    - Optimal operational voltages.
    - Architectures that provide sufficient throughputs need to be developed.
    - Selection of cells based on threshold options in 65-nm.

- Various architectures of a half band digital filter (HBD) are implemented:
  - Parallelized by 2,4, and 8.

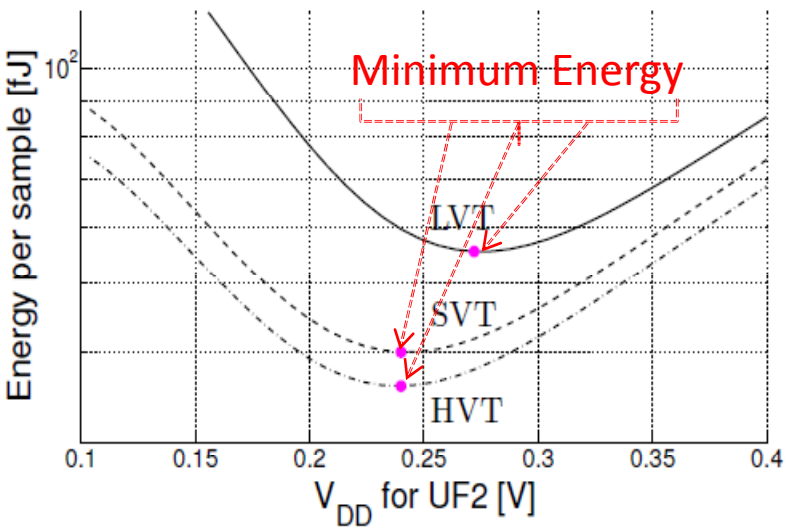
Original

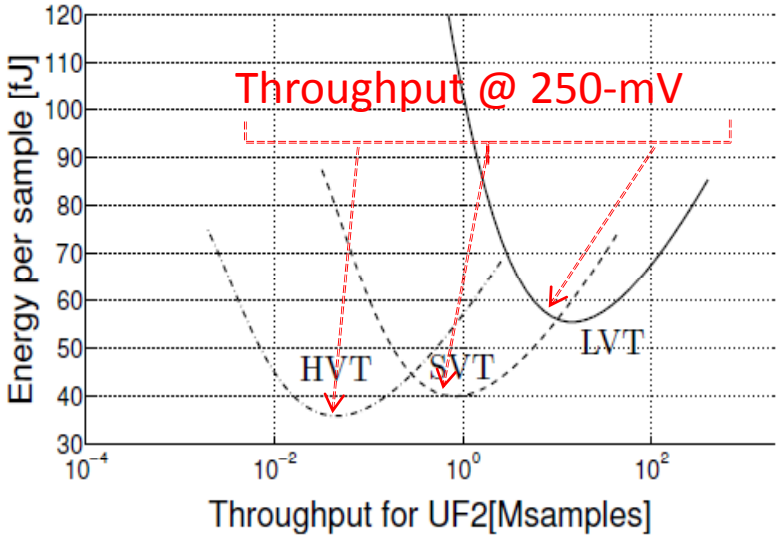
Parallelized by 4



[4] S. Sherazi, J. Rodrigues, O. Akgun, H. Sjöland, and P. Nilsson, "Ultra low power sub-V_T decimation filter chain," *Norchip, 2010*.
[5] S. Sherazi, P. Nilsson, O. Akgun, H. Sjöland, and J. Rodrigues, "Design exploration of a 65 nm sub-V_T CMOS digital decimation filter chain," *ISCAS, 2011*.

Energy-Throughput Analysis w.r.t. different V_T's



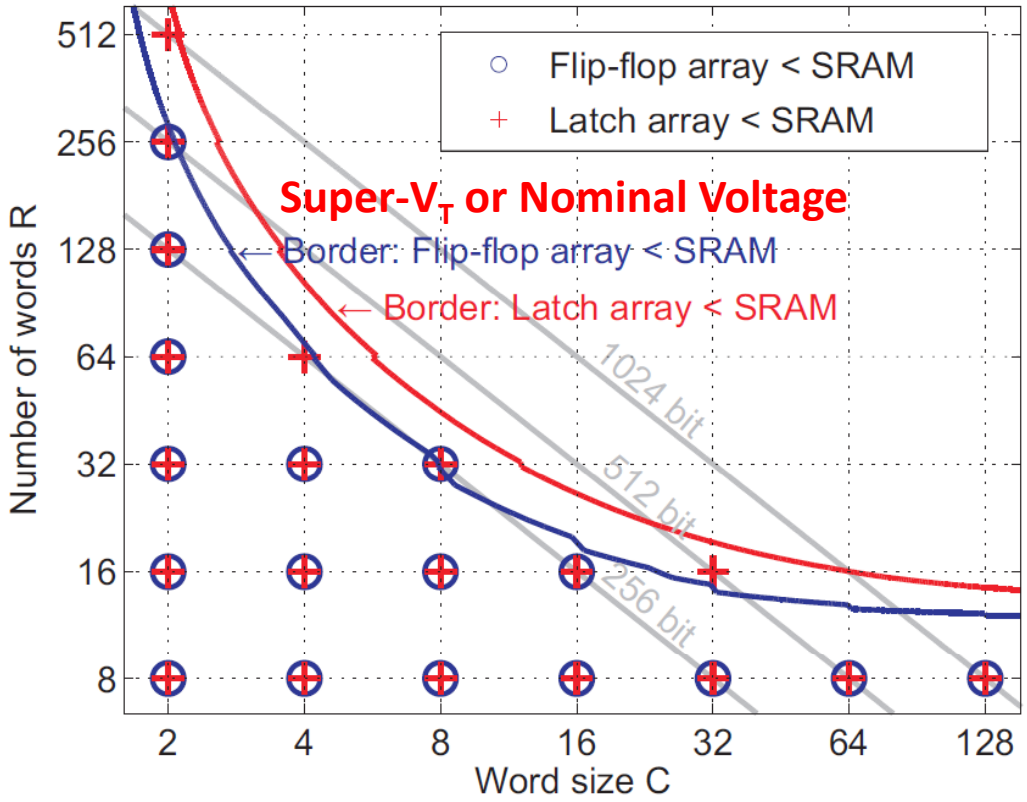


- Energy vs V_{DD}.
  - HVT cells have least energy dissipation.

- Energy vs Throughput.
  - SVT cells have least energy dissipation for moderate throughput requirments.

HVT = High V_T Cells
SVT = Standard V_T Cells
LVT = Low V_T Cells

Standard-Cell-Based Memory [6]



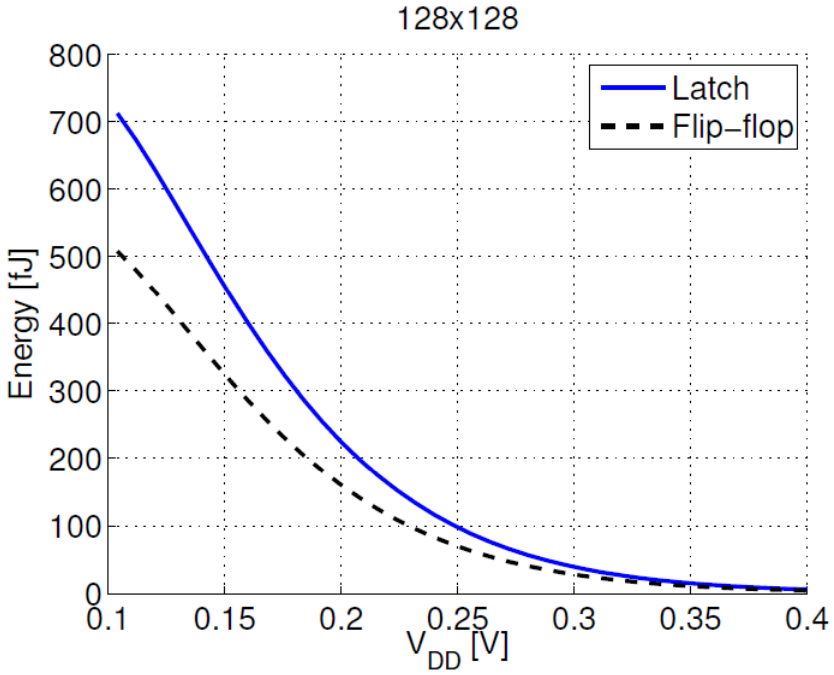
- SRAM macro-cells become significantly larger due to the need for 8 T or 10 T [7] bit-cells
- Additional assist circuits required for reliable sub-V_T operation (sense-amplifier).

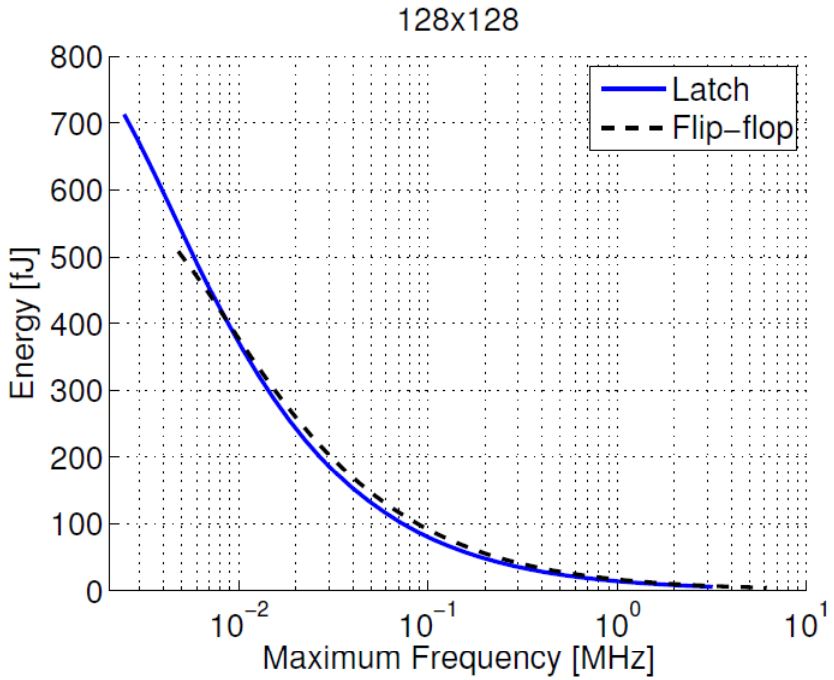
- Latch arrays are smaller than SRAM macro-cells for storage capacities of up to around 1 kbit.

[6] N. Verma and A. Chandrakasan, "A 65nm 8-10T sub-V_T SRAM employing sense-amplifier redundancy," in *Proc. IEEE ISSCC, Feb. 2007.*

[7] P. Meinerzhagen, S. M. Y. Sherazi, A. Burg, and J. N. Rodrigues, "Benchmarking of standard-cell based memories in the sub-V_T domain in 65-nm CMOS technology," *IEEE Journal on JETCAS*, 2011.

Standard Cell Based Memories (SCM) [7]

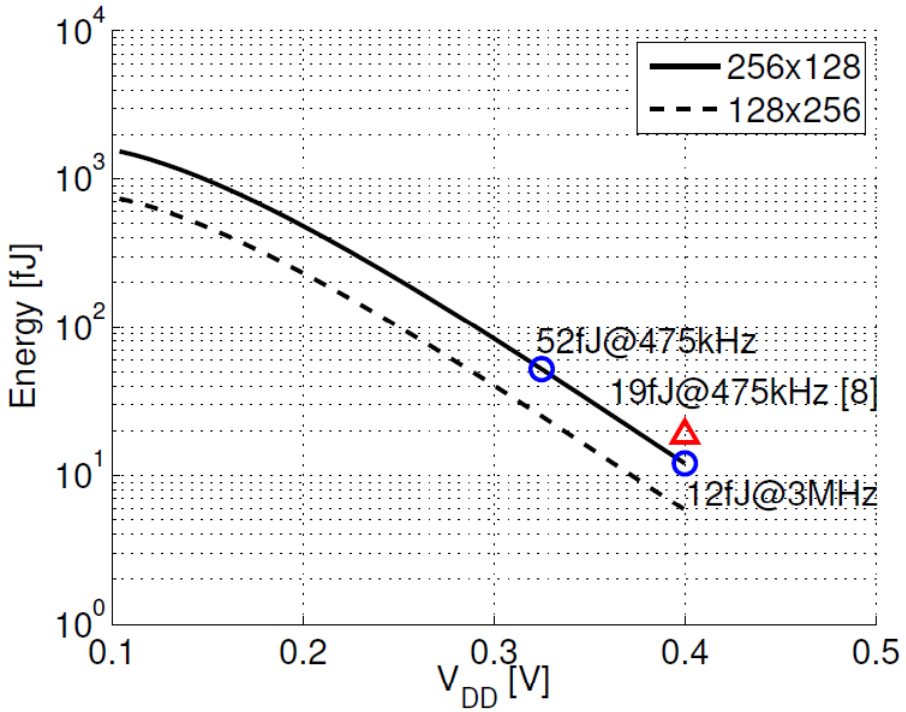


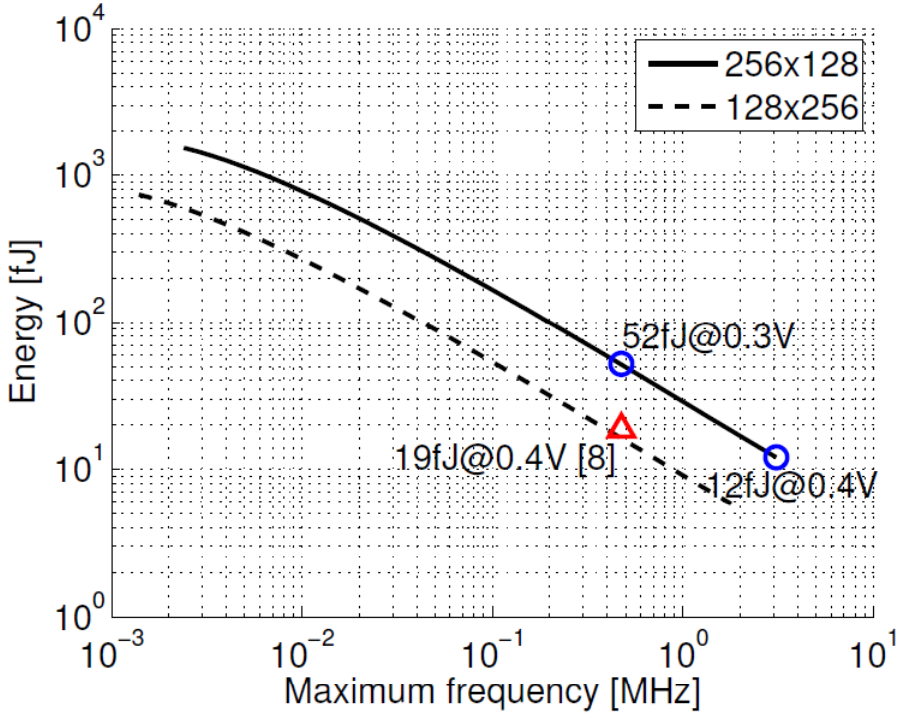


- Energy vs Voltage
  - Flip-Flop based implementation are a bit faster.

[7] P. Meinerzhagen, S. M. Y. Sherazi, A. Burg, and J. N. Rodrigues, "Benchmarking of standard-cell based memories in the sub-V_T domain in 65-nm cmos technology," *IEEE Journal on JETCAS*, 2011.

Energy Analysis of SCMs





- Energy vs Voltage
  - Latch based multiplexer clock-gate architecture for R = 256, C = 128 and for R = 128, C = 256. The **Δ** corresponds to **[8]**, a hard macro SRAM memory.

[8] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm subthreshold SRAM design for ultra-low-voltage operation," *in IEEE J. of Solid-State Circuits, 2007*.

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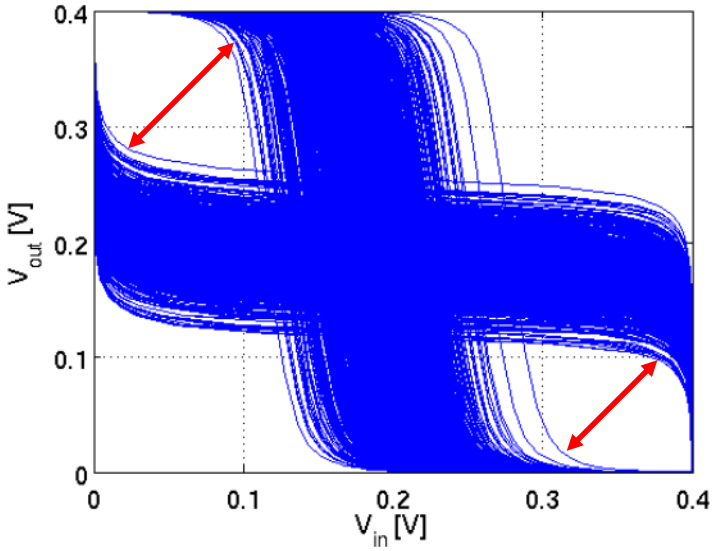
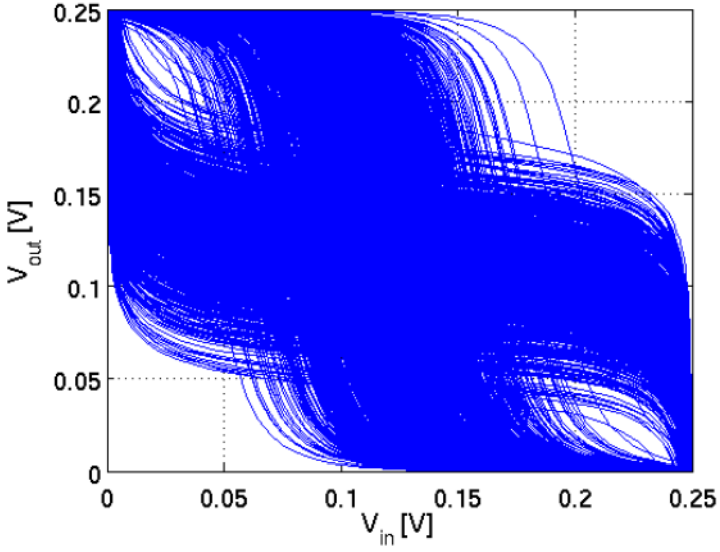
Reliability Analysis





- Eye diagram of the latch used in the SCM architecture for V_{DD}=0.4V and V_{DD}=0.25V.
- 1000-point Monte Carlo circuit simulation assuming within die process parameter variations.
- Operation is still possible below V_T, but the SNMs are small and reliability starts to become critical at 250mV.

Conclusions

- A high-level energy flow for sub-V_T domain characterization was presented.
  - Enables architectural design space exploration.
- SCM are promising option for sub-V_T memories.
- Proper knowledge of input stimuli is crucial for system specification.
- Scientific outcome
  - 3(+1) Journals published,
  - 6(+1) Conference papers published, 1 Invited.

Work done in close collaboration with EPFL.

This presentation is an excerpt of a keynote that will be held at PATMOS 2011 (Joachim N. Rodrigues).

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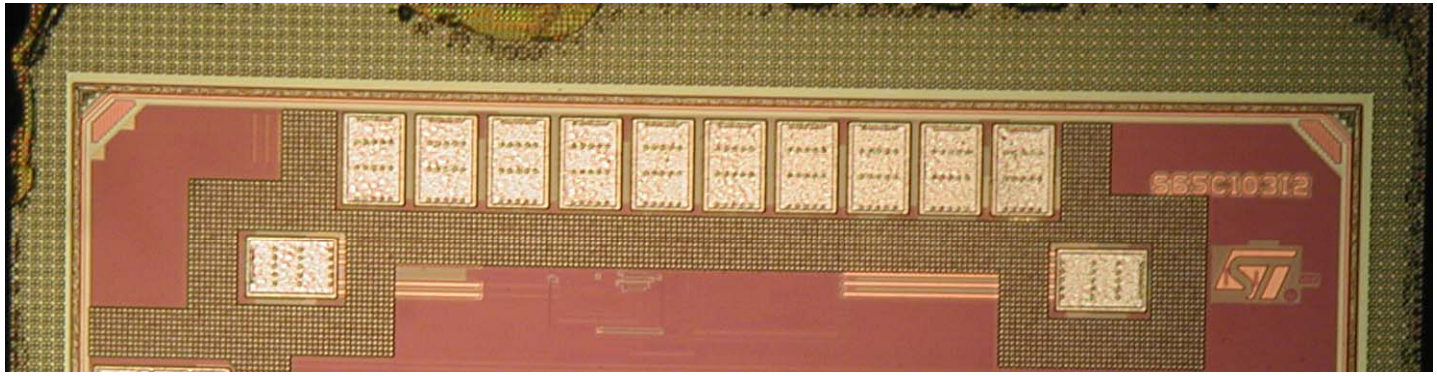
Thank You...

... to our sponsors SSF and VINNOVA

... colleagues at EPFL



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