Low Power III-V MOSFETs

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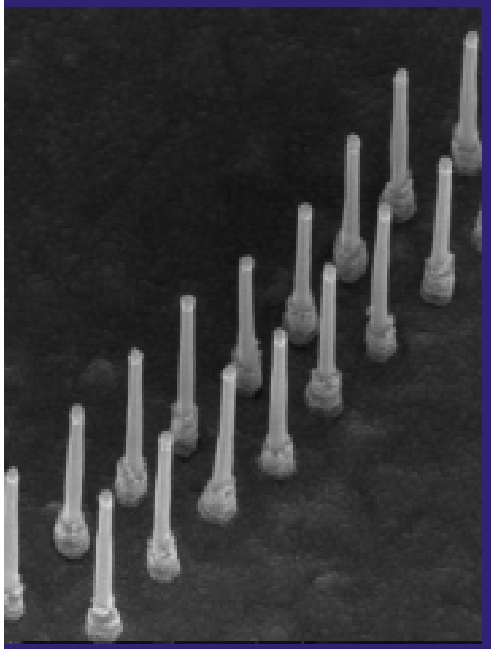
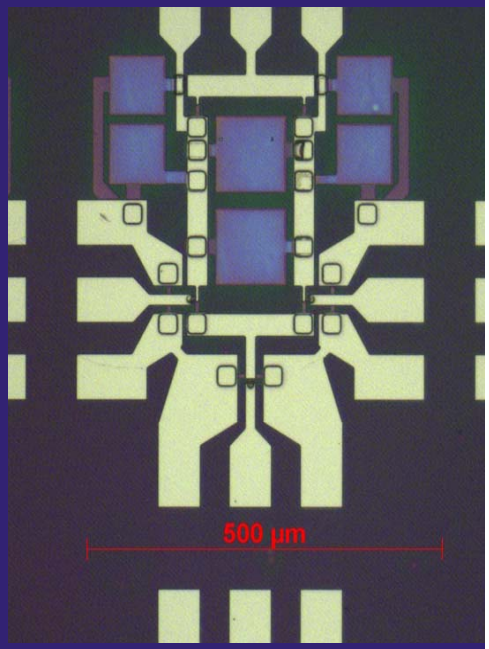
WWW: Wireless with Wires

InAs Nanowires

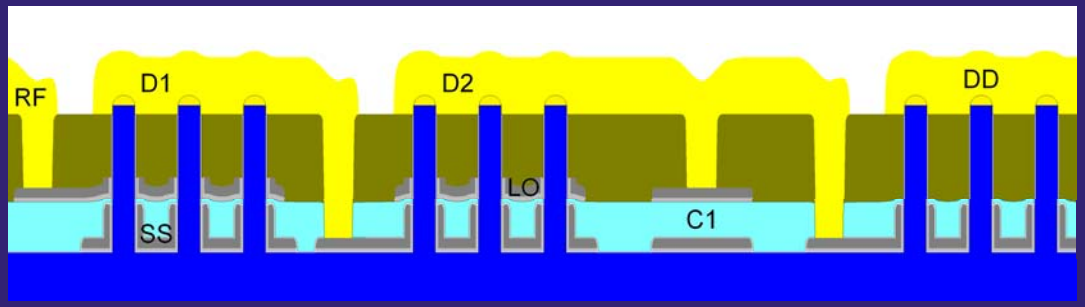


- High-speed digital and RF-circuits based on nanowire transistors
- Wrap-gates used to scale towards 10 nm L_g
- Optimize materials and device concepts
- How much do we gain by increasing g_m at low drive voltages (V_{dd}=0.5 V)?
- Can we reduce some "key capacitances" in the vertical geometry?

Fabricated mixer



Schematic cross-section



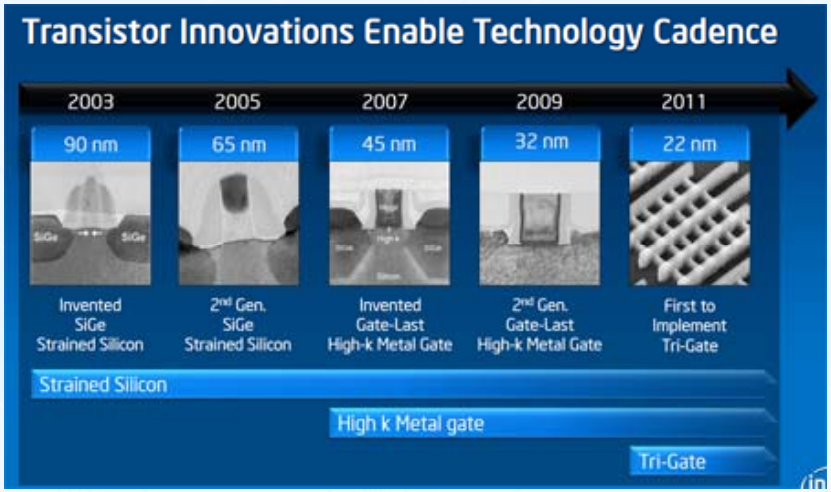
Current Trends in Device Scaling

Transport Enhancement

Graphene

III-Vs

Strained Si



Electrostatics

Planar Technologies

FinFets Trigates

Nanowires

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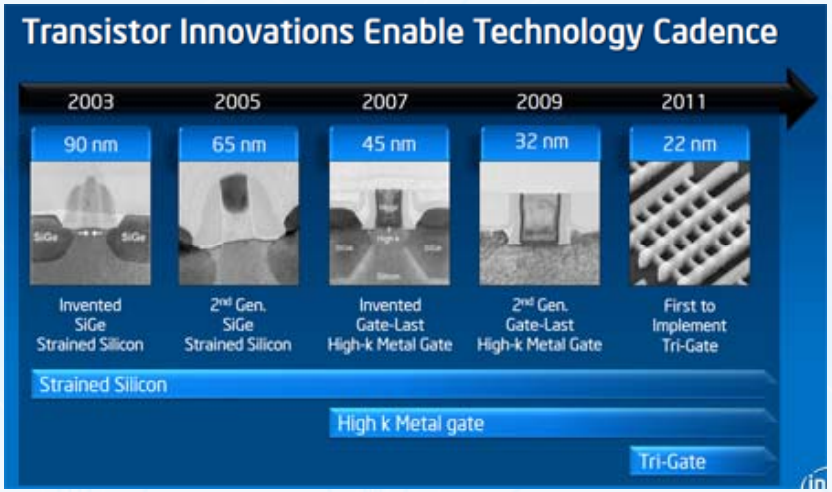

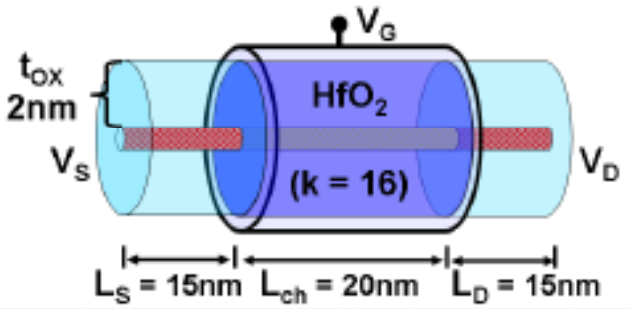

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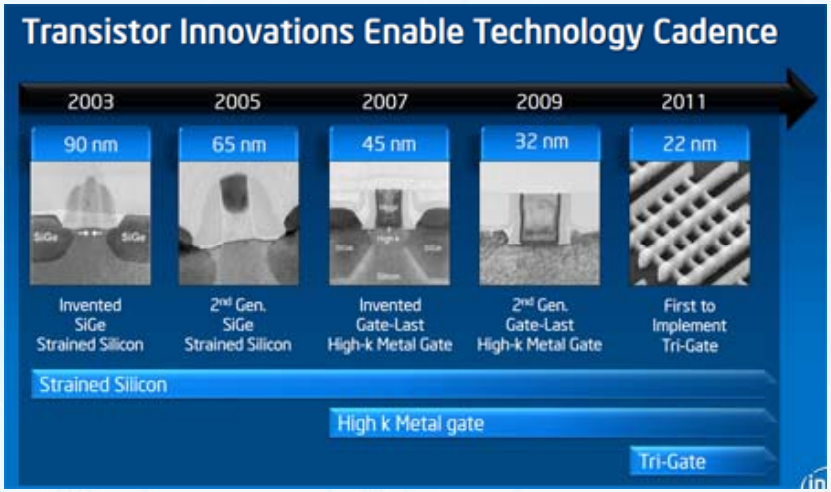

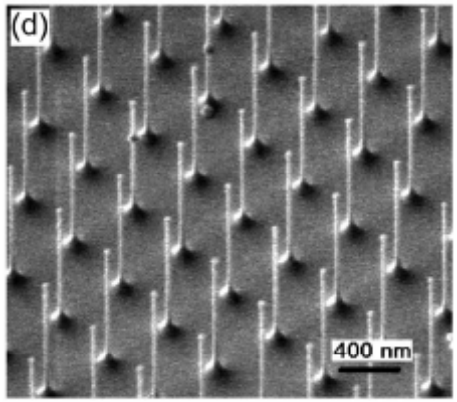

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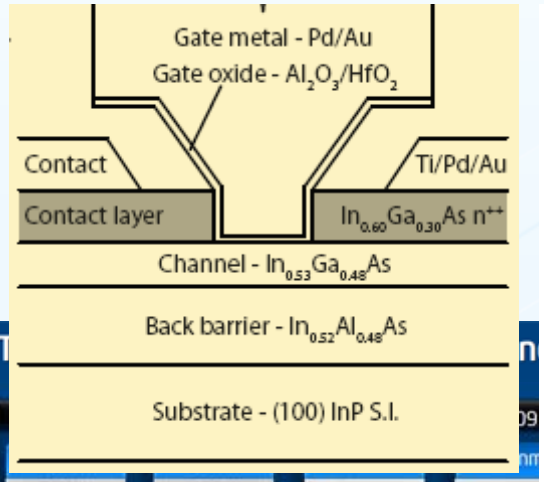

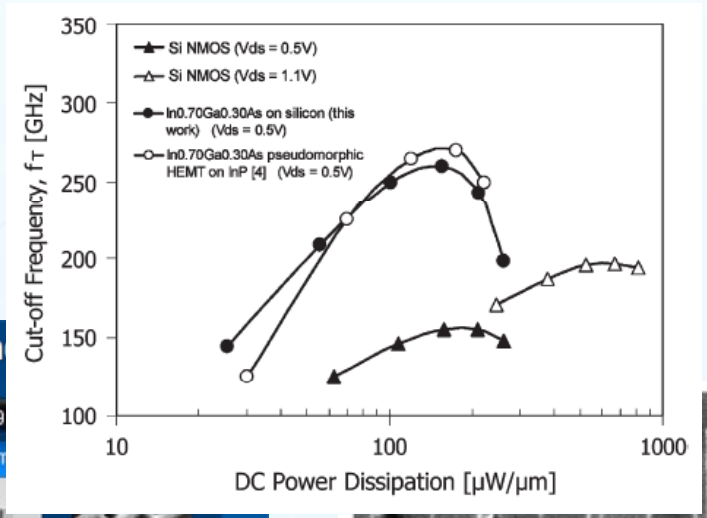

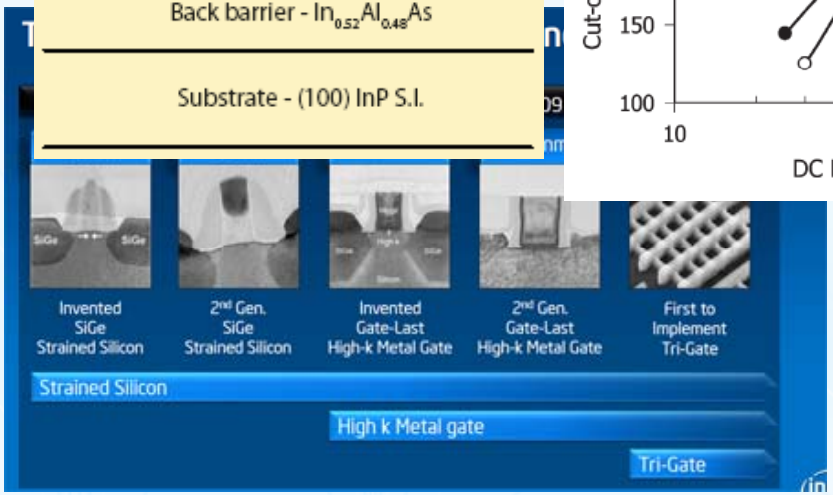

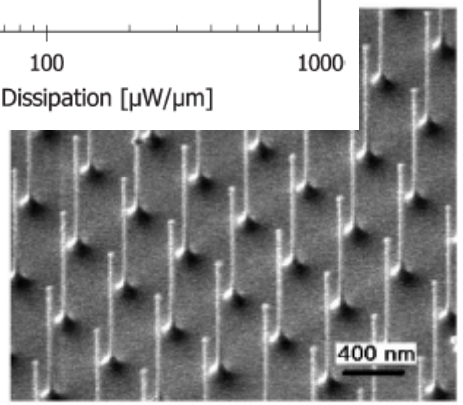

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Transport Enhancement

Graphene

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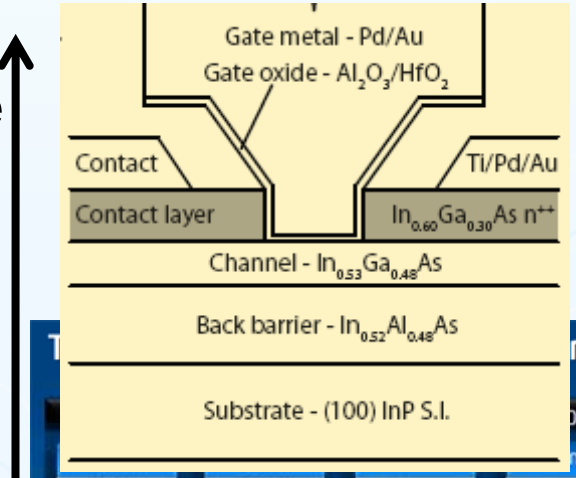

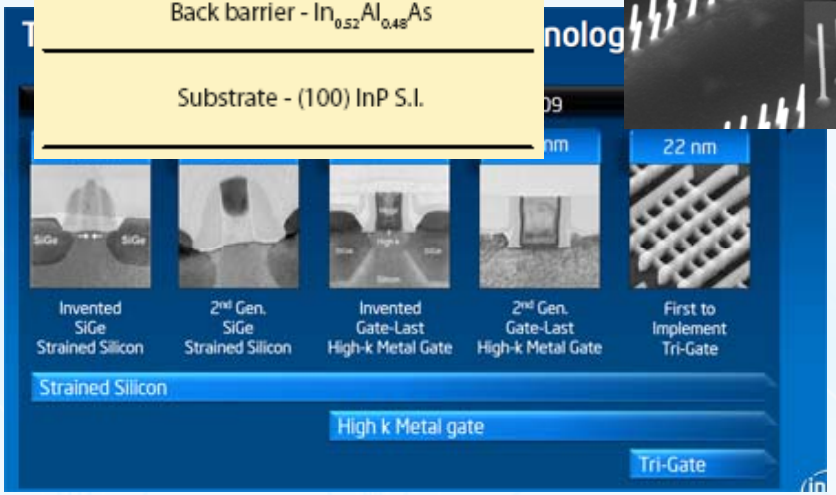

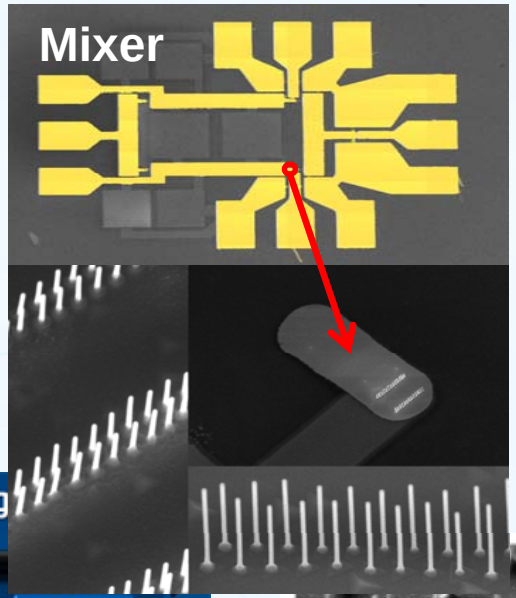

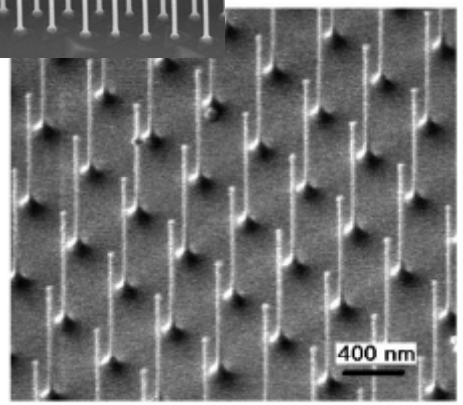

Electrostatics

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Nanowires

Current Trends in Device Scaling

Transport Enhancement

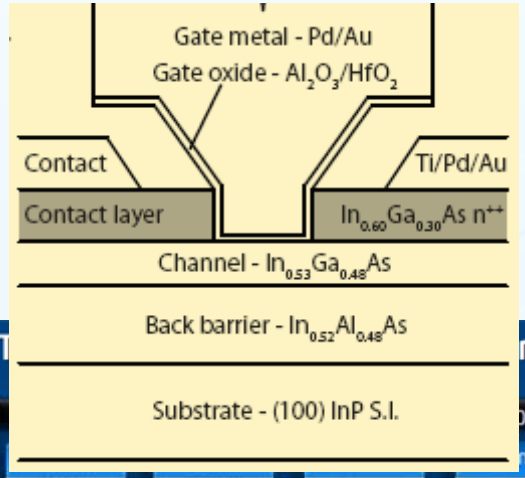
More than Moore

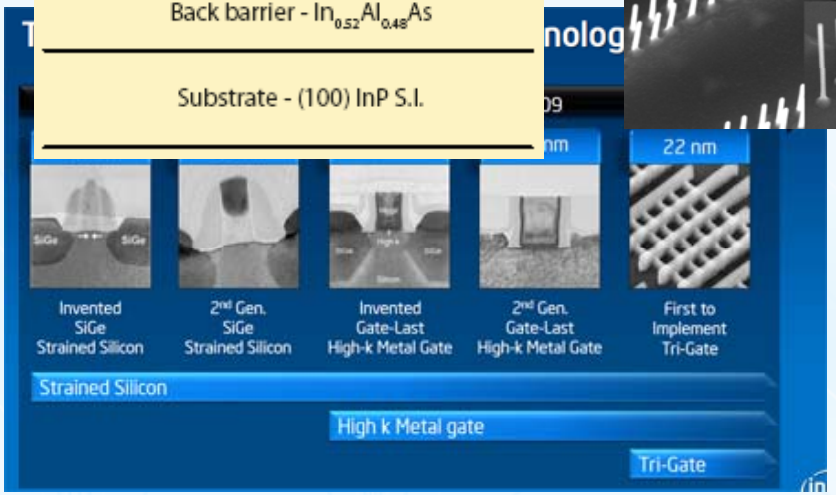
Beyond Moore

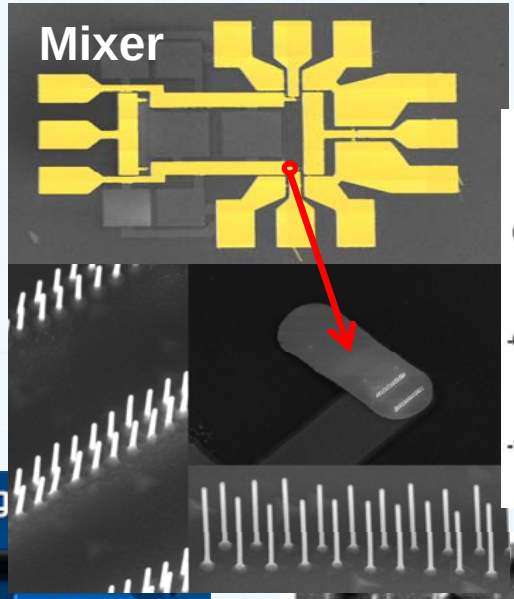
Graphene

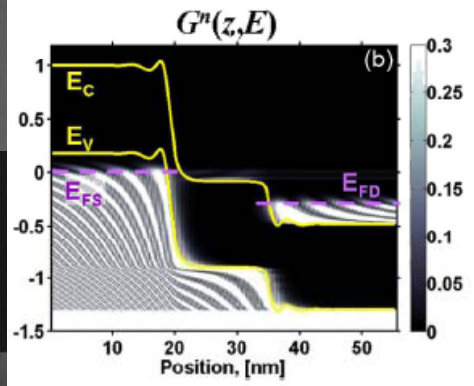
III-Vs

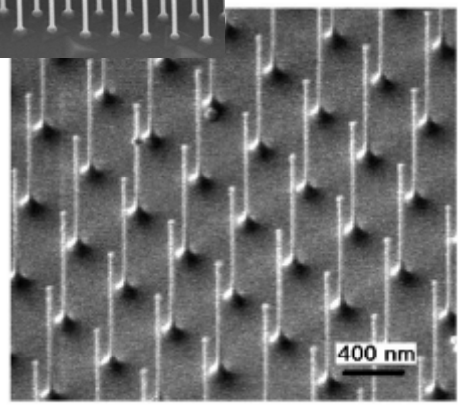
Strained Si











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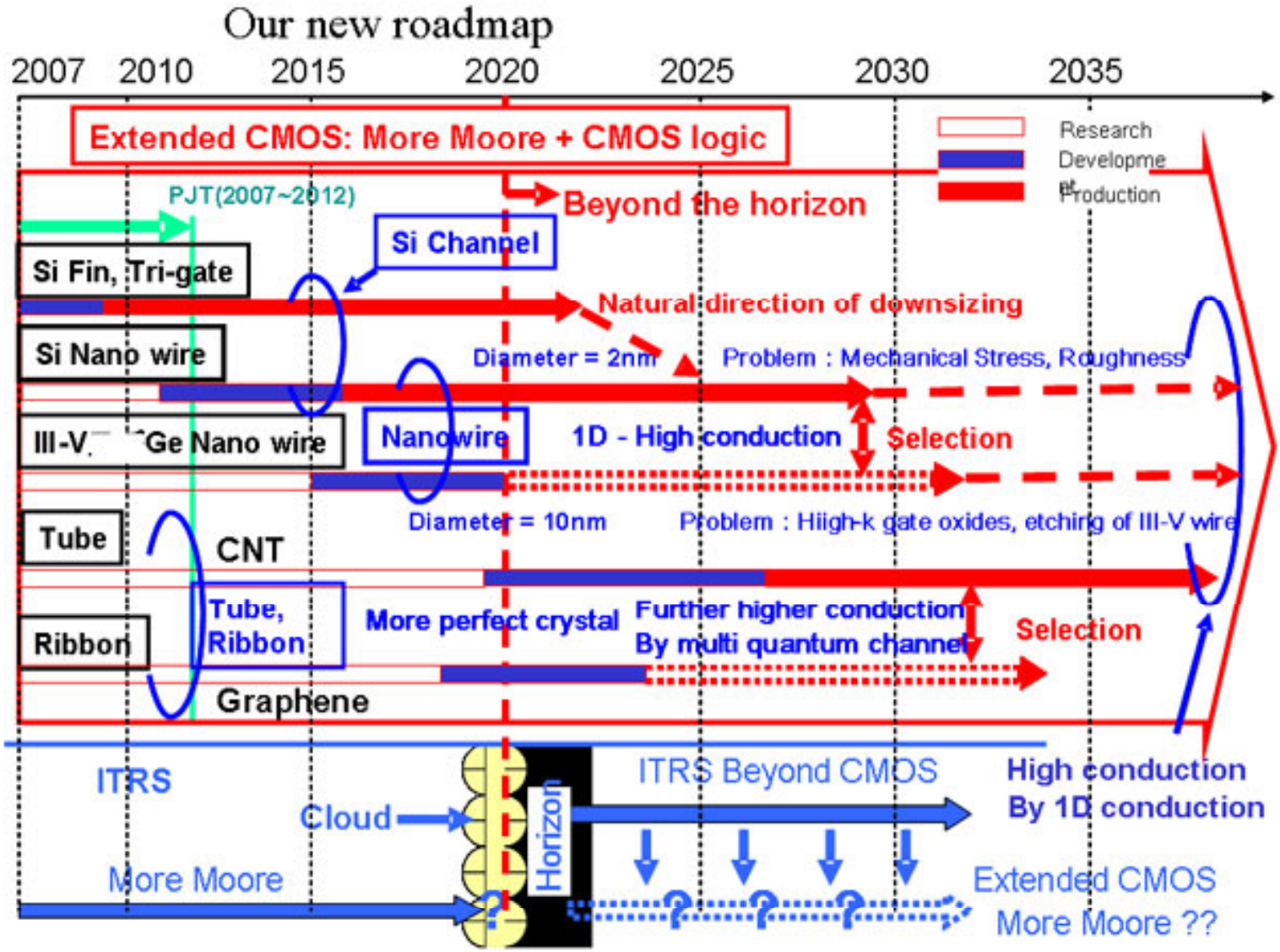


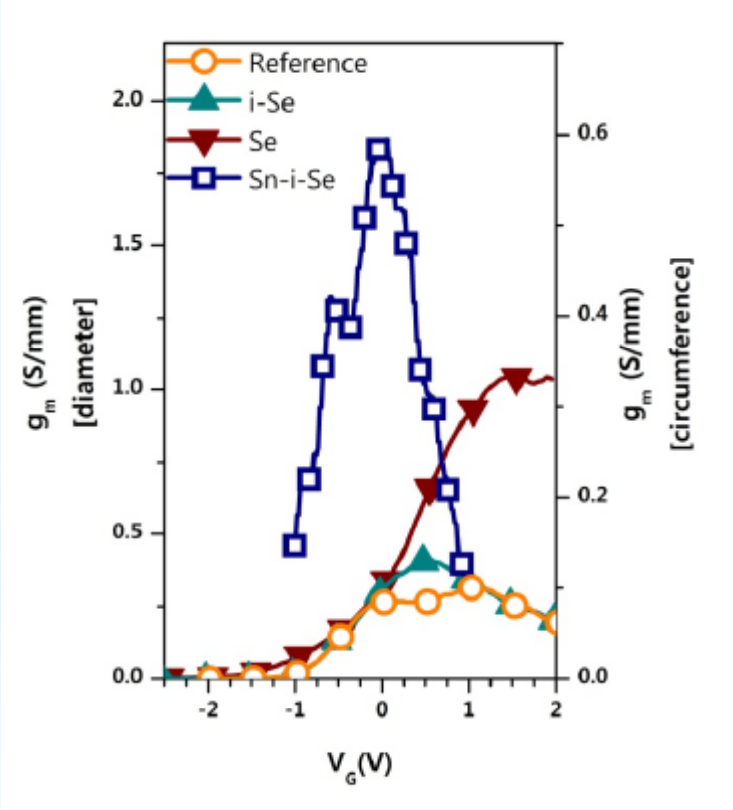
A roadmap from Japan's technical community sees silicon nanowires extending the reach of multi-gate devices.

H. Iwai (Tokyo Inst. of Techn.)

ISAGST, Sept. 25-28, 2007
Dallas, Texas, USA

Ultimate Transistor Performance

Transport in thin (15 nm) InAs NWs



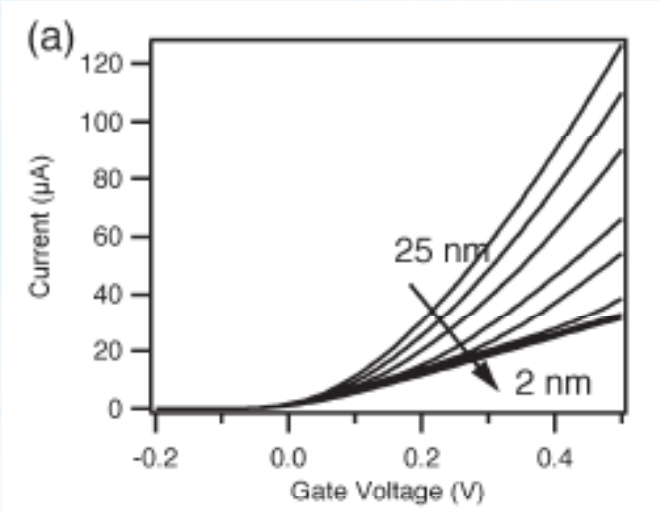
Lateral transistors 500 nm L_g

Doping essential to reduces access resistance

Max transconductance 1.8 S/mm

I_d=8300 kA/cm^2 or 600 mA/mm

Best g_m/g_o=10.4



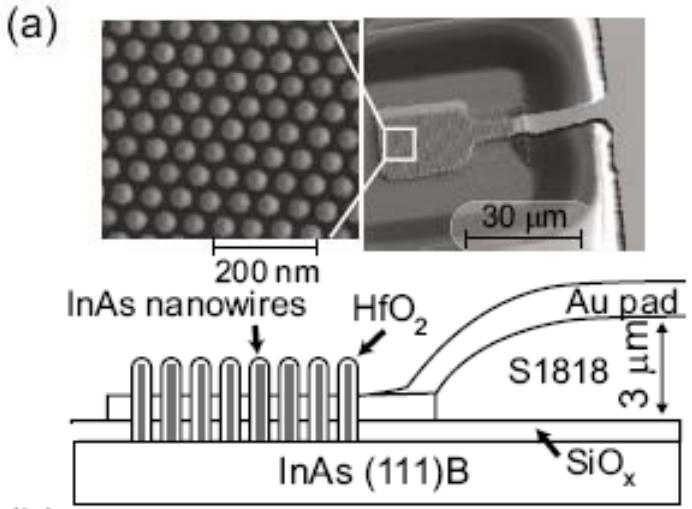
Simulated data (tight binding)

I_{on} =120 μA

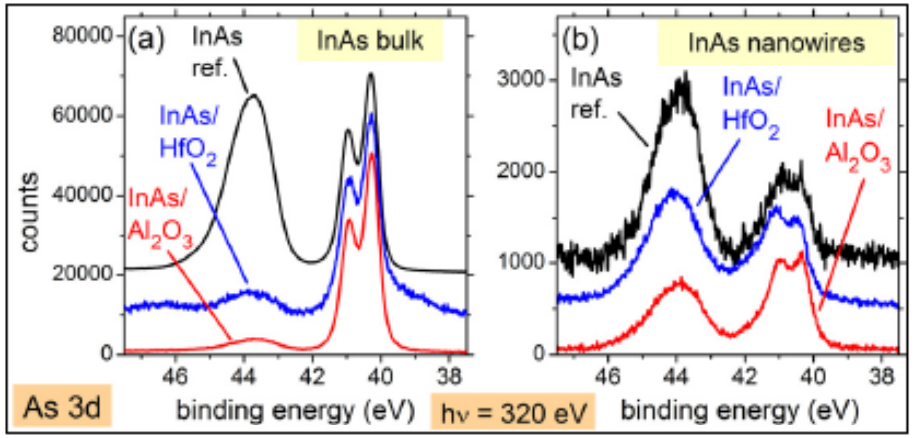
$I_{on,exp}$ =30 μA

High-κ on III-V Nanowires

InAs/HfO2 nanowire capacitors



XPS on InAs nanowires



Nanowire capacitors behave like planar InAs capacitors

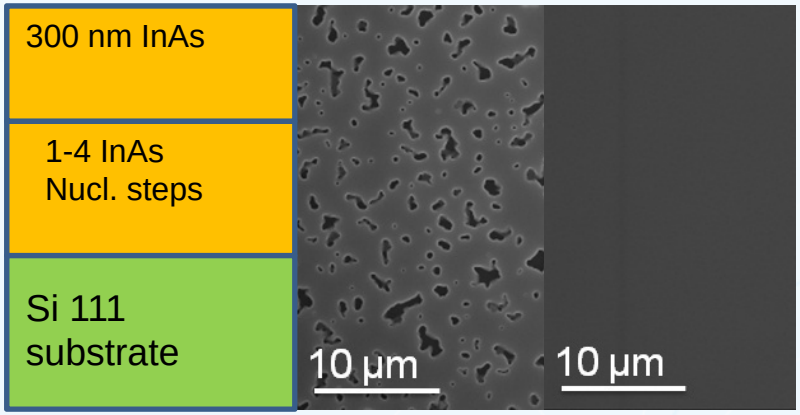
Temperature and frequency dependence

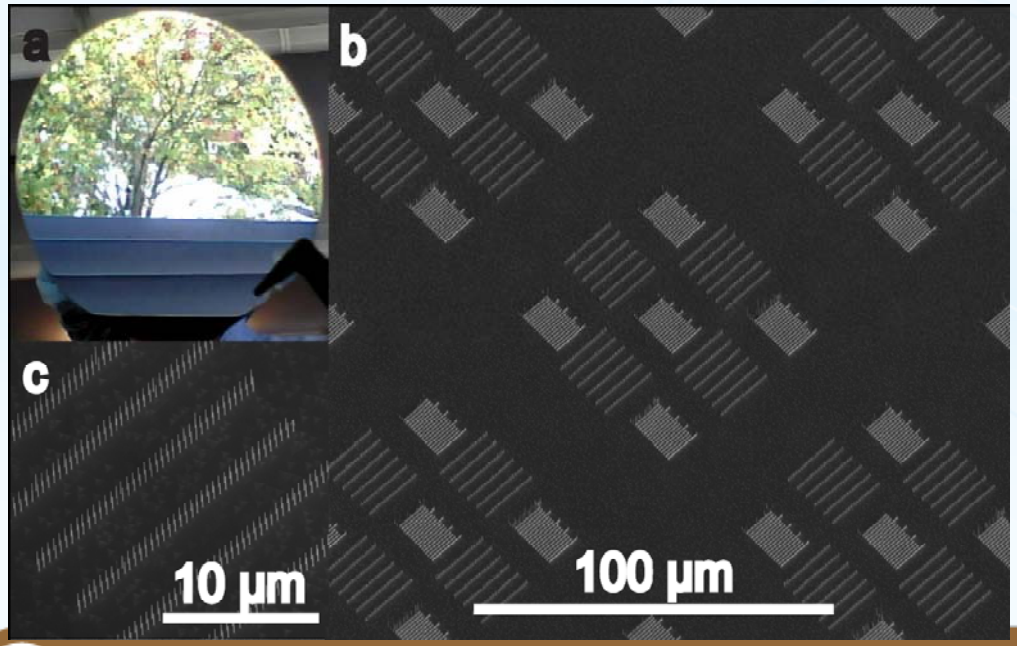
Holes may play a role due to narrow gap

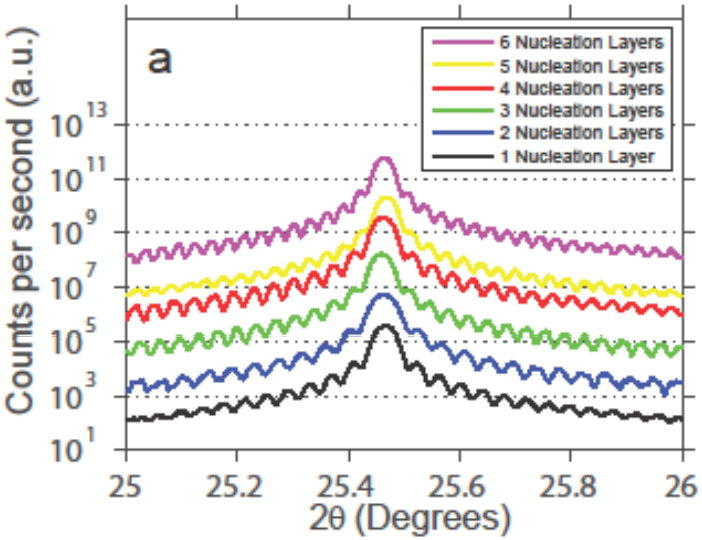
Less effective oxide reduction

InAs RF-transistors on 2” Si

Effect of InAs nucleation layer



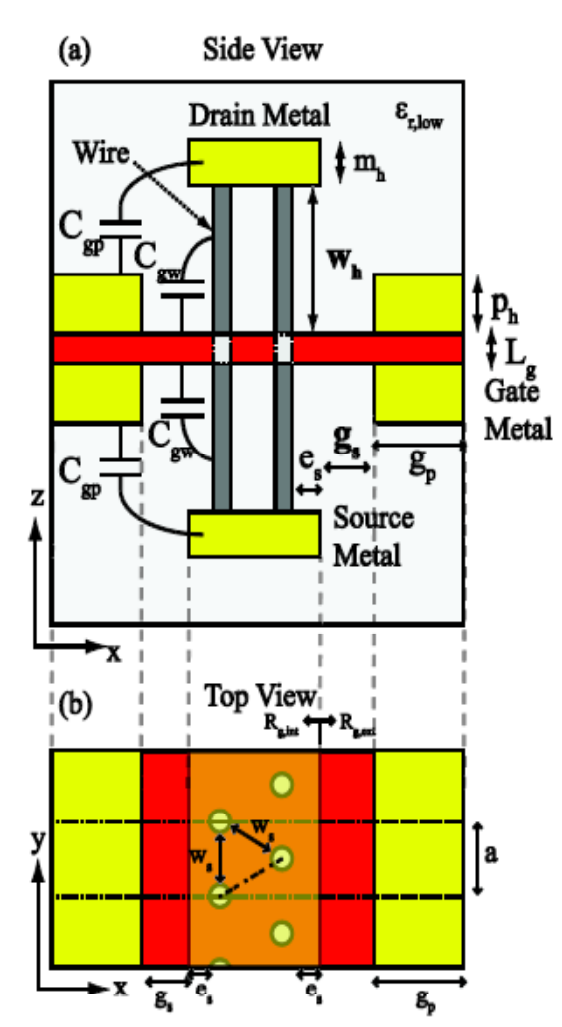


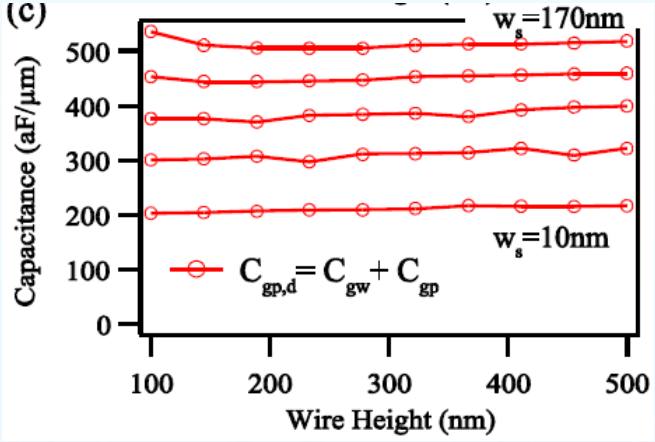


Buffer layer technology
used for InAs layers on Si
4-6 nucleation layers
Wafer patterning
Uniform nanowire growth

Strategy to Reduce Capacitances

Close packing of nanowires to screen the electric fields





Internal capacitance low in the quantum limit, also including parasitics advantages are found

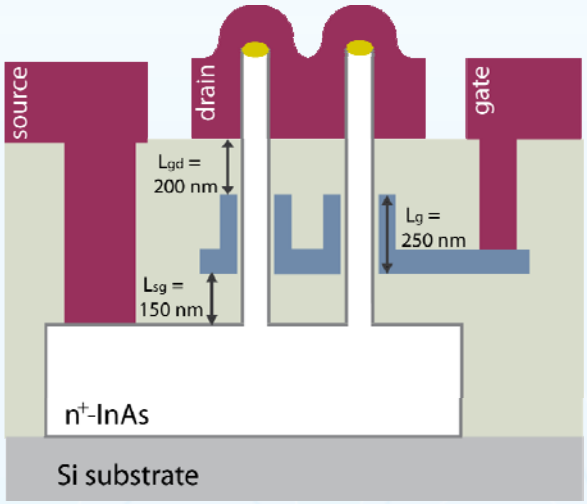
TABLE I
BENCHMARKING OF PARASITIC CAPACITANCES

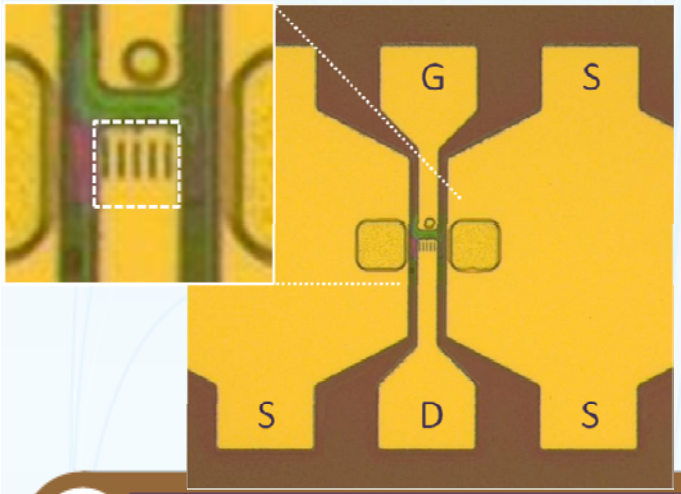
(aF/μm)		f_t-design		f_{max}-design[a]		ITRS[b]	
Node	L_g	$C_{gg,i}$	$C_{gg,t}$	$C_{gg,i}$	$C_{gg,t}$	$C_{gg,i}$	$C_{gg,t}$
35 nm	47.1 nm	364	611	364	741	766	967
22 nm	29.6 nm	285	514	285	655	739	980
16 nm	21.5 nm	235	511	235	617	675	888
12 nm	16.1 nm	218	449	218	590	501	716
8 nm	11.1 nm	127	403	127	509	378	562

[a] f_{max}-optimized design with double gate electrode.
[b] Interpolated data from the ITRS roadmap.

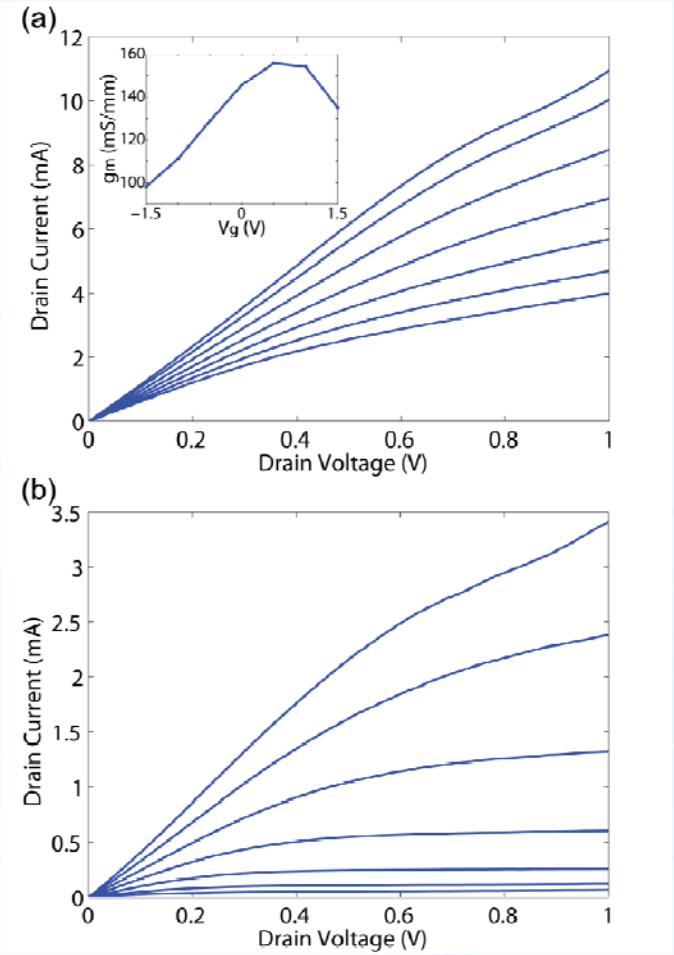
InAs RF-transistors on 2” Si

Device layout with W gate





182 nanowires, 35 nm diameter

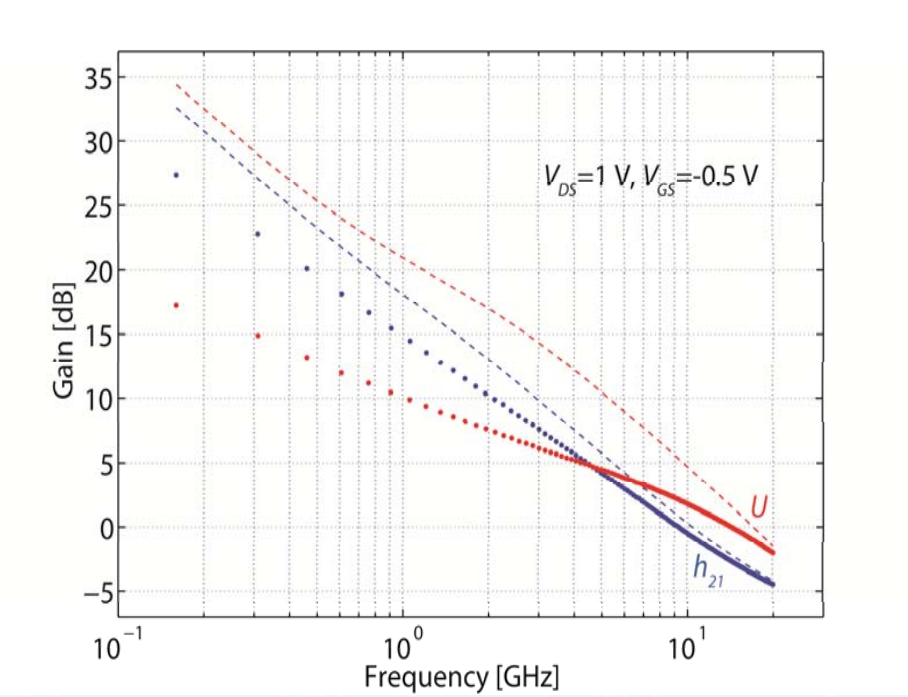


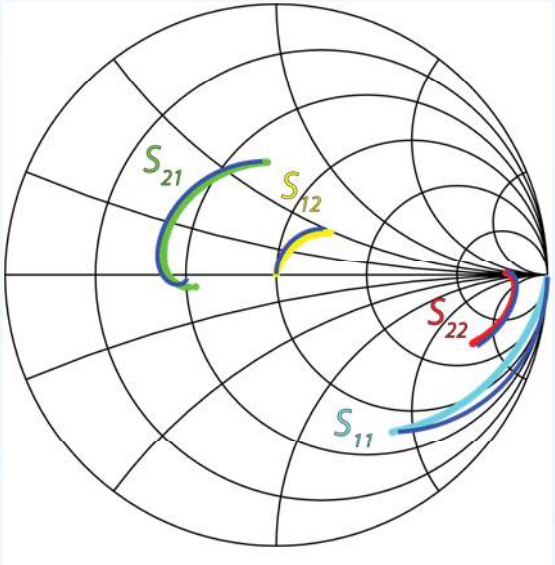
PMA 300 ºC
30 min
I_{max} 550 mA/mm

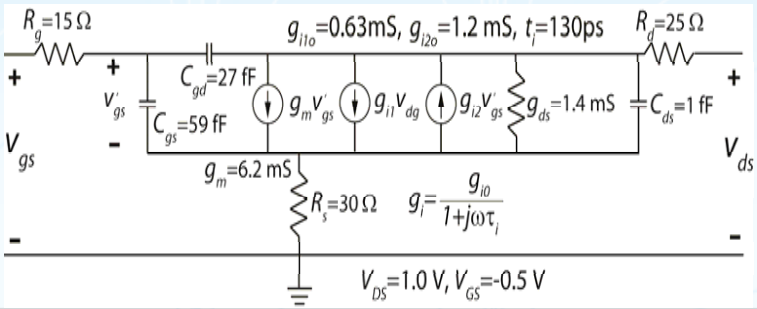
As processed device

InAs RF-transistors on 2” Si

Measured High-Frequency Properties



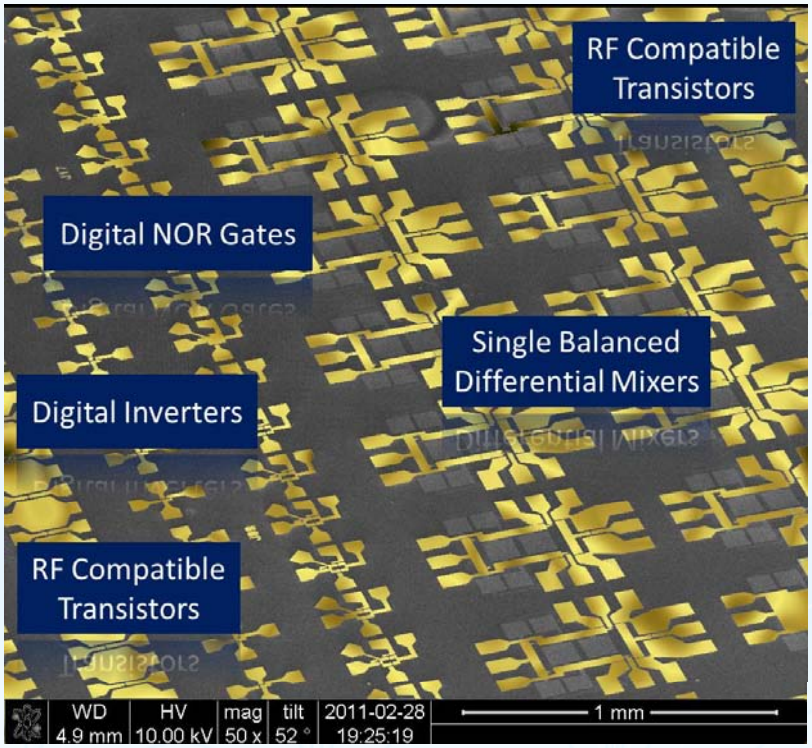




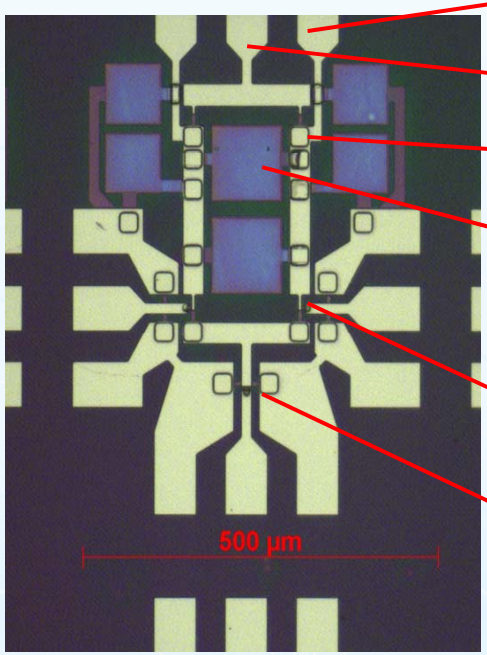
f_t and f_{max} limited by parasitics
Intrinsic f_t about 200-300 GHz
Non-ideal U and S11: High-κ?

InAs Circuits on 2” Si

Good wafers: 80% yield
Area: 2000x6000 µm²



First test circuit:
Balanced mixer



Output voltage

V_{dd}

Resistive loads

Capacitive decoupling

LO^+ and LO^- input

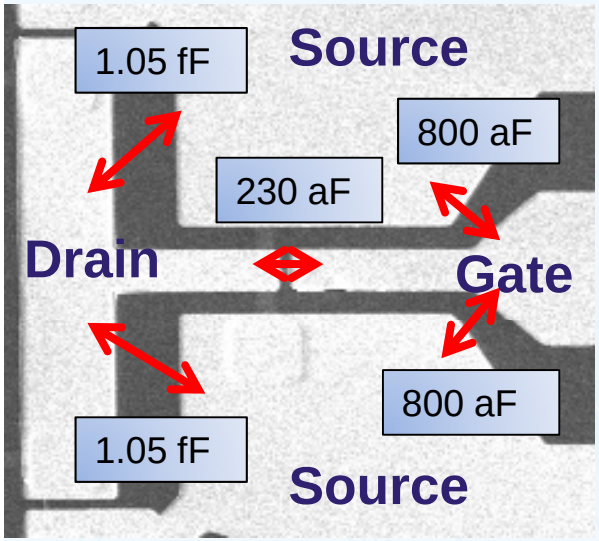
RF-input

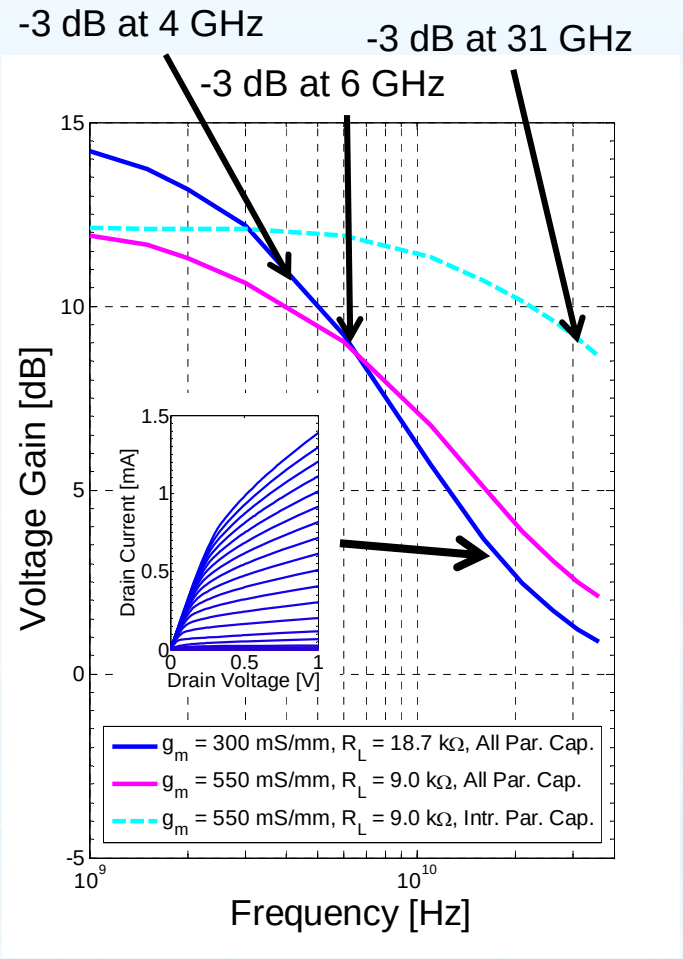
Design with 52 nanowire transistors
Nanowire resistors
Designed for 1 GHz input

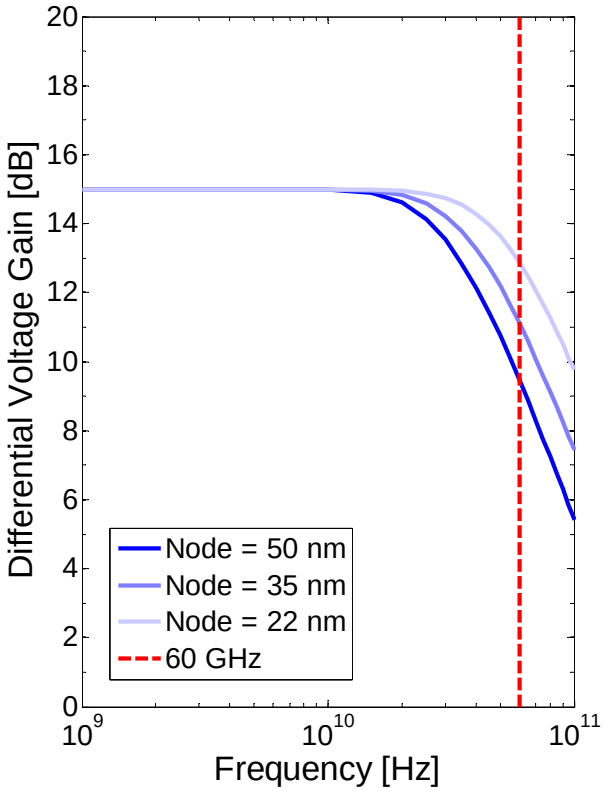
InAs Circuits on 2” Si

DC model from experimental data

Evaluation of parasitics







Par C_{gs}	Par C_{gd}	Par C_{ds}	Int C_{gs}	Int C_{gd}	Int C_{ds}
7.9 fF	6.5 fF	2.1 fF	1.6 fF	1.2 fF	0.7 fF

V_{dd}=1V
V_t=0.1 V
g_m=300 mS/mm

V_{od}=80 mV
I=51 µA
P=51 µW

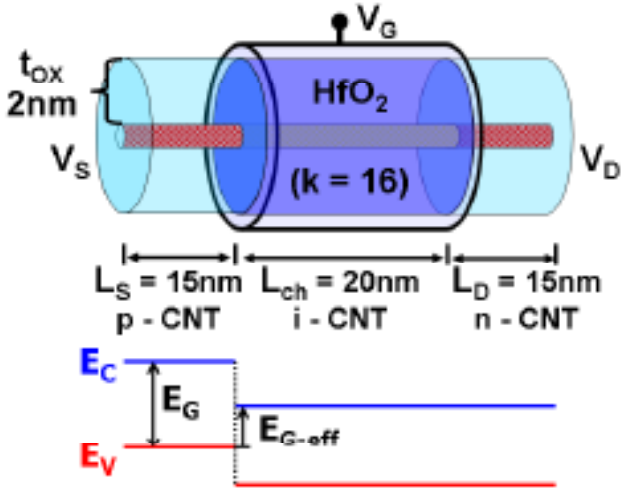
Benchmarking III-V MOSFETs

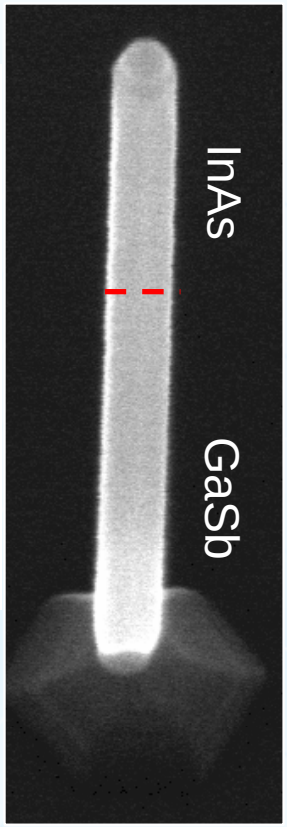
Technology	Drive current (mA/mm) V_{ds}=0.5V	Trans-conductance (mS/mm) V_{ds}=0.5V	L_g (nm)	SS (mV/dec)
Lund DC NW Transistors 2008	330	520	50	88
Lund RF NW Transistors 2011	140	1000	250	-
Lund Planar Transistors 2011	2000	1900	55	187
Intel FinFETs 2010	100	500	70	120
Purdue FinFETs 2009	150	200	100	170
Intel Planar 2009	550	1750	75	100
UCSB Planar * 2009	950	450	200	550

* V_{gs}=4 V_{ds}=2

New Device Concepts

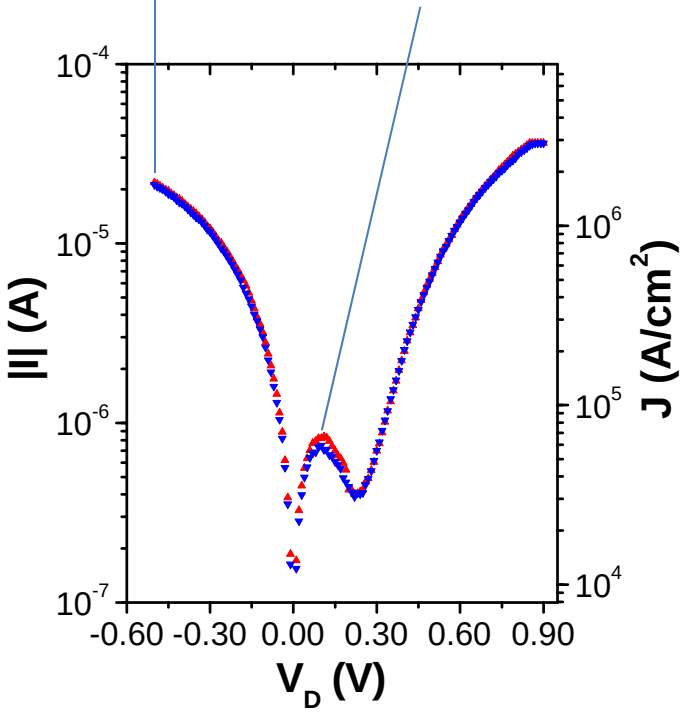
InAs/GaSb Esaki diodes for TFETs





-22 uA@ -0.50 V
(1750 kA/cm^2)

838 nA @ 0.11 V
(66.7 kA/cm^2)

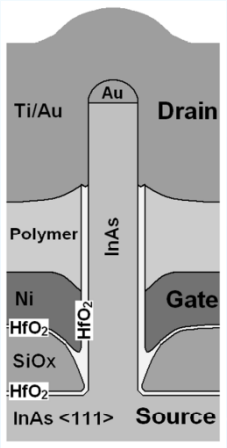


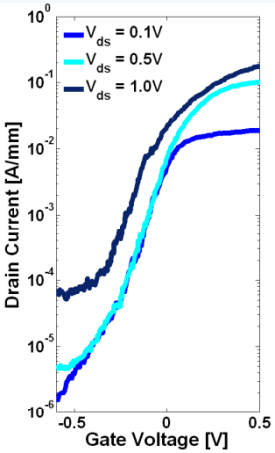
InAs growth at 460C

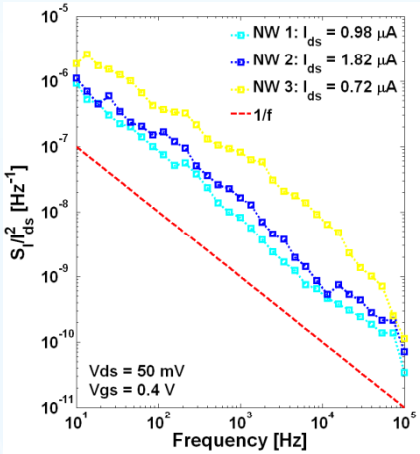
Diameter 40 nm
PVR @ RT = 2.1

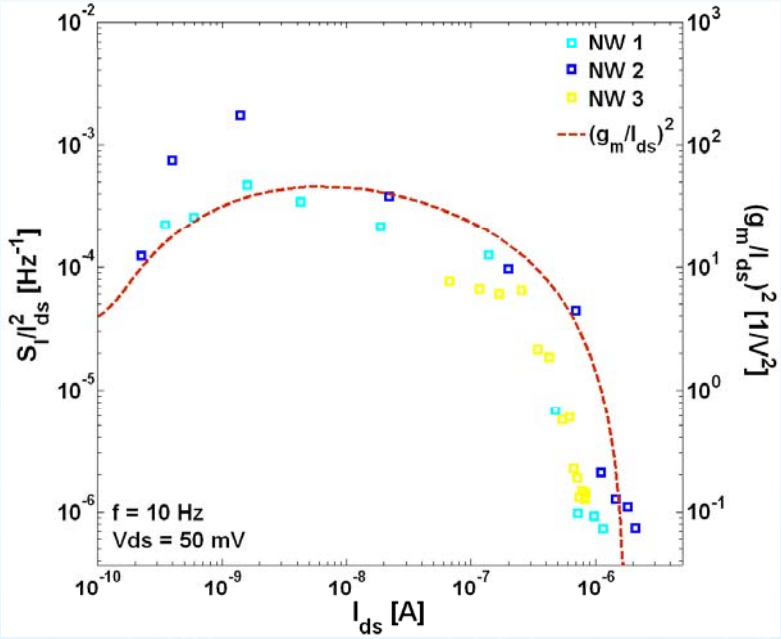
Low-Frequency Noise

Cross-section **DC-characteristics** **1/f-noise**









Average SS: **130 mV/decade**
Norm. I_{ds}: **0.16 S/mm**
V_T: **-0.1 to 0.0 V**

$$\frac{S_I}{I_{DS}^2} = \left(\frac{q^2 kT\lambda N}{f^\gamma WLC_{ox}^2}\right)\frac{g_m^2}{I_{DS}^2}$$

Hooge's Parameter: **4.2×10^{-3}**

Normalized 1/*f* Noise Figure: **7.3×10^{-7} Hz^{-1}**

Indication of number fluctuations.
Traps are equally distributed in energy.
Noise figure is comparable with other studies on NW FETs
The Hooge's parameter has a relatively low value.

Persson et al IEEE EDL, 31, 428 (2010)

Journal Publications 2010-2011

23 Journal Papers 2010-2011

1 Invited in Proceedings of IEEE

2 IEEE Trans Microwave Theory and Techniques

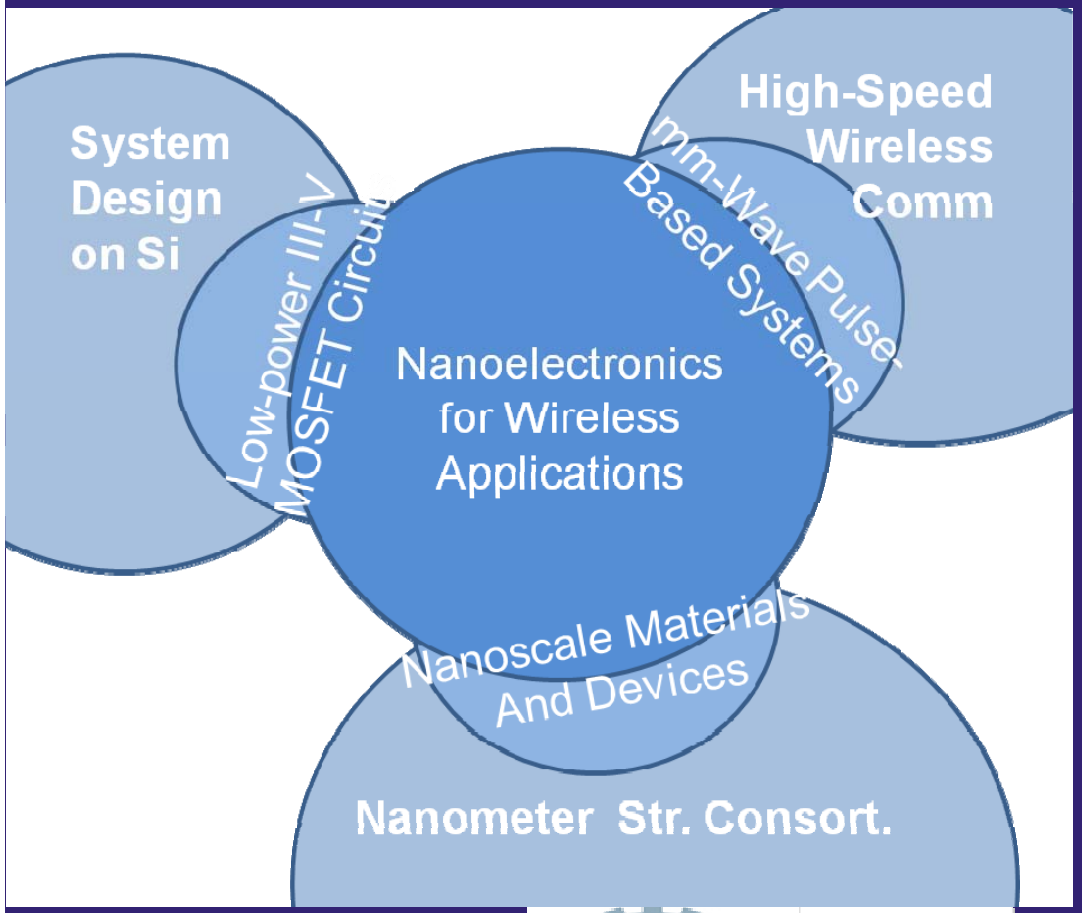
2 IEEE EDLs/Electronics Letters

1 IEEE MWCL

7 APLs/NanoLetters

3 patent applications filed

The Nanoelectronics Group



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