



#### Reconfigurable Cell Array as an Enabler for Future Processing

Chenxin Zhang<sup>1</sup>, Per Andersson<sup>2</sup>, and Viktor Öwall<sup>1</sup>

<sup>1</sup>Department of Electrical and Information Technology <sup>2</sup>Department of Computer Science Lund University, Sweden

Lund CD Workshop

Sep. 9<sup>th</sup>, 2011

### Outline

- Motivation
- Coarse-grained reconfigurable cell array
  - Resource cell
  - System reconfiguration
- Software development
  - Application mapping
  - Design exploration
- Case study: multi-standard OFDM synchronization



#### **Motivation**

- Hardware sharing
  - Accelerators: poor hardware reusability



- Reconfigurable architecture
  - + Multi-task
  - + Multi-standard
  - + Multi-algorithm
  - Control overhead, e.g. area, power.





#### **System infrastructure**

- An array of resource cells.
- Heterogeneous cell array:
  - Processing cell
  - Memory cell
  - Accelerator
    - (e.g. no configuration)
- Hierarchical cell array.



#### **Resource cell**

- Dedicated local interconnections:
  - High data throughput
- Hierarchical global routing network:
  - Flexible global data transmission
  - External data access
  - Global cell (re)configuration
- AMBA 4 AXI4-stream protocol
- Single-Cycle-Per-Hop latency
- Data driven synchronization
- GALS network data transmission



### **Processing cell**

- Processing core
  - ALU, DSP, SIMD, VLIW, CORDIC...
  - Implicit load-store operations in all instructions.
  - Run-time control and conditional reconfiguration.
  - In-cell NoC supervision and reconfiguration.
- Processing shell
  - Network adapter



P3 = f(P1, P2)

P2

P1



### **Memory cell**

- Cell structure:
  - Divided into banks
  - Configurations and operations handled locally
- Operation mode: FIFO & RAM
- Run-time memory cell concatenation in FIFO mode.
- Blocking/Non-blocking execution.
- Programmable descriptor execution.
- Micro-block memory access.





#### Static & Dynamic configuration (I)



## Static & Dynamic configuration (II)





#### Software development

- Automated application mapping.
  - CAL dataflow language
  - Parallelism exploration
  - Within the HiPEC project together with CS dept.

- Design exploration with SCENIC framework.
  - SystemC-based virtual platform
  - Explore system behavior and evaluate performance



CAL program

Hardwar Platform

Design

## **Application mapping**





#### **Application mapping from CAL**





#### **SCENIC** – Design Exploration



# Case study: multi-standard OFDM synchronization



- Multiple wireless radio standards
- Concurrent data stream processing
- Coarse Time Synchronization
- Carrier Frequency Offset (CFO) estimation







## Implementation results (I)

- 65 nm low-power regular VT CMOS:
  - Area: 0.479 mm<sup>2</sup>
  - Clock frequency: 534 MHz
- Adaptive word length scheduling.
- Adoption of different algorithms, e.g. Novel sign-bit OFDM acquisition.

	Concurrency	Standard	Quantization	Memory	
	Concurrency	Standard	accuracy	utilization	
		802.11n	4 bits	08.48%	
-	Single-Stream	LTE	4 bits	65.18%	
		DVB-H2K	4 bits	85.71%	
		DVB-H4K	2 or Sign bit	85.71%	
		DVB-H8K	Sign bit	85.71%	
		802.11n & 802.11n	4 or 2 bits	16.96%	
		802.11n & LTE	2 bits	45.09%	
	Dual-Stream	802.11n & DVB-H2K	2 bits	65.63%	
		LTE & LTE	2 bits	73.21%	
		LTE & DVB-H2K	2 bits	93.75%	
		-	-	-	





## Implementation results (II)

- Compare with ASIC solution, ~4 times more area cost.
- Case study does not explore the potential usage.
  - Simple algorithms
  - No task-level hardware sharing
- Currently looking at channel estimation & MIMO detection for LTE-A.
  - Task-level hardware sharing
  - Cooperation with the DARE project







#### **Configuration generator**

	Processor Cell	0 Configuration			_ 🗆 🛛		a Generator		Memory Cell 0 De	escriptor Configura	tion			
	File					File Setup Convert	About		File					
	PC Control Assemily Program							Execution DSC Configuration						
	ATLA								DM/DSC Configuration Header					
	PC control PC Control(0) Reset				PC0 (DST_ID0) MC0 (DST_ID1)			Config header	DSC(0)	×	Generate			
sector   generic <t< td=""><td>1 O Control</td><td>1.0_001101(0)_11030</td><td></td><td>denside</td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td></t<>	1 O Control	1.0_001101(0)_11030		denside						1				
Tege         Ordingwinetworkset         Ordingwinetworkset <td>Operation</td> <td>Write/Read</td> <td>Control operati</td> <td>ion, Default Write; Che</td> <td>ecked: Read</td> <td></td> <td></td> <td></td> <td>Operation</td> <td>🔲 Write/Read</td> <td>Contro</td> <td>ol operation, Default: W</td> <td>/rite; Checked: Read</td> <td></td>	Operation	Write/Read	Control operati	ion, Default Write; Che	ecked: Read				Operation	🔲 Write/Read	Contro	ol operation, Default: W	/rite; Checked: Read	
cordini che Cordinad dell'addella dottavatte. Chekel Diale Diale Diale della dottavatte addella dottavatte	Target	Program/Control	Configuration t	arget, Default: Program	m memory; Checked: Control register				Config. target	DM/DSC	Config	guration selection, Defa	ault: Data memory; Checked:	Descriptor
	Condition	Enable	Conditional co	nfiguration, Default: Di	sable; Checked: Enable				Start Addr.	0	Startin	ng address in memory	array	
	Condition addr.	0	Conditional co	nfiguration address			MC2 (DST ID4)		Transfersize	3	The n	umber of Data/Configu	ration packages	
											_			
I U U U U U U U U       I U U <td>Control options</td> <td>PC undate</td> <td>C Short</td> <td>Davina 🔽 D</td> <td>loost</td> <td></td> <td></td> <td></td> <td>Config. DSC</td> <td>DSC0</td> <td>DSC1</td> <td>DSC2</td> <td>DSC3</td> <td></td>	Control options	PC undate	C Short	Davina 🔽 D	loost				Config. DSC	DSC0	DSC1	DSC2	DSC3	
	Control opaons	- rc upuate	Stait	jrause 💽 n	ICSCI				Start config. pack	🗹 Package 0	📃 Package 1	🔲 Package 2		
		Step	Run to	Stop										
Add option •     Quarterine Meensery Address Saftup     Betra meterine     Both Mark Rg     Both Mark Rg    Both Mark Rg     Both Mark Rg     Both Mark Rg     Both Mark Rg     Both Mark Rg     Both Rg     Both Rg        Both Rg <td></td> <td></td> <td></td> <td></td> <td></td> <td>MC 1 (DST ID 2)</td> <td></td> <td>PC 1 (DST_ID 3)</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>						MC 1 (DST ID 2)		PC 1 (DST_ID 3)						
	Addr option	0	Address option	note										
									- Devening a Exercition O	and and a				
pur dener y Addens Svelig her name Ren name	]								Descriptor Excedition C					
Bit name       D 600       D 601       D 600       D 601       D 602       D 603         D 701       D 102       37       D 102       37       D 102       D 603       D 601       D 602       D 603         D 104       D 104       D 70       PF       D 603       D 601       D 603       D 601       D 602       D 603         D 104       D 603       D 70       PF       D 603       D 601       D 603       D 601       D 603	figuration Memory A	Address Setup							DSC execution	MC(0)	*	Generate		
Start starts (Def)         Start starts (Def)         O de 20         O									DSC anable		Dect	Deco		
0 C PRA LOL (Page)       0	Object name	Start address [Dec]	Start address [Hex]	End address [Dec]	End address [Hex]				DSC enable	Daco	Daci	Dac2	Daca	
Dia Magnetic       Dia Magnetic       Prime       Prim       Prim       Prime       Prime <td>PC0 PGM &amp; Ctrl_Reg</td> <td>0</td> <td>0</td> <td>1023</td> <td>3FF</td> <td></td> <td></td> <td></td> <td>Dac state reset</td> <td>M DSCU</td> <td>DSCI</td> <td>☑ D802</td> <td>Daca</td> <td></td>	PC0 PGM & Ctrl_Reg	0	0	1023	3FF				Dac state reset	M DSCU	DSCI	☑ D802	Daca	
000 Public Monorpoint     004     000     007     PF       000 Public Monorpoint     007     007     977     000     989     FF       000 Public Monorpoint     007     976	PC1 PGM & Ctrl_Reg	1024	400	2047	7FF	- Configuration Gener	ator		- 🗌 🔀 ogram	Enable	Descri	iptor execution prograr	m select	
1C1 Data Many       322       0.0       338       FF         1C1 Data Many       320       F00       3375       F24       3311       F47         1C1 Data Many       376       F24       3311       F47       F68       Seconda Participanti III       Configation Lit       Configation Lit       FC	MCO Data Memory	2048	800	3071	BFF	File Update			)m. mode	🔲 Resume/Resta	t DSCe	xe. pgm. operation mo	ode, Default: Resume; Check	ed: Restart
0000 monopia       340       90       975       72         1010 monopia       3476       744       341       F47         122 concipia       342       748       347       758         122 concipia       342       748       344       768       768         1334       760       349       760       349       760       349       760         1337       758       356       756       356       757       3565       773       757       3565       774       3565       774       3565       774       3565       774       3565       774       3565       774       3565       774       3565       774       3565       774       3565       774       3565       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774       3567       774	MC1 Data Memory	3072	C00	3839	EFF	Configuration List OVM file	Special Control		ogram size	0	The nu	umber of programs to e	execute (Max. 16)	
11 Decorptiv       3976       F24       3911       F47         12 Decorptiv       3912       F46       3947       F88       F82         contrig Reg11       3948       F60       3948       F60       500         contrig Reg11       3949       F60       3948       F60       500	MC0 Descriptor	3840	F00	3875	F23	Configuration List:		Configuration Database:			E e: D		oize: 6	
122 Decorptor       312       F48       947       F68         122 Decorptor       312       F48       947       F68         scoritg Reg(1)       3448       F60       946       F60         scoritg Reg(1)       3949       F60       946       950         scoritg Reg(1)       3949       F60       946       950         scoritg Reg(1)       3950       F6E       950       F6F         scoritg Reg(1)       3953       F71       3955       F73         scoritg Reg(1)       3956       F74       3956       F73         scoritg Reg(1)       3958       F76       3956       F77         scoritg Reg(1)       3958       F77       3956       F73         scoritg Reg(1)       3958       F76       3956       F73         scoritg Reg(1)       3958       F77       3959       F76         scoritg Reg(1)       3958       F77       3959       F78         scoritg Reg(1)       3960       F78       3960       F78         scoritg Reg(1)       3961       F79       5950       F73         scoritg Reg(1)       3961       F78       3960       F78	MC1 Descriptor	3876	F24	3911	F47	PC_1_Program			ogram	6	D:	SC(0)	13126.0	
corrig Reg(1)       349       F6C       349       F6D       349       F6D         corrig Reg(1)       349       F6D       349       F6D       550       550         corrig Reg(1)       350       F6       350       F6E       550       770         corrig Reg(1)       355       F7       355       F71       550       771         corrig Reg(1)       355       F72       354       F72       354       F72         corrig Reg(1)       356       F74       365       F74       505       673       3957       F75         corrig Reg(1)       356       F76       356       F77       505       577       505       577         corrig Reg(1)       356       F76       356       F77       505 <t< td=""><td>MC2 Descriptor</td><td>3912</td><td>F48</td><td>3947</td><td>F6B</td><td>PC_1_Control_0_Reset PC_1_Control_1_PCUpdate</td><td>,</td><td></td><td></td><td></td><td>D</td><td>SC(2) SC(0)</td><td></td><td></td></t<>	MC2 Descriptor	3912	F48	3947	F6B	PC_1_Control_0_Reset PC_1_Control_1_PCUpdate	,				D	SC(2) SC(0)		
corrig Reg11       3949       F60       3949       F60       990       F6E       990       F71       995       F73       995	Reconfig. Reg[0]	3948	F6C	3948	F6C =	PC_1_Control_2_Start PC_0_Program					D	SC(2)		
corring Reg12       3900       Fbk       3950       Fbk       3950       Fbk         corring Reg13       3951       FFF       9951       FBF       9951       FBF         corring Reg13       3953       F71       3953       F71       9953       F71         corring Reg13       3956       F73       9956       F73       9956       F74         corring Reg13       3957       F76       3958       F776       3958       F776         corring Reg113       3961       F77       3953       F77       9960       F78         corring Reg13       3961       F79       3960       F78       MC_DOSC and C2       MC_DOSC and C2         widt DoSC and C2       MC_DOSC and C2         corring Reg113       3961       F77       3963       F77       MC_DOSC and C2       MC_DOSC and C2 <td>Reconfig. Reg[1]</td> <td>3949</td> <td>F6D</td> <td>3949</td> <td>F6D</td> <td>PC_0_Control_0_Reset</td> <td></td> <td></td> <td></td> <td></td> <td>D</td> <td>SC(1) SC(3)</td> <td></td> <td></td>	Reconfig. Reg[1]	3949	F6D	3949	F6D	PC_0_Control_0_Reset					D	SC(1) SC(3)		
conting flegil 3       351       PEF       361       PEF         conting flegil 3       352       F70       3952       F70         conting flegil 3       365       F71       9853       F71         conting flegil 3       365       F73       3856       F73         conting flegil 3       365       F73       3856       F73         conting flegil 3       365       F74       3956       F74         conting flegil 3       365       F73       3957       F75         conting flegil 3       3661       F74       3958       F76         conting flegil 3       3661       F73       1000 Effectual 3       1         conting flegil 1       3658       F76       3959       F77         conting flegil 2       3661       F79       3661       F79         conting flegil 3       361       F79       3661       F79         conting flegil 3       3661       F79       3661       F79         conting flegil 3       3661       F79       1       C         conting flegil 3       3661       F79       C       C       C       C         Color Stelesculan       C       C <td>Reconfig. Reg[2]</td> <td>3950</td> <td>FBE</td> <td>3950</td> <td>F6E</td> <td>PC_0_Control_2_Start</td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td>(-)</td> <td></td> <td></td>	Reconfig. Reg[2]	3950	FBE	3950	F6E	PC_0_Control_2_Start					-	(-)		
Backer Frid       353.2       Frid       353.2       Frid       353.2       Frid         Backer Frid       3953       F71       3953       F71       3953       F71         Backer Frid       3953       F71       3953       F71       3955       F73         Backer Frid       3955       F73       3955       F73       3955       F74         Backer Frid       3956       F74       3956       F74       3956       F74         Backer Frid       3957       F75       3957       F75       3957       F75         Backer Frid       3958       F76       3959       F77       3959       F77         Backer Frid       3956       F78       3960       F78       MC_0 DSC Header_0       MC_0	Recontig. Reg[3]	3351	F0F	3351	F0F	MC_0_DataMemory_0 MC_0_DSCHeader_0	-							
contra Bodie       000       111       000       111         contra Bodie       3954       F72       3954       F72         contra Bodie       3956       F73       3955       F73         contra Bodie       3956       F74       3956       F74         contra Bodie       3957       F75       3957       F75         contra Bodie       3958       F76       3958       F77         contra Bodie       3950       F77       3959       F77         contra Bodie       1000 ECE-actuin       MC_DOSC_2       MC_DOSC_2         MC_DOSCAR       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR         contra Bodie       F76       3959       F77       3959       F77         contra Bodie       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR         contra Bodie       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR         contra Bodie       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR         contra Bodie       F78       3961       F79       3961       F73       MC_DOSCAR       MC_DOSCAR       MC_DOSCAR         MC_DOSCAR       MC_DOSCAR       MC_DOSCAR	Reconfig. Reg(4)	3953	F71	3953	F71	MC_0_DSC_0 MC_0_DSCHeader_1	• • • •							_
config. Reg/1       395       F73       3955       F73         econfig. Reg/3       3956       F74       3956       F74         econfig. Reg/10       3957       F75       3957       F75         econfig. Reg/11       3959       F77       3959       F77         econfig. Reg/12       3960       F78       3961       F78         econfig. Reg/13       3961       F79       3961       F73	Reconfia, Rea(6)	3954	F72	3954	F72	MC_0_DSC_1 MC_0_DSCHeader 2	(m)		and the second s			and the second second	1000	1 10 Mar
econfig Regi8]       3956       F74       3956       F74         econfig Regi3]       3957       F75       3967       F75         geonfig Regi10]       3958       F76       MC_10 SEC seculion MC_10 s	Reconfig. Reg(7)	3955	F73	3955	F73	MC_0_DSC_2 MC_0_DSCHeader_3	>>>					Stra 25	and the second second	
econfig. Reg(9)       3857       F75       3857       F75         econfig. Reg(10)       3958       F76       3858       F76         econfig. Reg(11)       3959       F77       3959       F77         econfig. Reg(12)       3960       F78       3960       F78         econfig. Reg(13)       3961       F79       3960       F78	Reconfig. Reg(8)	3956	F74	3956	F74	MC_0_DSC_3						A States	and the	
econfig Reg110       3568       F76       3568       F76         econfig Reg111       3559       F77       3959       F77         econfig Reg112       3960       F78       3660       F78         econfig Reg113       3561       F79       3961       F79         Image: Config Reg113       3561       F79       3961       F79         Image: Config Reg113       3561       F79       Image: Config Reg113       Image: Config Reg113         Image: Config Reg113       Stol       F79       Image: Config Reg113       Image: Config Reg114       Image: Config Reg115       Image: Config Reg115       Image: Config Reg116       Image: Config Reg117       Image: Config Reg118       Image: Config Re	Reconfig. Reg(9)	3957	F75	3957	F75	MC_1_DataMemory_0						1000		
econfig. Reg111] 3363 F77 3363 F77 econfig. Reg112] 3960 F78 3360 F78 econfig. Reg113] 3961 F79 3361 F73	Reconfig. Reg(10)	3958	F76	3958	F76	MC_1_DataMemory_1 MC_1_DSCHeader_0						Section Section		
econing. Reg112] 3960 F78 3960 F78 econing. Reg113] 3961 F79 3961 F79	Reconfig. Reg[11]	3959	F77	3959	F77	MC_1_DSC_0 MC_1_DSCHeader 1				1	10 10 10	A 40 10-		
econig. Reg[13] 3961 F79 3961 F73	Reconfig. Reg[12]	3960	F78	3960	F78	MC_1_DSC_1 MC_1_DSCHeader_2	~			2.	1000	A CONTRACTOR		
MC_1_DSLEweedin V	Reconfig. Reg[13]	3961	F79	3961	F79	MC_1_DSC_2				1	1000		and the second se	
	1 100	and the second second	C. Links Colors		and the second second	MC_1_DSCHeader_3 MC_1_DSC_3	- ×		1	The second second	AT		and the second	
		and the second second				MC_1_DSCExecution					A COLOR OF	and the second second	and the second second	
	1	and the second second	and the second	Part Share					03	S and the second		AL OF	and the	A CONTRACTOR
													14/172	-160
													S TITLE	NIN-

## Conclusion

- Reconfigurable cell array enables hardware sharing at different levels, i.e., task-, function-, and algorithm-level.
- Coarse-grained reconfigurable cell array comprises distributed processing and memory cells, and a *hierarchical* NoC structure.
- In-cell *dynamic reconfiguration* enables fast context switching.
- Application mapping from CAL and design exploration with SCENIC tool.
- The system flexibility is illustrated by performing OFDM synchronization for multiple standards.





