2011/12

Cellular IC design – RF, Analog, Mixed-Mode

Mohammed Abdulaziz, Mattias Andersson, Jonas Lindstrand, Xiaodong Liu, Anders Nejdel

Ping Lu, Luca Fanori

Martin Anderson, Lars Sundström, Pietro Andreani

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Overview

- A reconfigurable channel-select filter
  - Mohammed Abdulaziz
- A continuous-time ΔΣ A/D converter
  - Xiaodong Liu
- A filtering continuous-time ΔΣ A/D converter
  - Mattias Andersson
- PA / TX circuits
  - Jonas Lindstrand
- A noise-shaping time-to-digital converter
  - Ping Lu

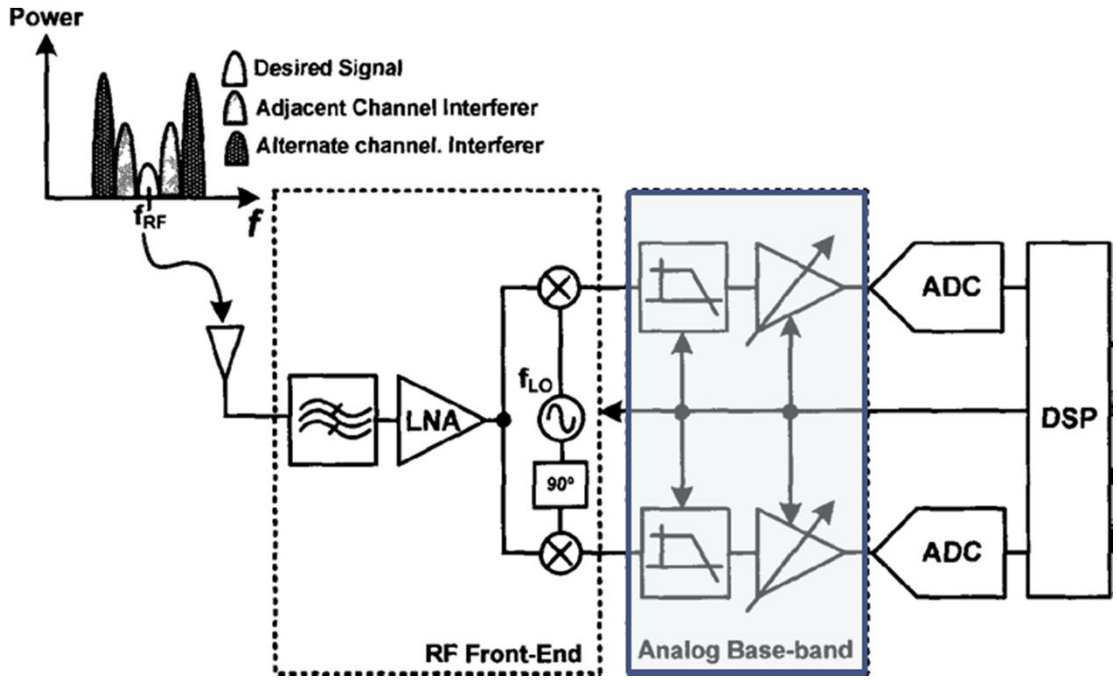
Overview – II

- Linear RX front-end (previous presentation)
  - Anders Nejdel (SSF DARE project)
- Highly efficient class-C VCO (next presentation)
  - Luca Fanori (FP7 DRAGON project, SoS)
- RX BB for carrier aggregation (not included)
  - Martin Anderson, Lars Sundström

A reconfigurable channel-select filter (SSF DARE project)

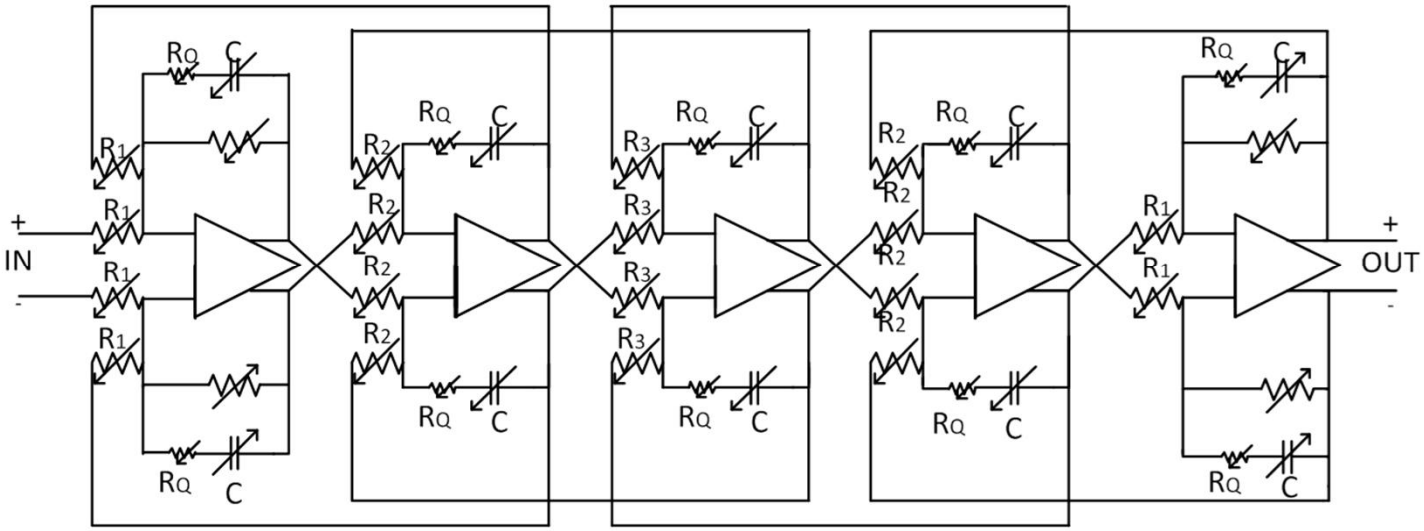
Mohammed Abdulaziz

- Limit unwanted signals falling close to the baseband
- Relax the dynamic range requirements of the ADC



Project goals and challenges

- Linearity vs. noise control via digital control word
- Break the linearity vs. noise trade-off with a linearization scheme

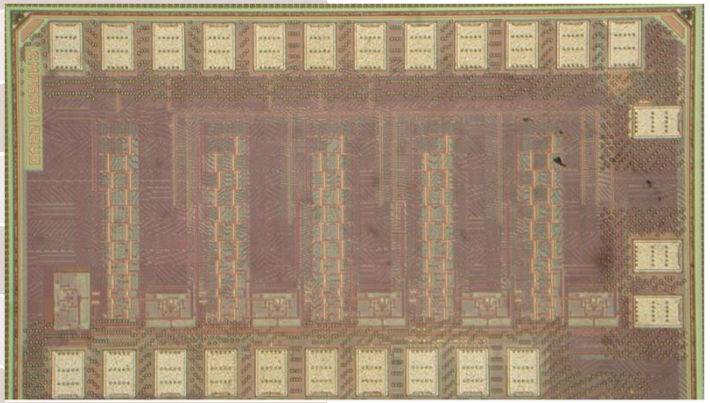


- R_Q: tunes the Q factor of the filter
- C: selects the operating band
- R1, R2 and R3: compensate process variations

Chip photo and Simulations

Taped out in June 2012, under measurement

Parameter	Value
Process Technology	65nm CMOS
Response	Chebyshev
Order	5^{th}
Power Supply	1.2 V
Current Consumption	3.2 mA
Input Referred Noise	38nV/√Hz
IIP3	24 dBm
Frequency Bands	20/15/10/5/3/1.4 MHz
Tuning Range	±40%



Complete RF front-end (LNA+Mixer+Filter) for Oct. 2012 TO

Wideband A/D converters (SSF DARE project)

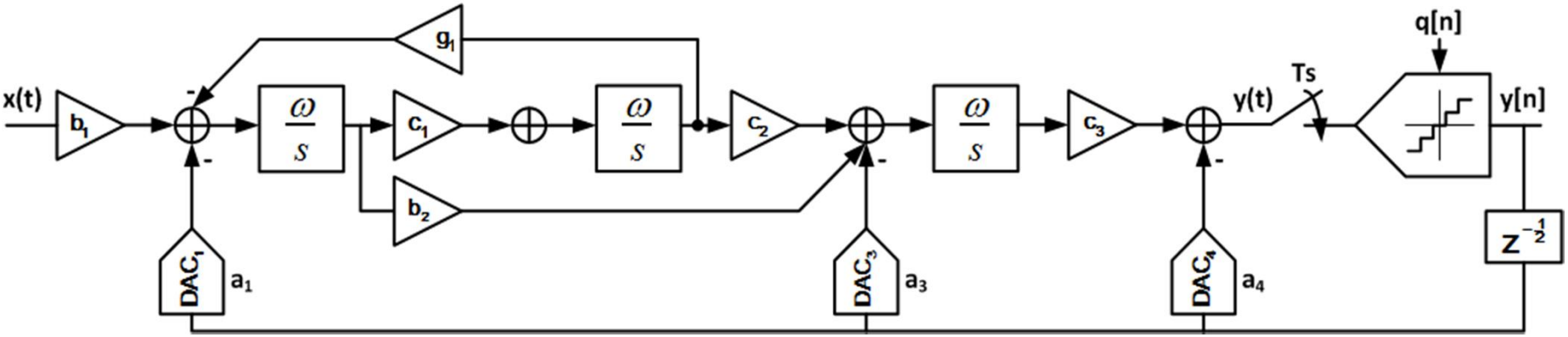
Xiaodong Liu

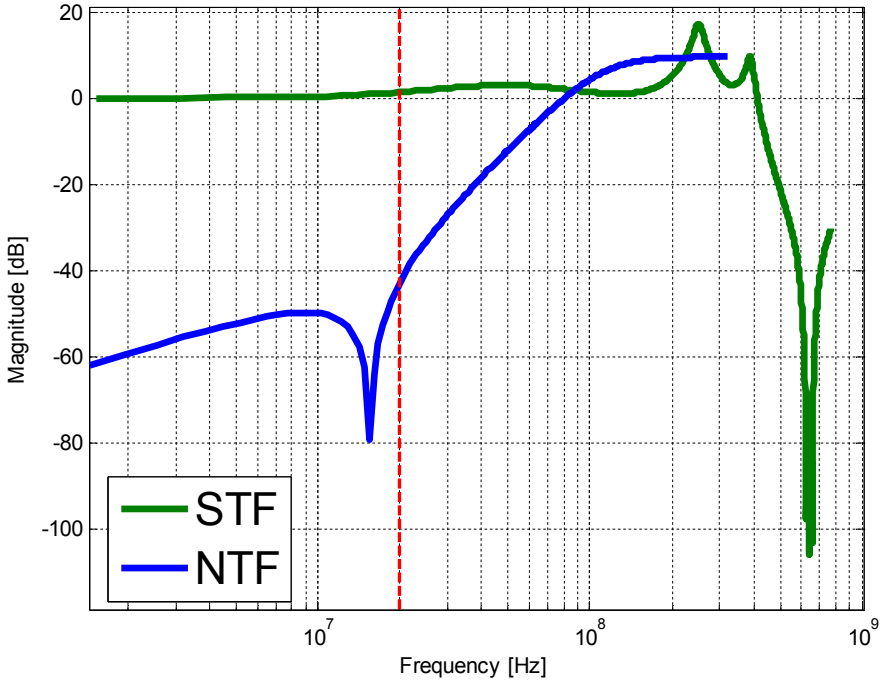
- 3^{rd} order, 4-bit, f_s=640MHz, BW=20MHz (OSR=16)

- Goal
  - To meet the bandwidth requirement of LTE Advanced standard (20MHz to 100MHz)
  - To demonstrate the feasibility of reducing power consumption while maintaining a good SNR by means of digital enhancement techniques

- Approach
  - Continuous-time Delta-Sigma modulator is attractive for BW beyond 20MHz
  - Pipelined A/D is a good candidate for the LTE Advanced maximum bandwidth of 100MHz

Delta-Sigma A/D – system level design

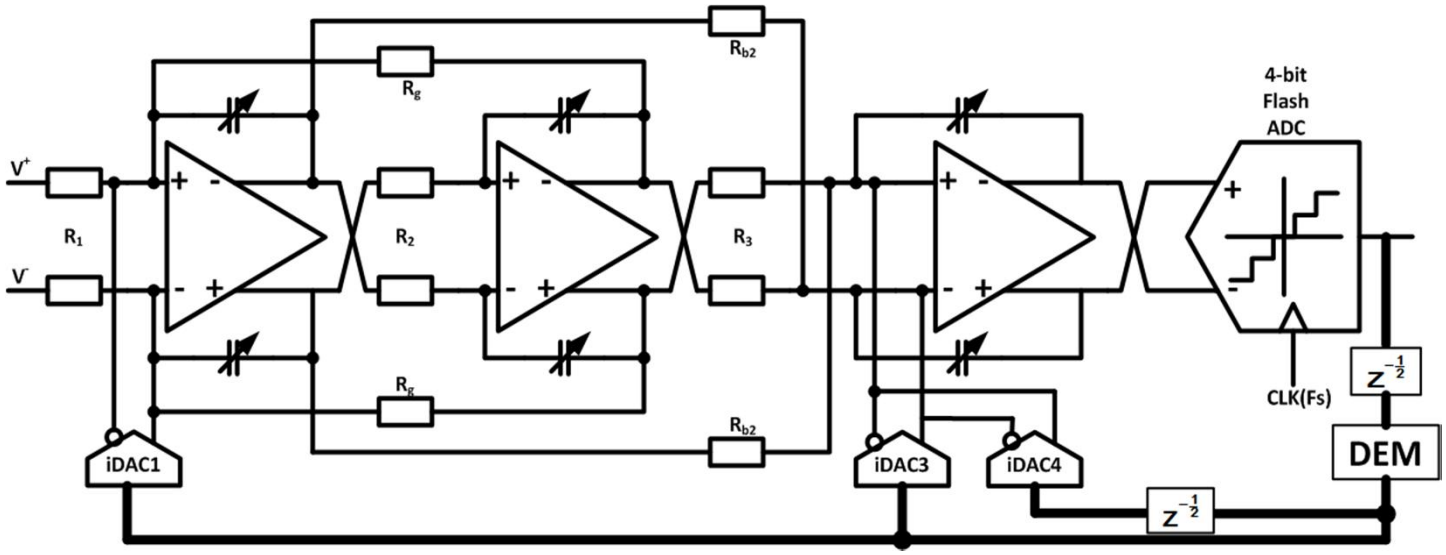




- CT sigma-delta modulator with inherent anti-aliasing
- Combination of feedforward and feedback topology
- Direct feedback path around quantizer through DAC_4 for delay compensation

Circuit implementation

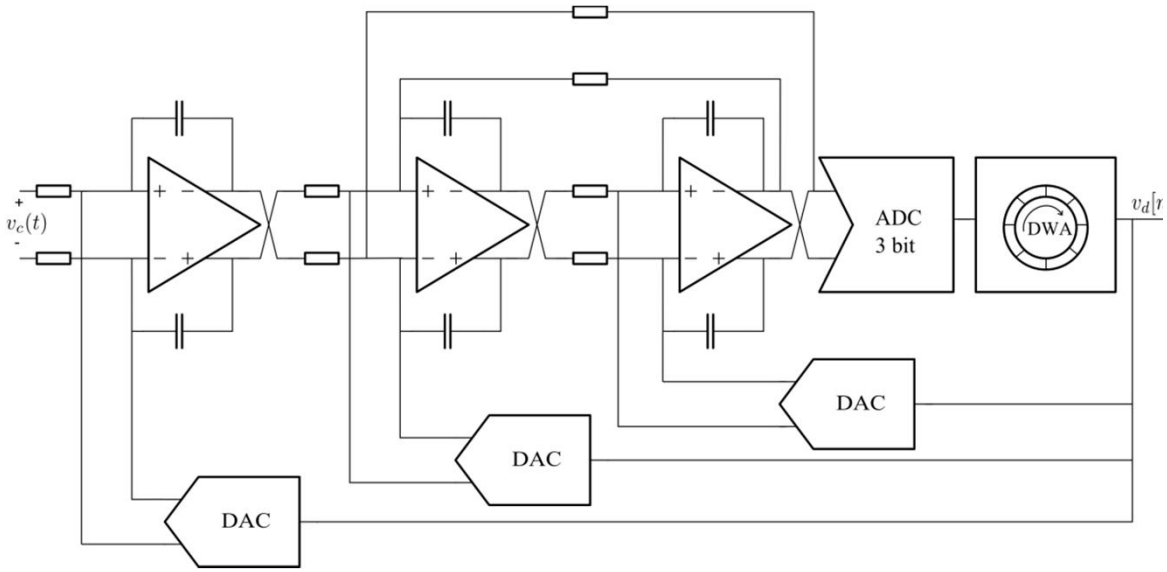
- Active-RC op-amp filter with feedforward gm compensation in the op-amp
- Current-steering DAC with non-return to zero (NRZ) pulses
- Dynamic element matching to mitigate distortion effect of mismatch in the DAC elements
- TO in March 2013

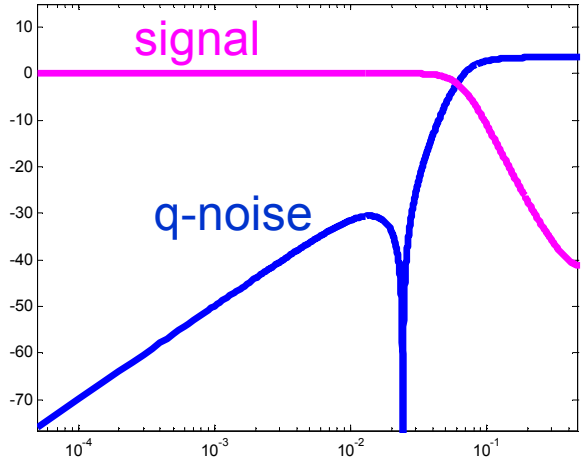


Continuous-Time ΔΣ ADC for LTE (FP7 DRAGON project, SoS)

Mattias Andersson

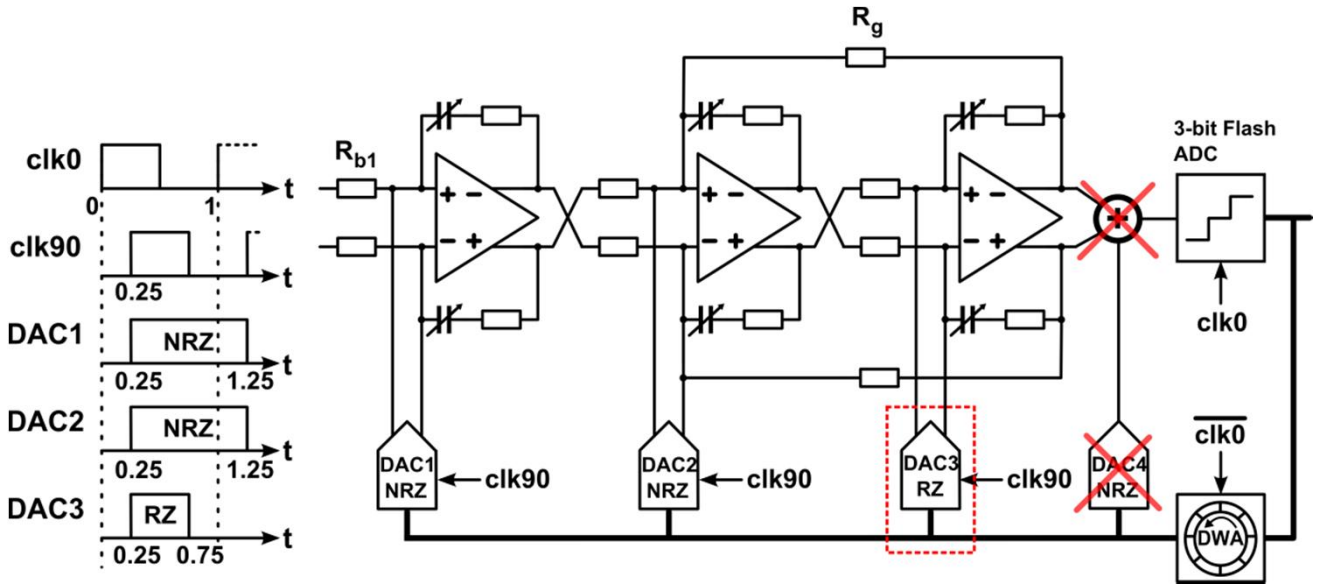
- 3rd order, 3-bit, f_s=288MHz, BW=9MHz (OSR=16)





Tayloring the feedback pulses for the three DACs, the 4th DAC around the quantizer is avoided!

Design details

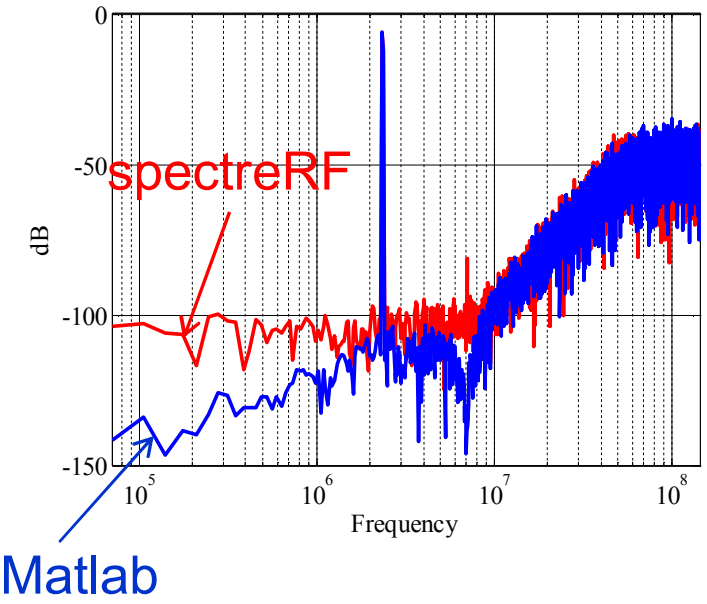


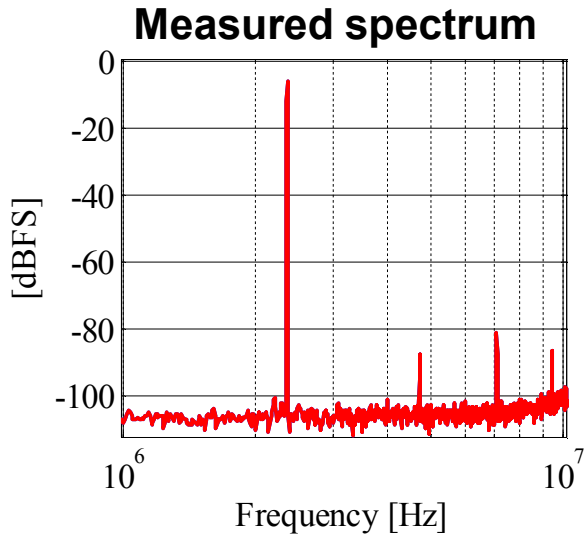
RZ pulses in DAC3 reduce sensitivity to loop delay

Loop delay compensation (DAC4) can be omitted

Quadrature clock phases assumed (available ”for free” in any radio RX)

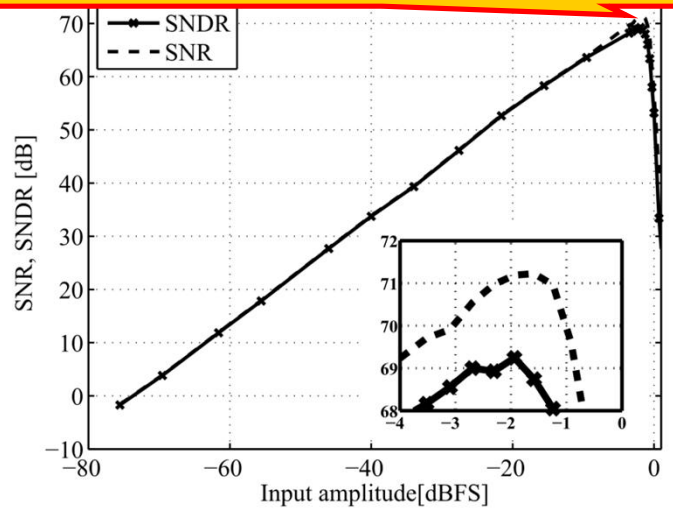
Measurement results





Very good predictions with spectreRF + transient noise

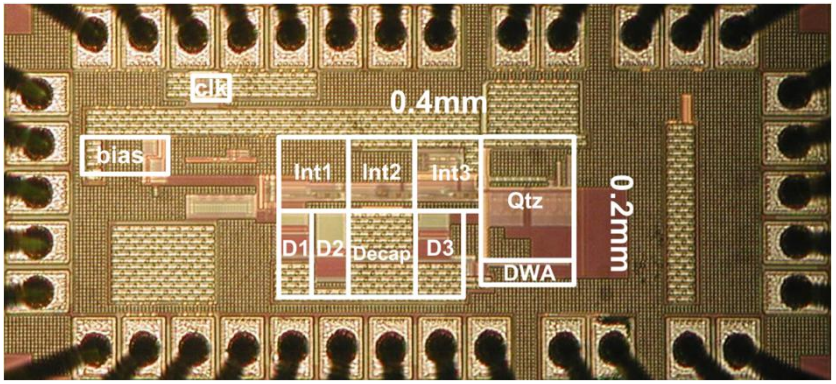
Peak SNDR 69dB **Peak SNR 71dB**



Chip photograph and performance summary

To be presented at the A-SSCC 2012

65nm CMOS



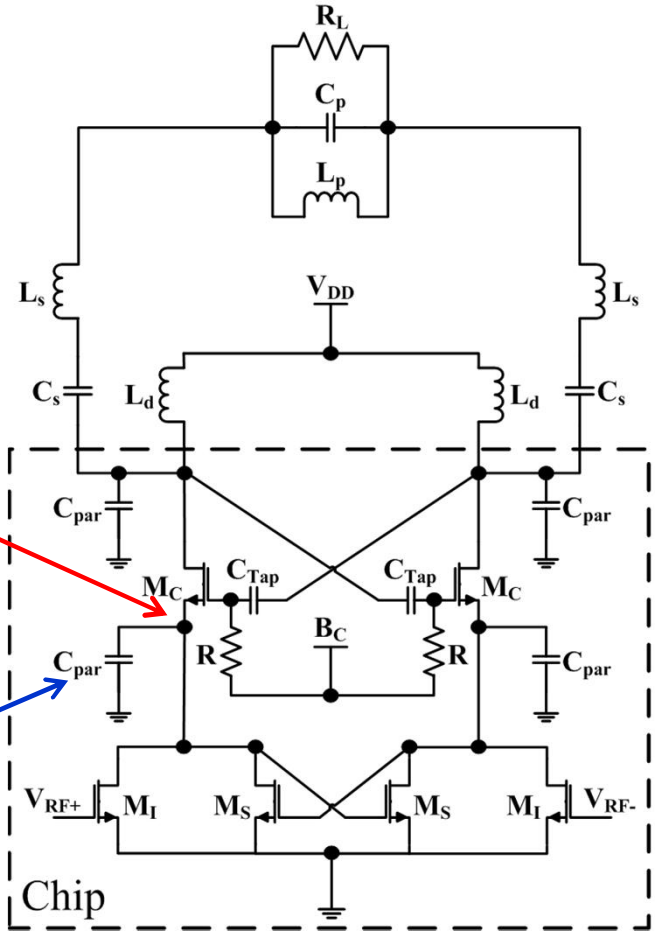
Parameter	Value
BW	9MHz
OSR	16
SNDR	69dB
I_{vdd}	6.2mA
FOM	175fJ/conv step
Area	0.1mm^2

Improved version with added filtering action:
TO in June 2012 (not yet received), and again in Oct. 2012

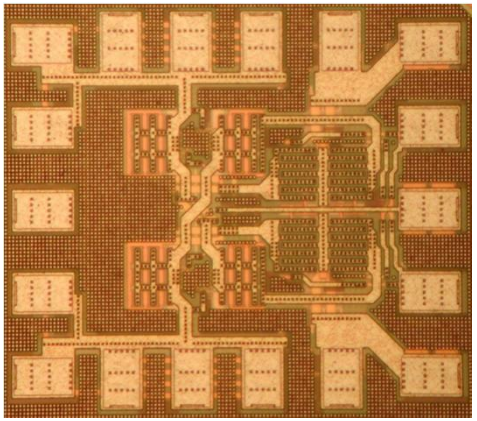
Power Amplifier in 65nm CMOS (VINNOVA, SoS)

Jonas Lindstrand

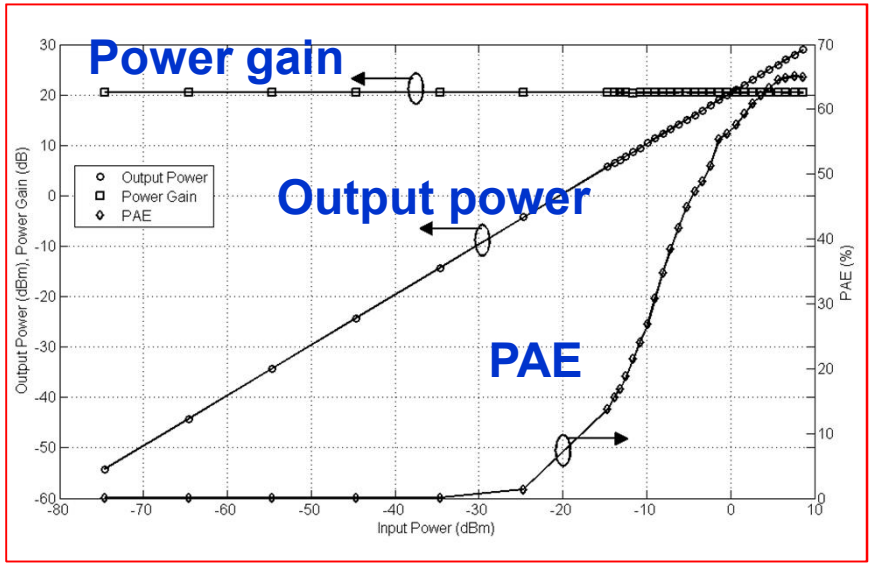
- Self-oscillating PA
  - Supply (V_{dd}) modulation
  - Reduced switching losses
- Wideband injection lock
  - Resistive injection node
  - M_S amplifies injected current
- Tapped cascode
  - C_{Tap} + $C_{par,Mc}$
  - Reduced stress on M_I/M_S
  - Reduced "SC" loss on C_{par}



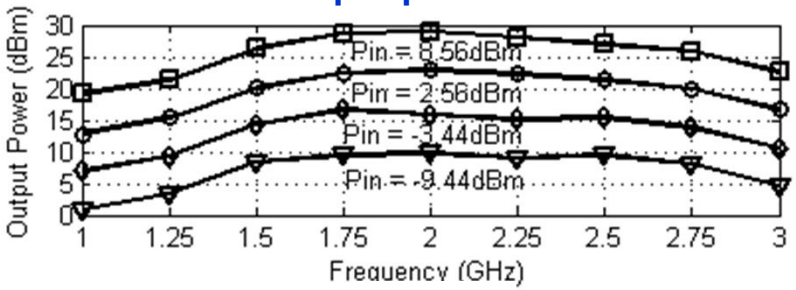
Chip photograph and performance



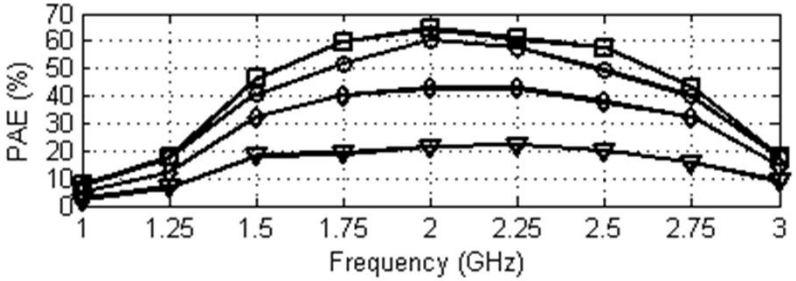
Presented at ESSCIRC 2011



Output power



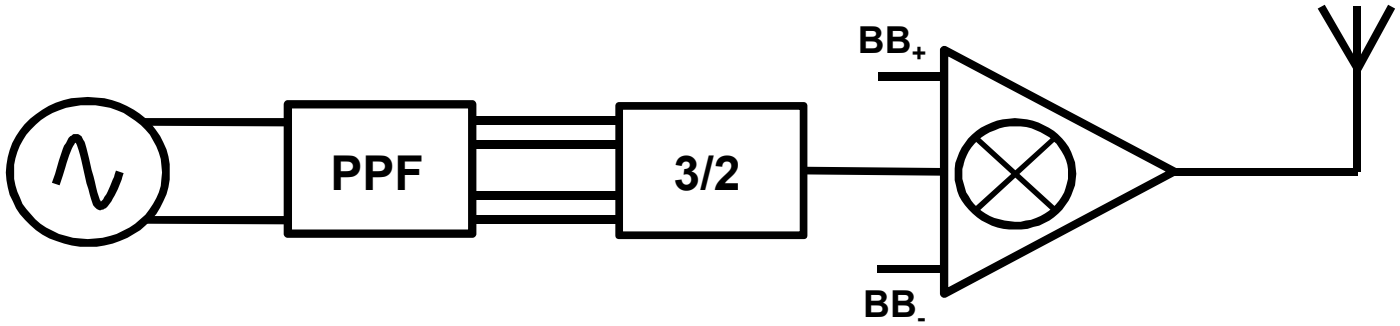
PAE



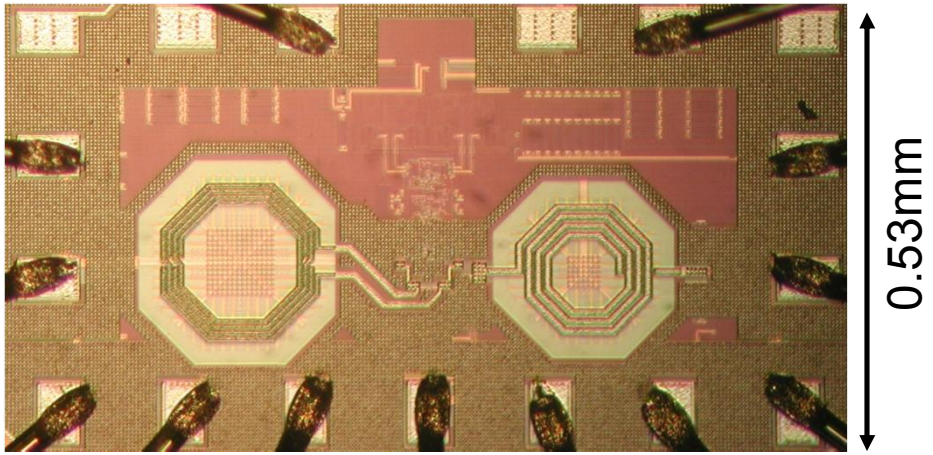
LO generation (VCO, active-PPF, 3/2 divider)

with M. Törmänen and A. Axholt

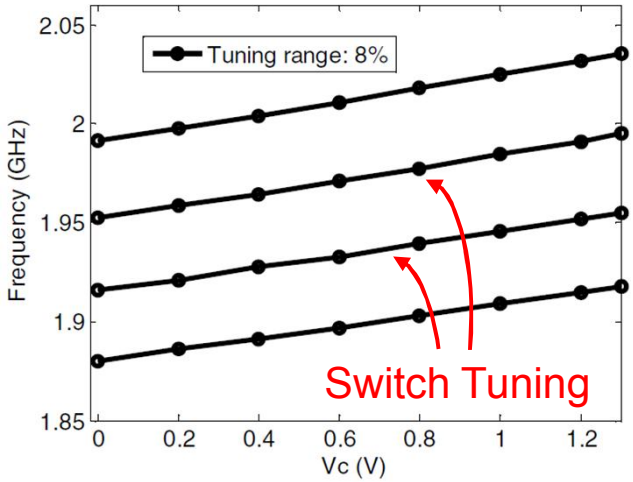
Reduces VCO pulling from PA

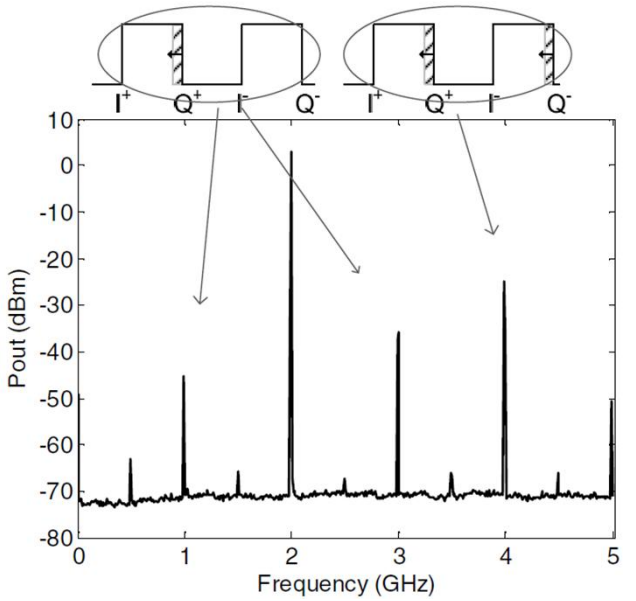


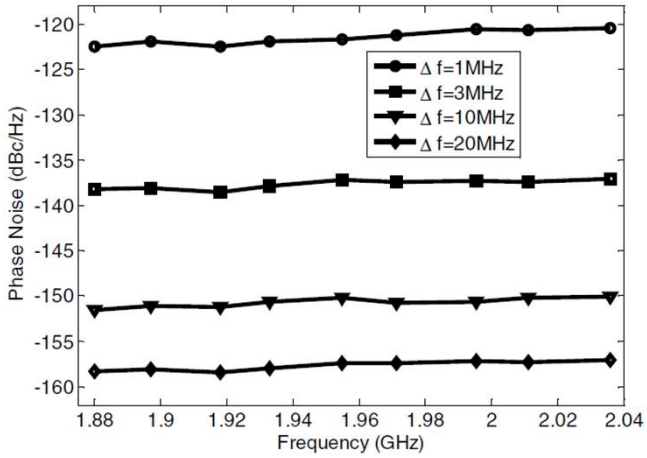
30mW Power Consumption

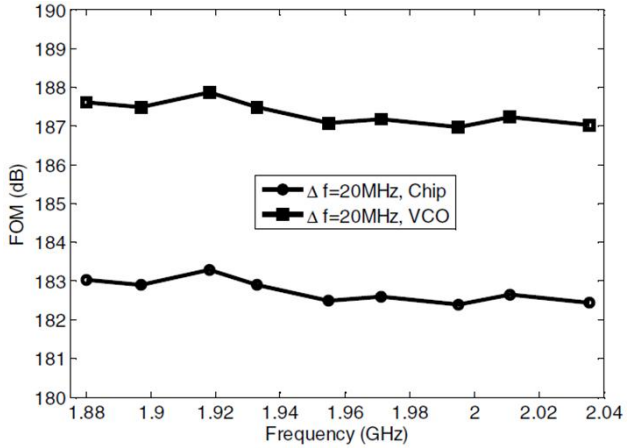


LO generation – performance



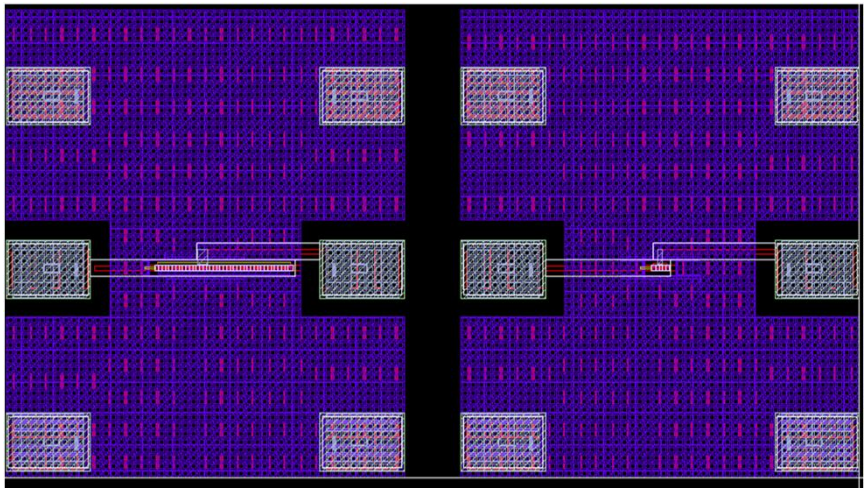






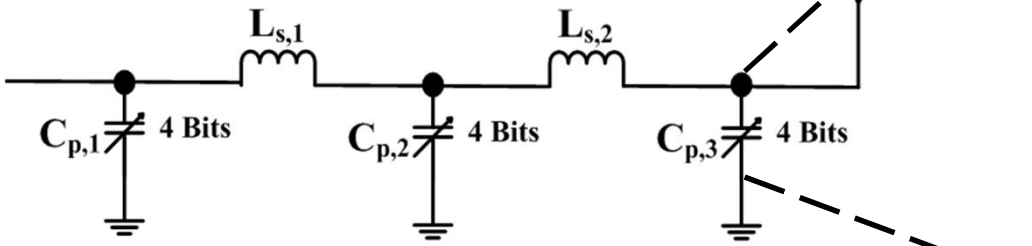
Models for ED-MOS in STM 65nm CMOS

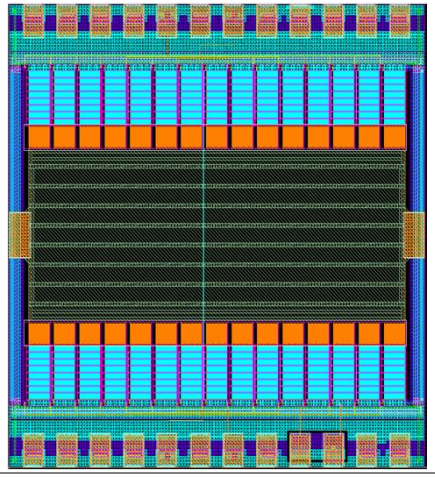
- Increase PA output power
  - Use ED-MOS transistors with high breakdown voltage
- No real RF model is supplied from CMP
- We will build our own RF MOS model
- Together with Prof. Christian Fager at Chalmers



700-900MHz Impedance Tuner in STM 65nm CMOS-SOI

- Compensate for the antenna mismatch
  - Up to a VSWR of 4.5
- Low insertion loss (IL)
  - Less then 1dB with off-chip inductor Q of 50 for $L_{s,1}$ and $L_{s,2}$
- 4-bit switched capacitor banks ($C_{p,1}$, $C_{p,2}$, $C_{p,3}$)
  - Can handle 30dBm of TX power at an antenna VSWR of 4
- Taped-Out in June 2012
  - Still waiting for fabrication…



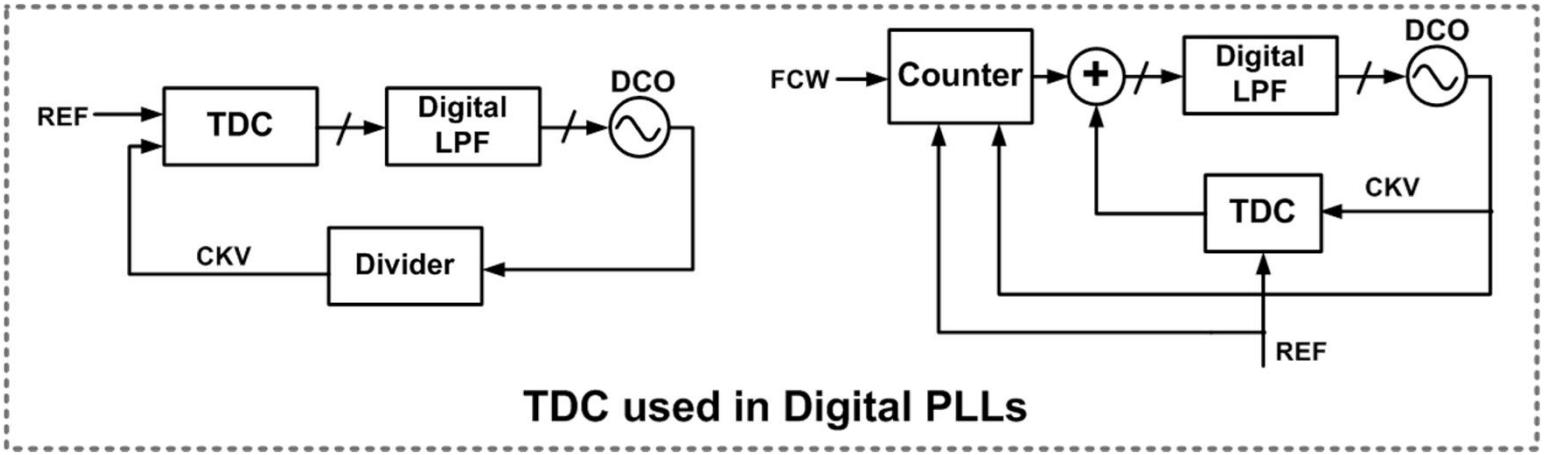


1x1mm^2

Time-to-digital converter (VR, SSF DARE, EU Marie Curie)

Ping Lu

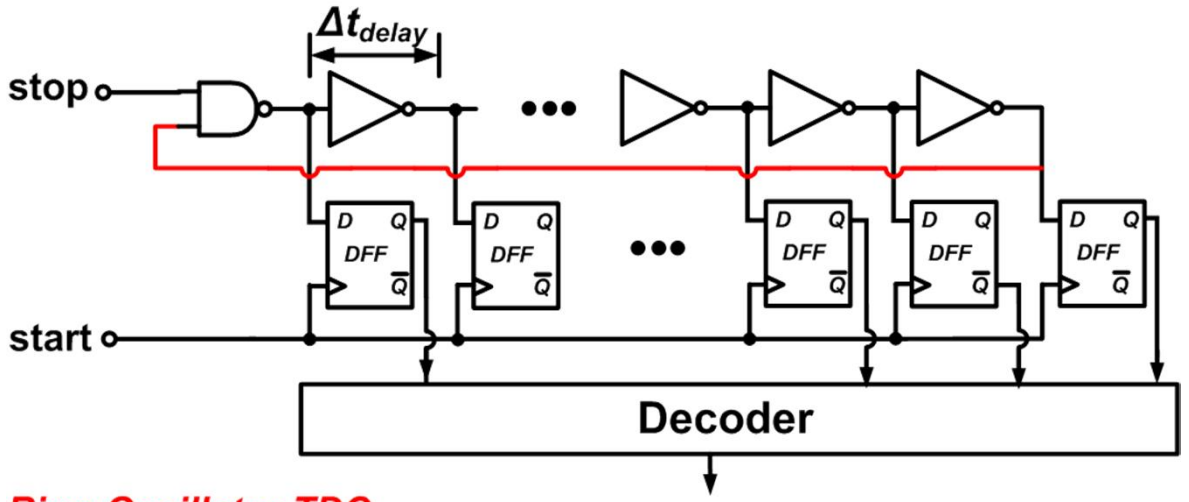
- TDC in digital PLL replaces phase-frequency detector of analog PLL



- Smaller TDC-cell delay (Δt_{delay}) → lower in-band PLL noise

Ring-oscillator TDC

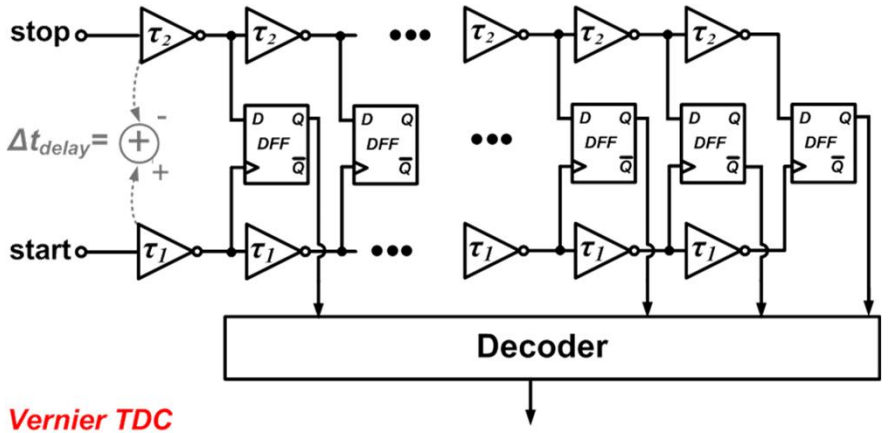
- Ring-Oscillator TDC → large detection range with few stages



Ring-Oscillator TDC

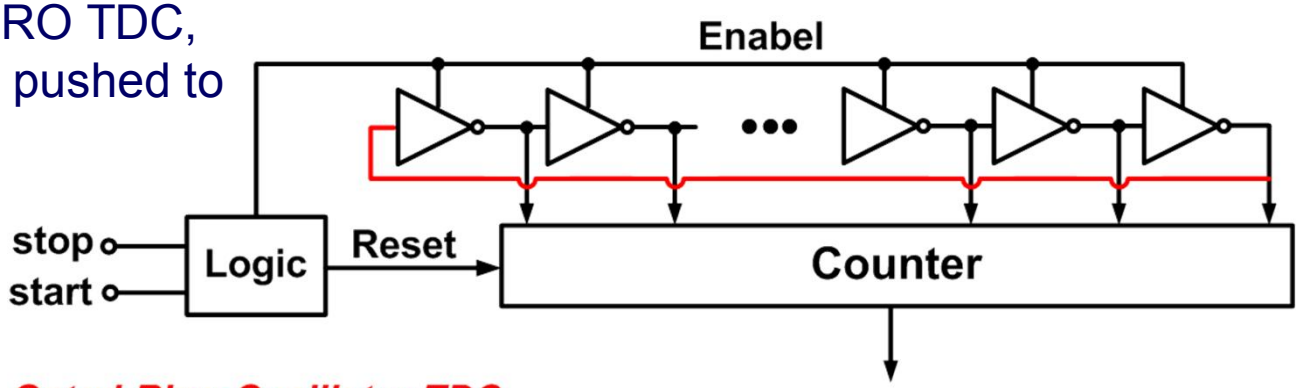
Varnier TDC and GRO TDC

- Vernier TDC → τ_1-τ_2 = Δt_{delay} < τ_1 (τ_2)
  - However, a very large number of stages are required



Vernier TDC

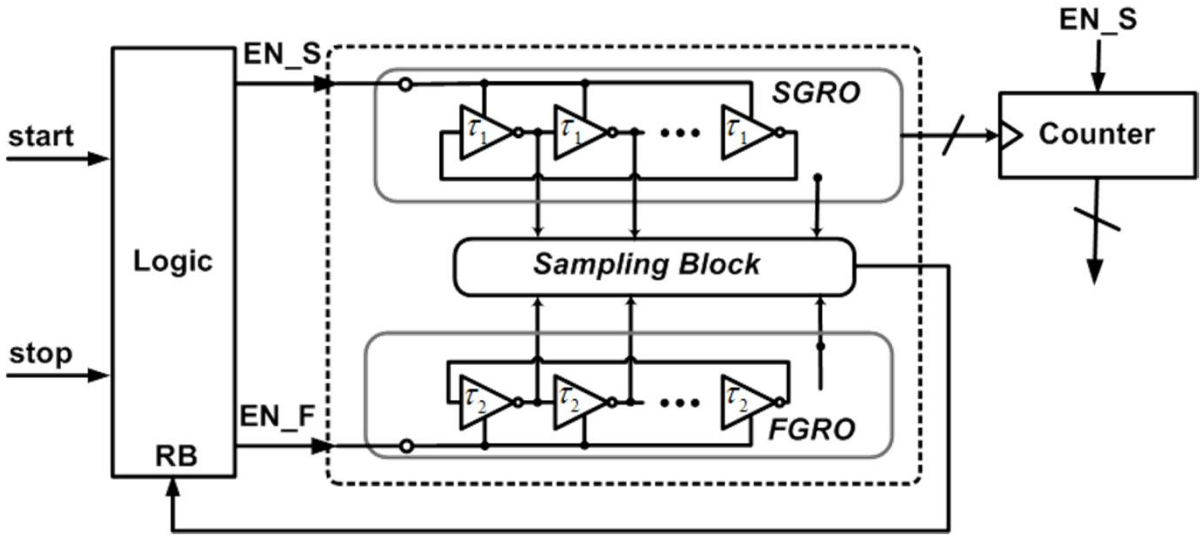
- Ring-Oscillator (RO) TDC → large detection range with few stages
- ✓ Gated-RO TDC → ar RO TDC, with quantization noise pushed to high frequencies



Gated-Ring-Oscillator TDC

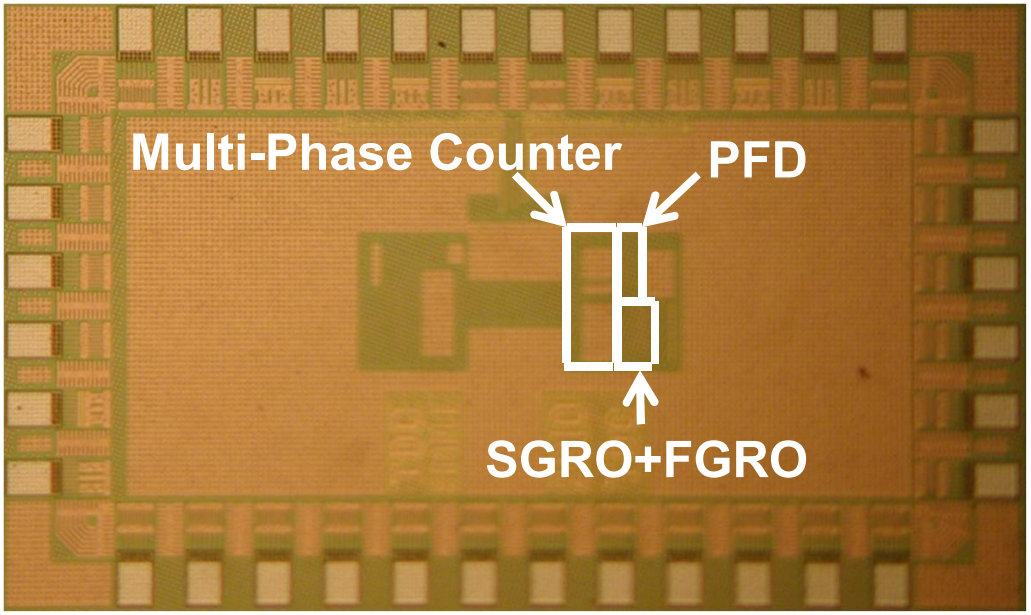
Vernier + gated ring oscillator

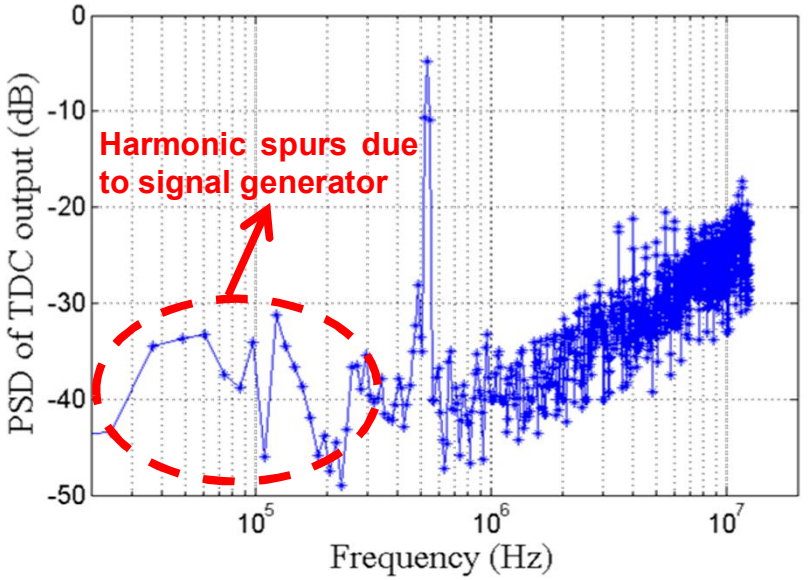
- New TDC → combines Vernier + GRO



High Vernier time resolution + First-order noise shaping

Chip photograph and results of VGRO TDC



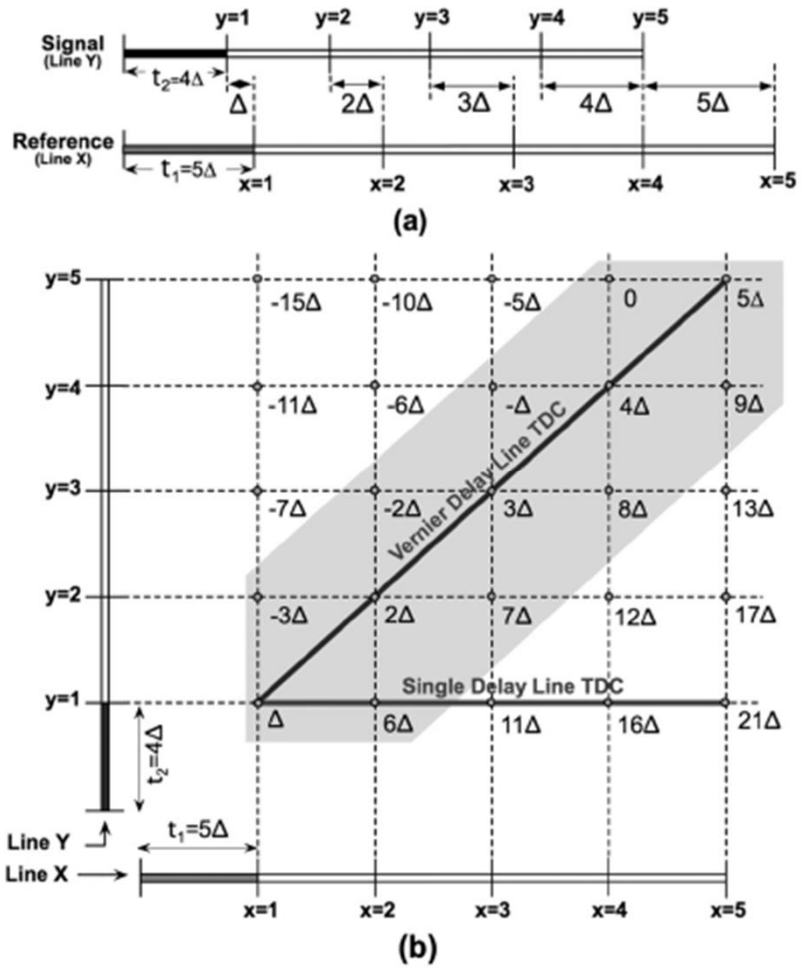


Area	**0.027mm^2**
Process	**90nm CMOS**
Current (Supply)	**3mA (1.2V)**
Vernier resolution	**~5ps**
Effective in-band resolution (OSR= 16)	**~3ps**

Presented at ESSCIRC 2011

Invited and published in JSSC July 2012

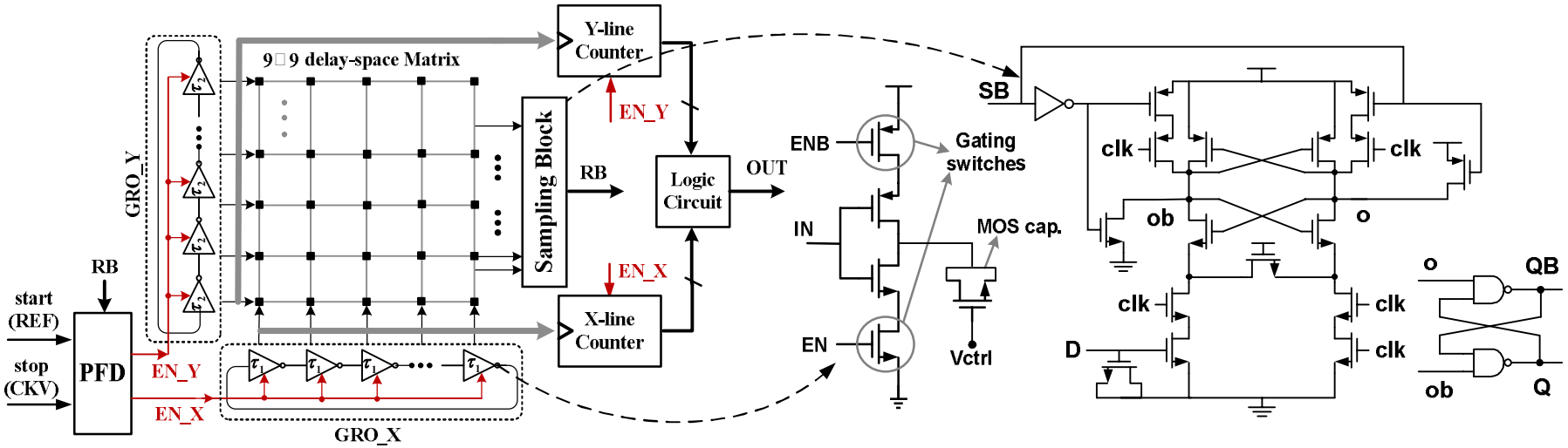
Two-dimensional VGRO TDC



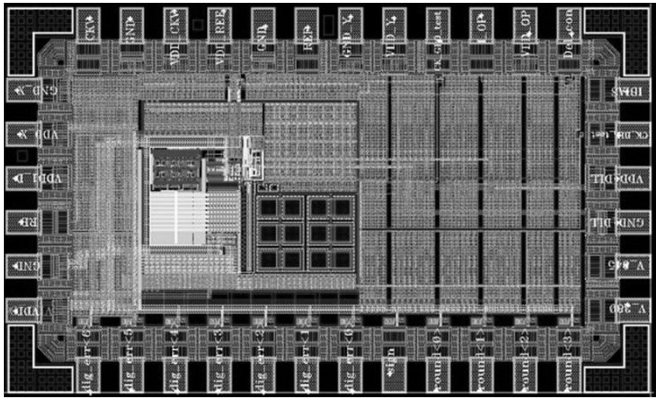
- Developed from VGRO TDC and 2-D Vernier (Univ. of Pavia, Italy)
- Many more signal pairs used than in 1-D VRGO TDC → enhanced detection range
- Reduce latency time
- Under measurement, to be presented at NORCHIP 2012

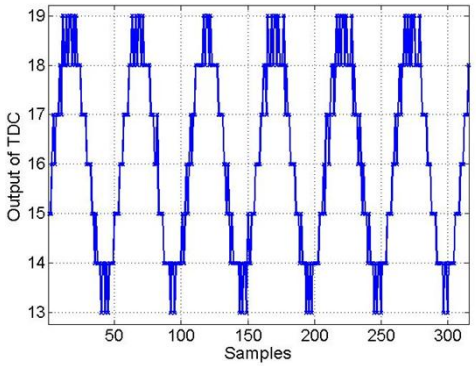
Vercesi et al, JSSC Aug. 2012

Chip photo and simulations

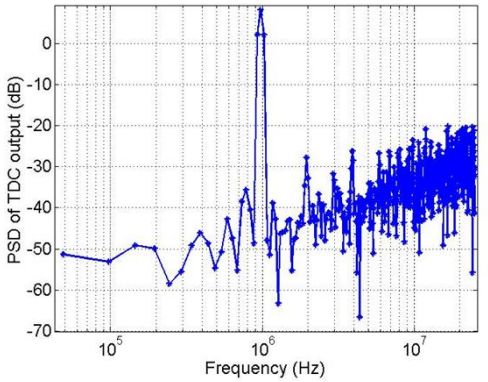


GRO based 2-D Vernier TDC implementation





Transient output



PSD of TDC output

SCANDINAVIAN EXCELLENCE DEFINED IN LUND

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