Low Phase Noise 3.4-4.5GHz Dynamic-Bias Class-C CMOS VCOs with a FoM of 191dBc/Hz

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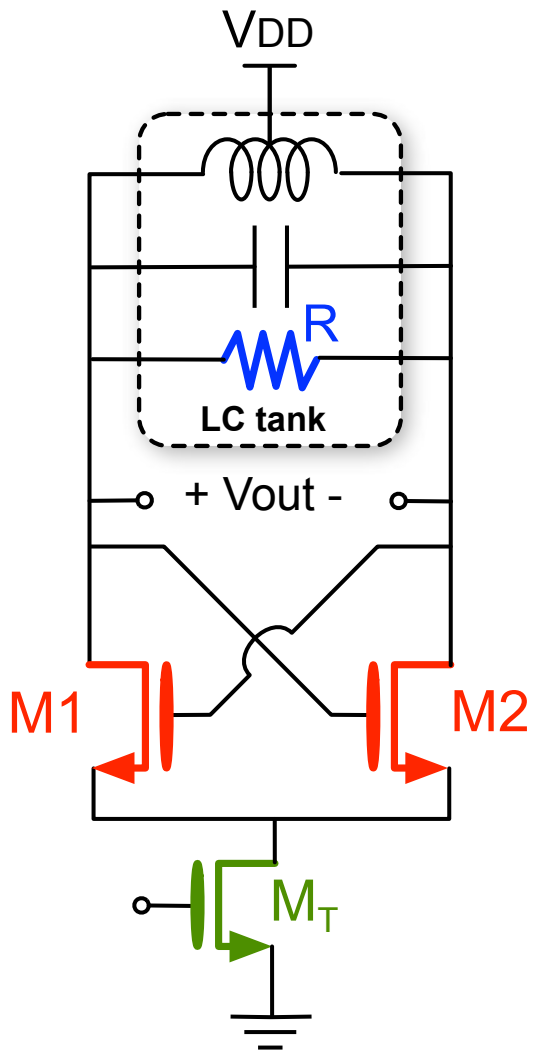
Class-B VCO



Andreani et al. [JSSC '05]

Phase noise of class-B oscillator:

$$L(\Delta\omega) = 10\log\left[\frac{\kappa_B T R \omega_0^2}{4A^2 Q^2 \Delta\omega^2}\left(\gamma + 1 + \eta\gamma g_{mT} R\right)\right]$$

VCO swing $\propto I_{bias}$ — Tank quality factor

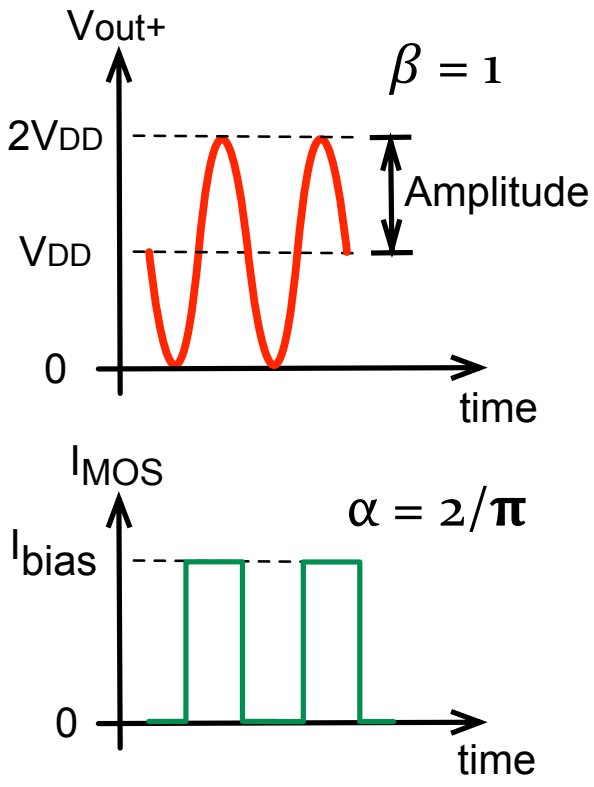
The resulting FoM is:

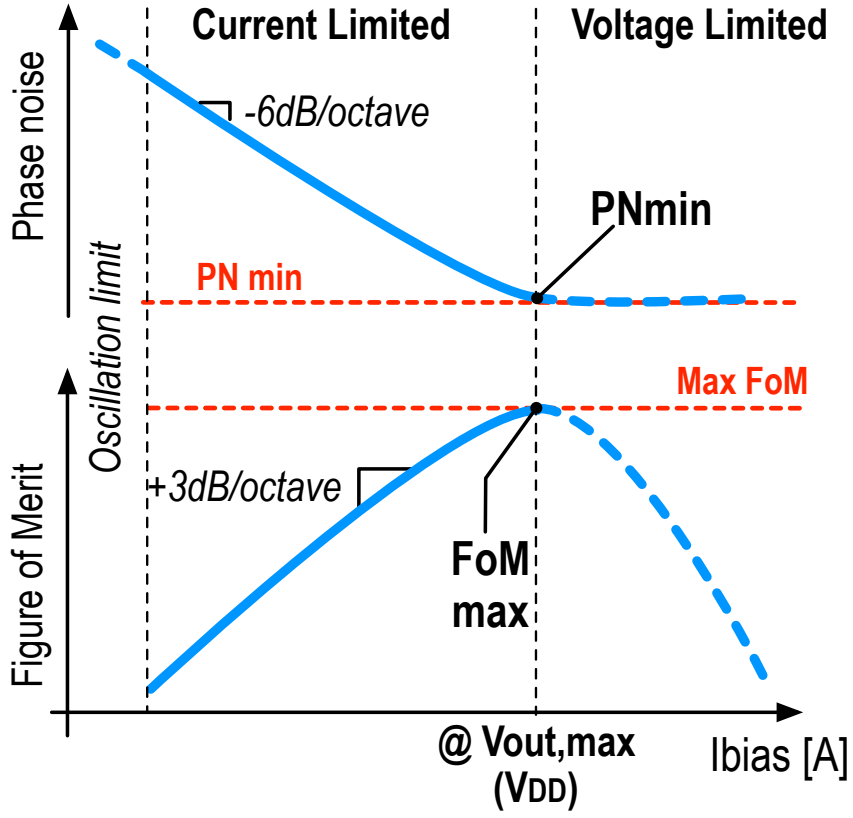
$$FoM = -10\log\left[\frac{10^3 \kappa_B T}{2Q^2 \alpha\beta}\left(\gamma + 1 + \gamma g_{mT} R\right)\right]$$

current efficiency = $\frac{I_{\omega_0}}{I_{bias}}$ — voltage efficiency = $\frac{A}{V_{DD}}$

Ideal performance

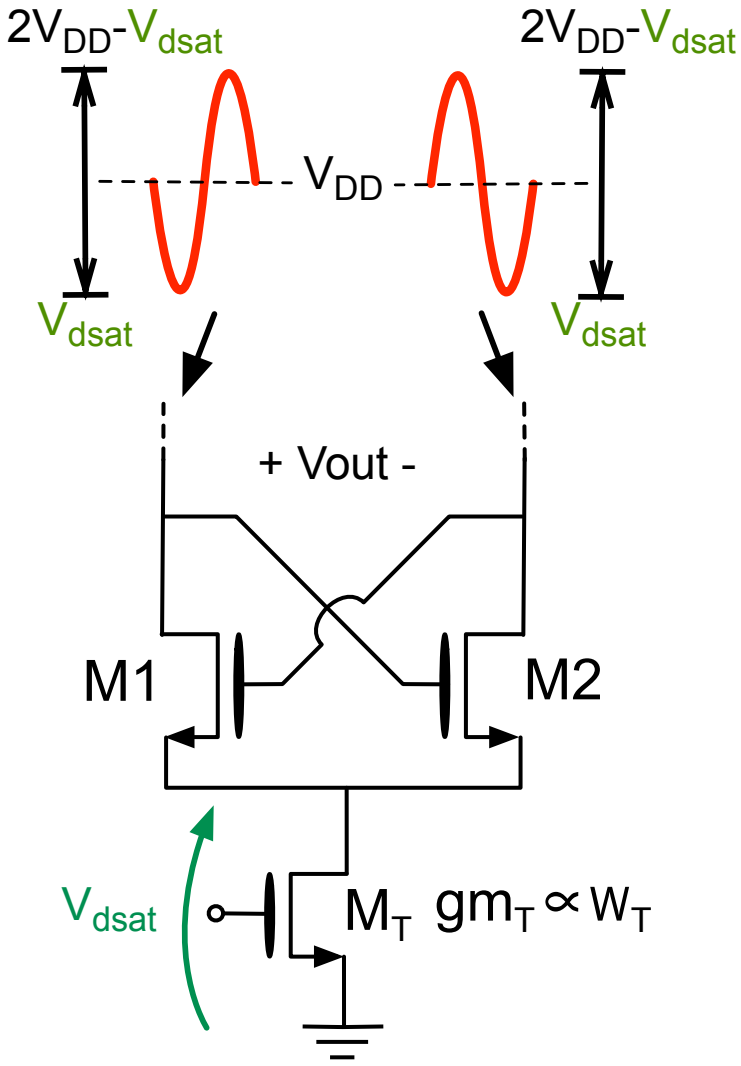
Ideal class-B → $A = V_{DD}$ → $\alpha = 2/\pi$, $\beta = 1$ → Best phase noise and FoM





With Q_t= 13, the Class-B oscillator has an ideal maximum FoM of 194dBc/Hz

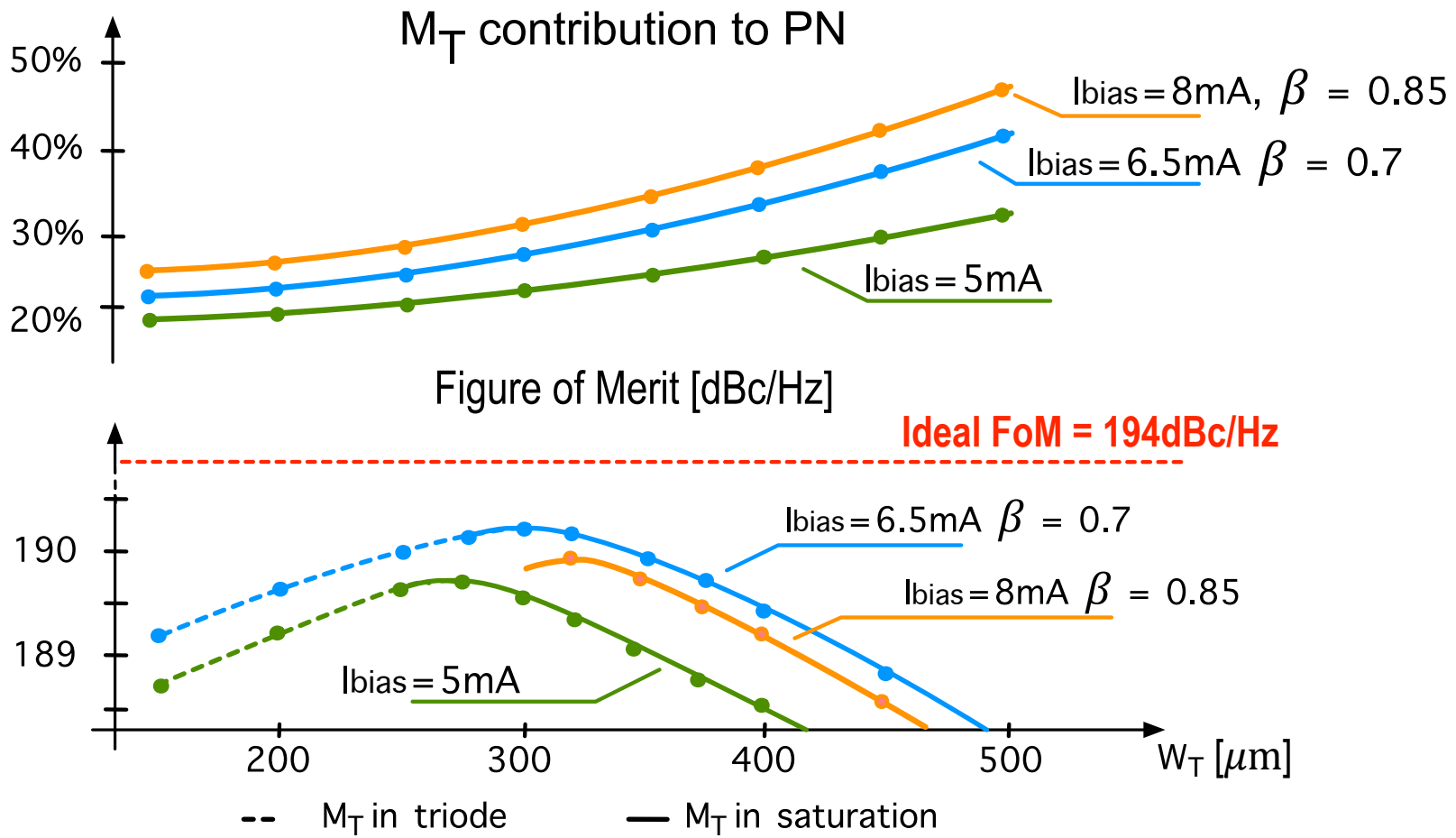
Noise vs. Amplitude



- Maximum amplitude is **limited** by $\mathbf{V_{dsat}}$
- β in VCOs for cellular applications has typical values of **0.8-0.6**, **degrading** the **FoM** by **1.5-2dB**
- $\mathbf{V_{dsat}}$ could be minimized increasing the width W_T of M_T

Bias noise vs. FoM

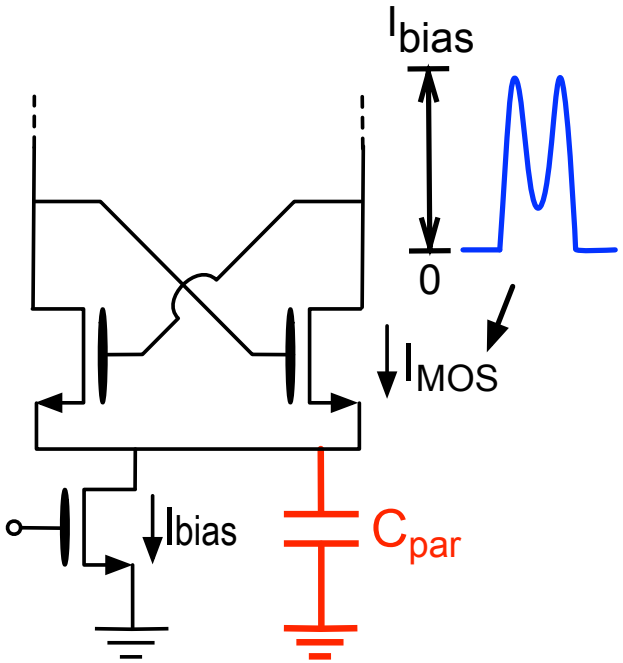
A large W_T increases the transconductance of M_T, and its noise as well

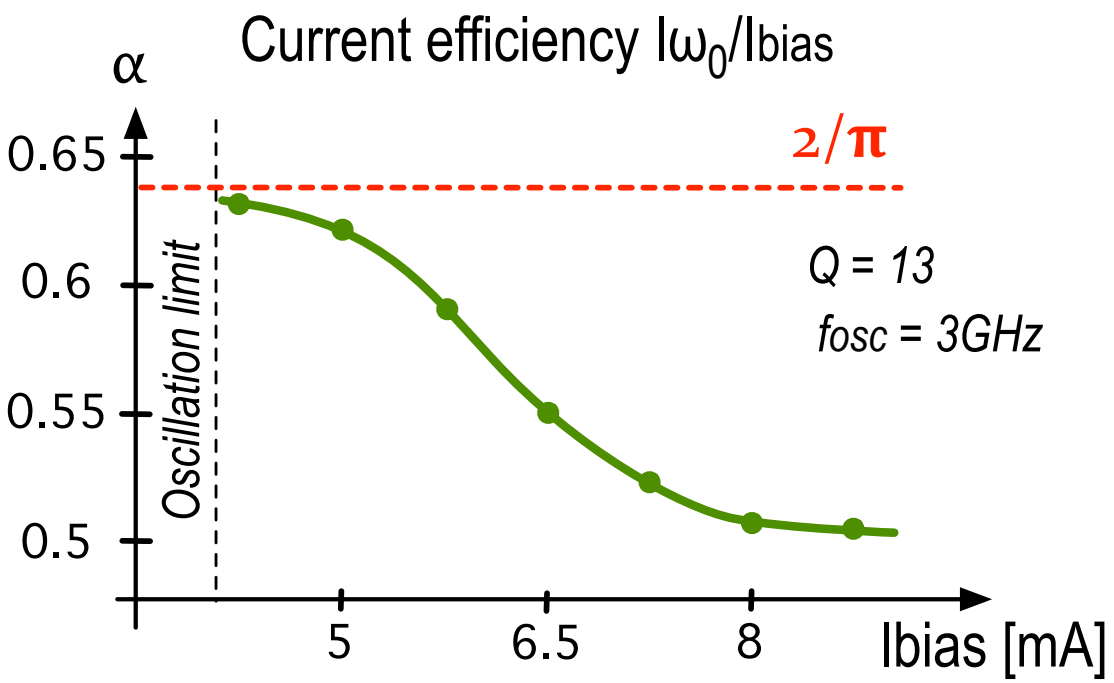


A M_T contribution of 25-30% reduces the FoM by 1.3-1.5dB

Current efficiency

Parasitic capacitance C_{par} reduces the current efficiency α when the switching pair works in the linear region

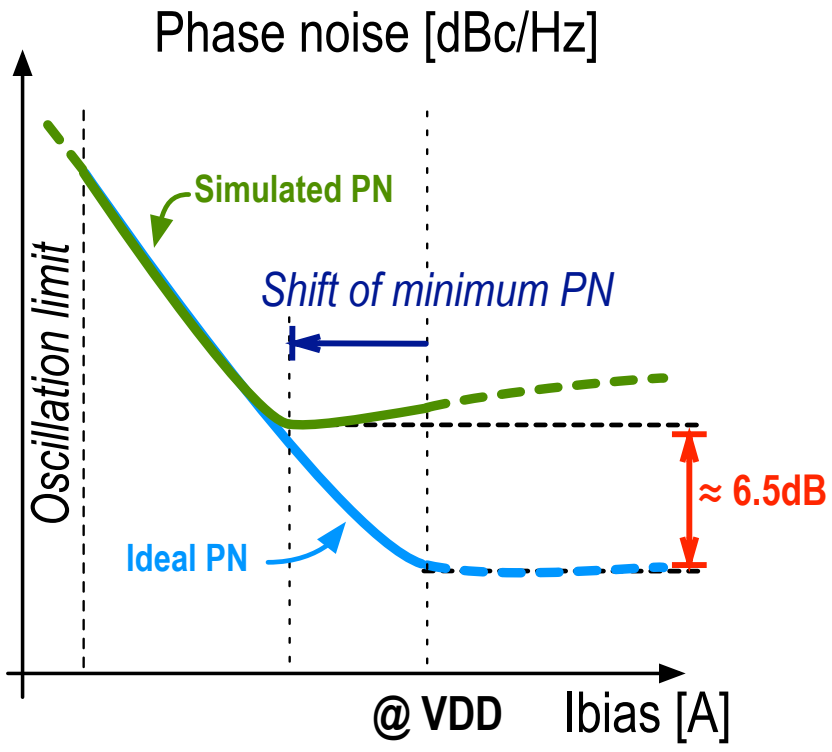


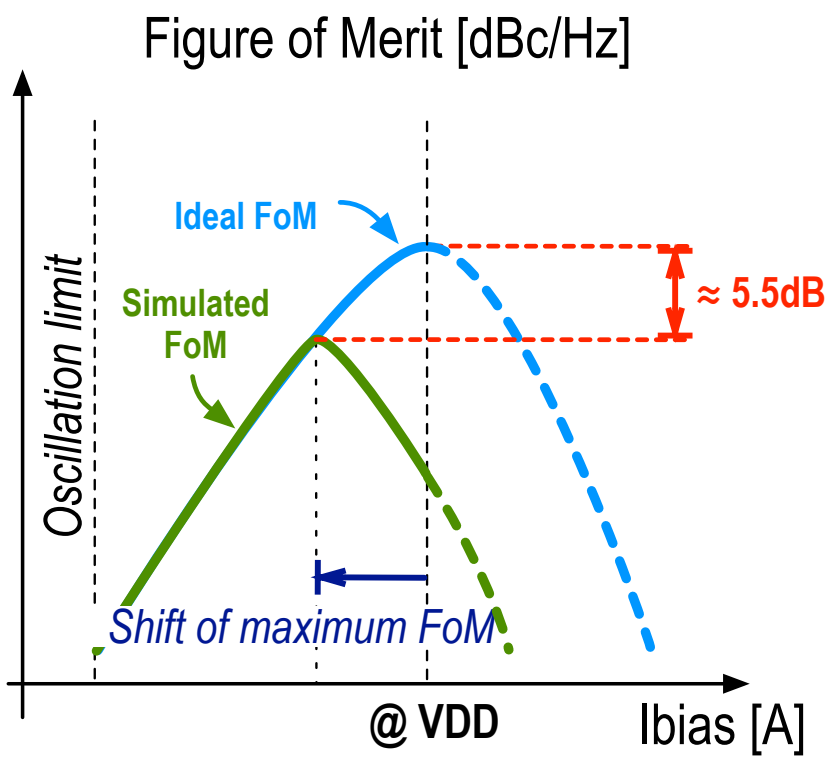


α = 0.55 deteriorates FoM by another **0.7dB**

Real vs. Ideal class-B VCO

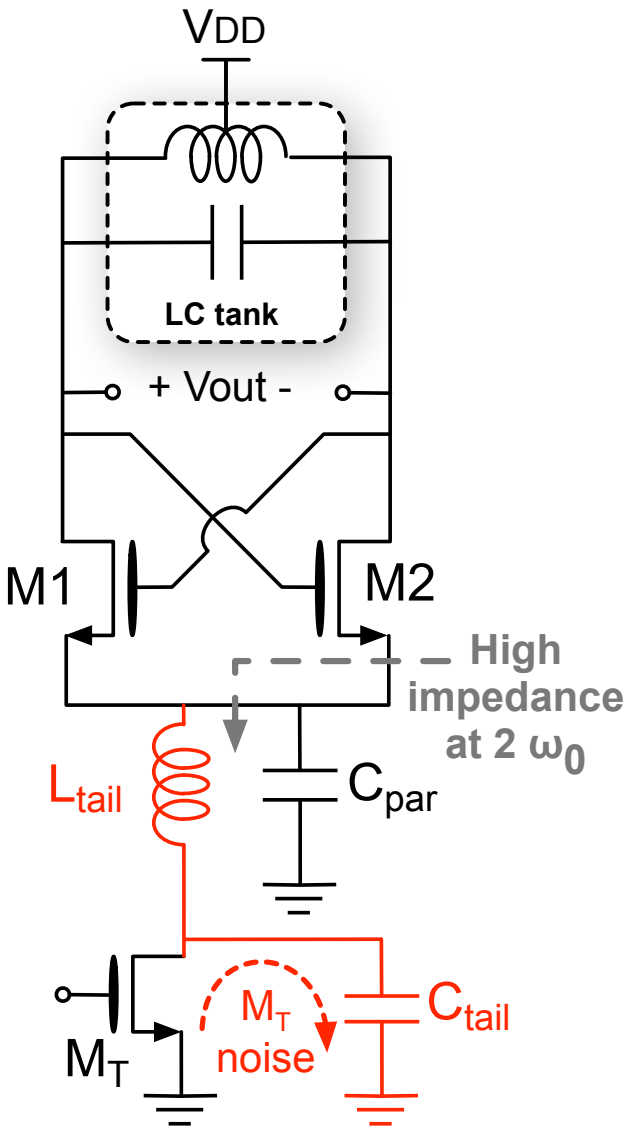
The tank non-linear capacitances (tuning range of 30%) affects FoM by 0.5-1dB





Best real FoM of class-B VCOs is several lower than the ideal one.

Possible solution – Noise filter

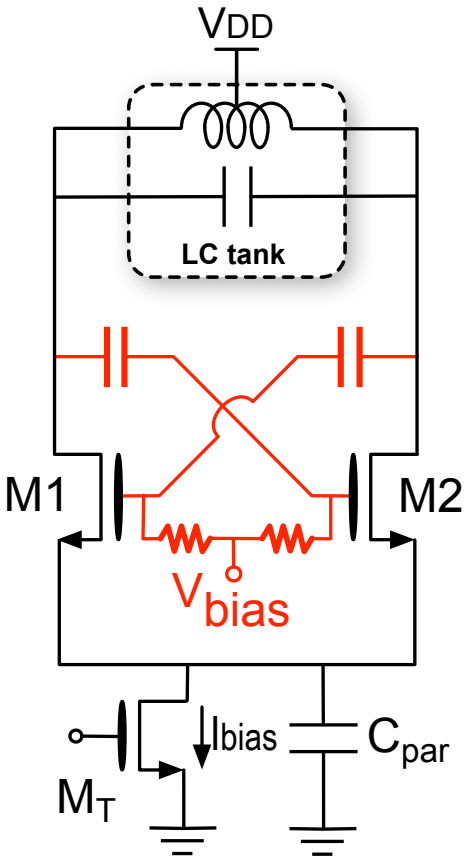


- L_{tail} resonates at $2\omega_0$ with C_{par}, increasing the impedance and the current efficiency
- The large C_{tail} filters M_T noise
- L_{tail} increases the VCO area
- Tunable L_{tail} is required when VCO has a large tuning range

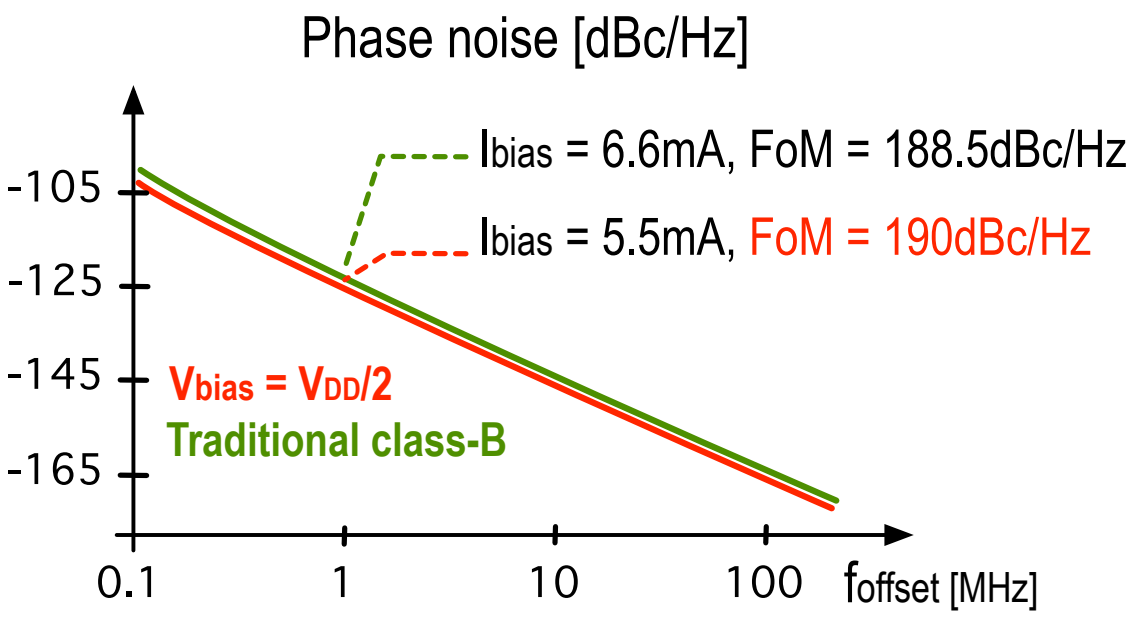
Hegazi et al. [JSSC '01]

Class-B VCO with low V_{gate}

A low V_{bias} keeps the MOS pair out of the linear region, improving current efficiency



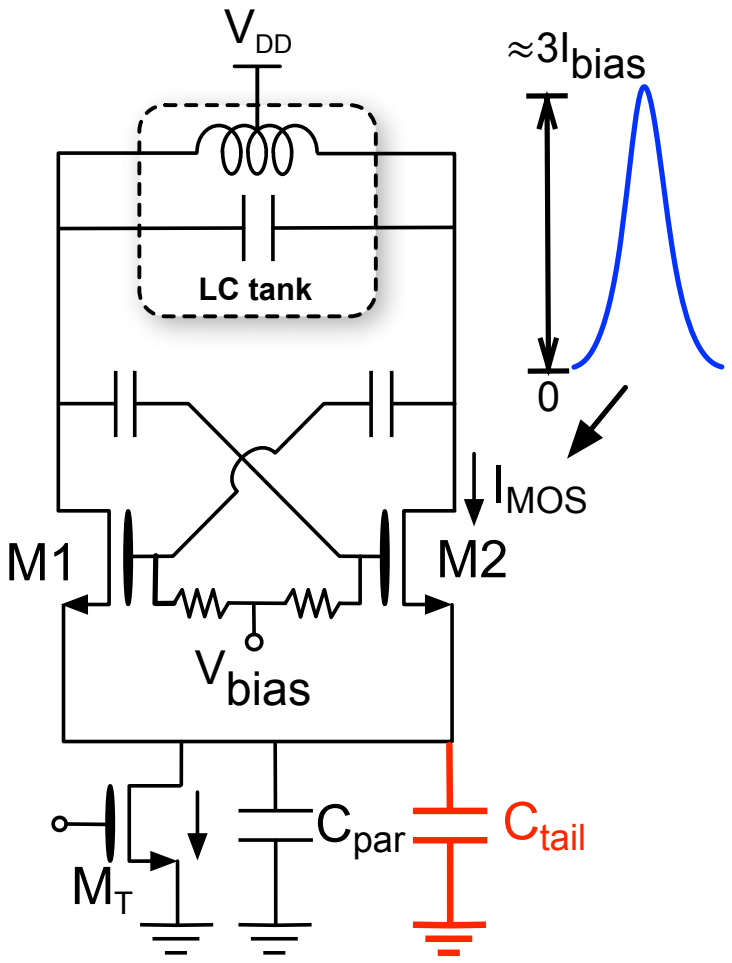
$$2/\pi < \alpha < 1$$



Simulations with f_{osc}=3GHz and Q_{tank}=13

FoM improvement of 1.5dB compared to traditional class-B

Class-C VCO



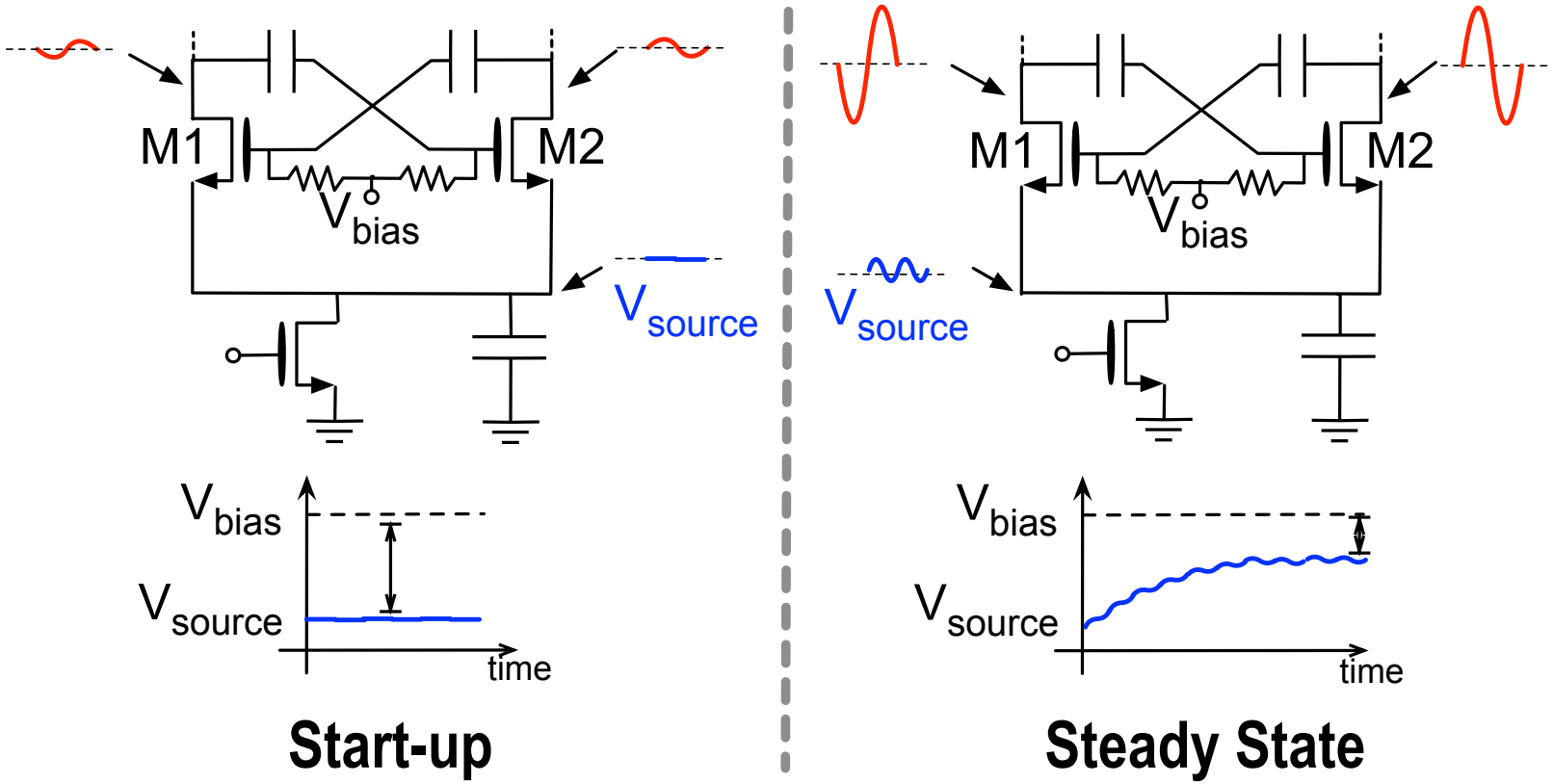
- The current efficiency $\alpha \approx 1$
- C_{tail} filters out current source noise
- M_T size are optimized to reduce V_{dsat} maximizing amplitude
- Simulations shows **FoM improvement by another 1dB** compared to class-B low V_{bias}

$$C_{par} + C_{tail} = 2C_{tank}$$

Mazzanti and Andreani [JSSC '08]

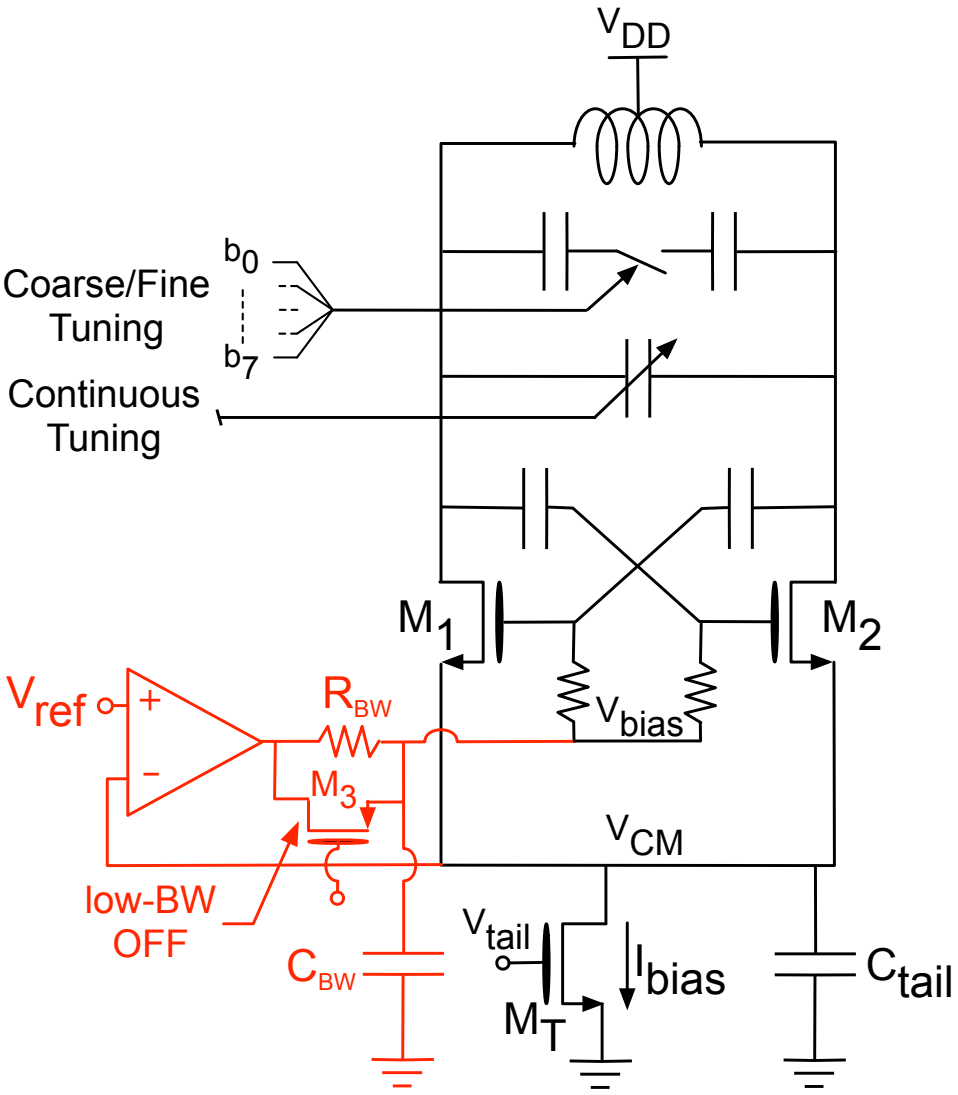
Start-up vs. steady state

The maximum amplitude increases reducing V_{bias}



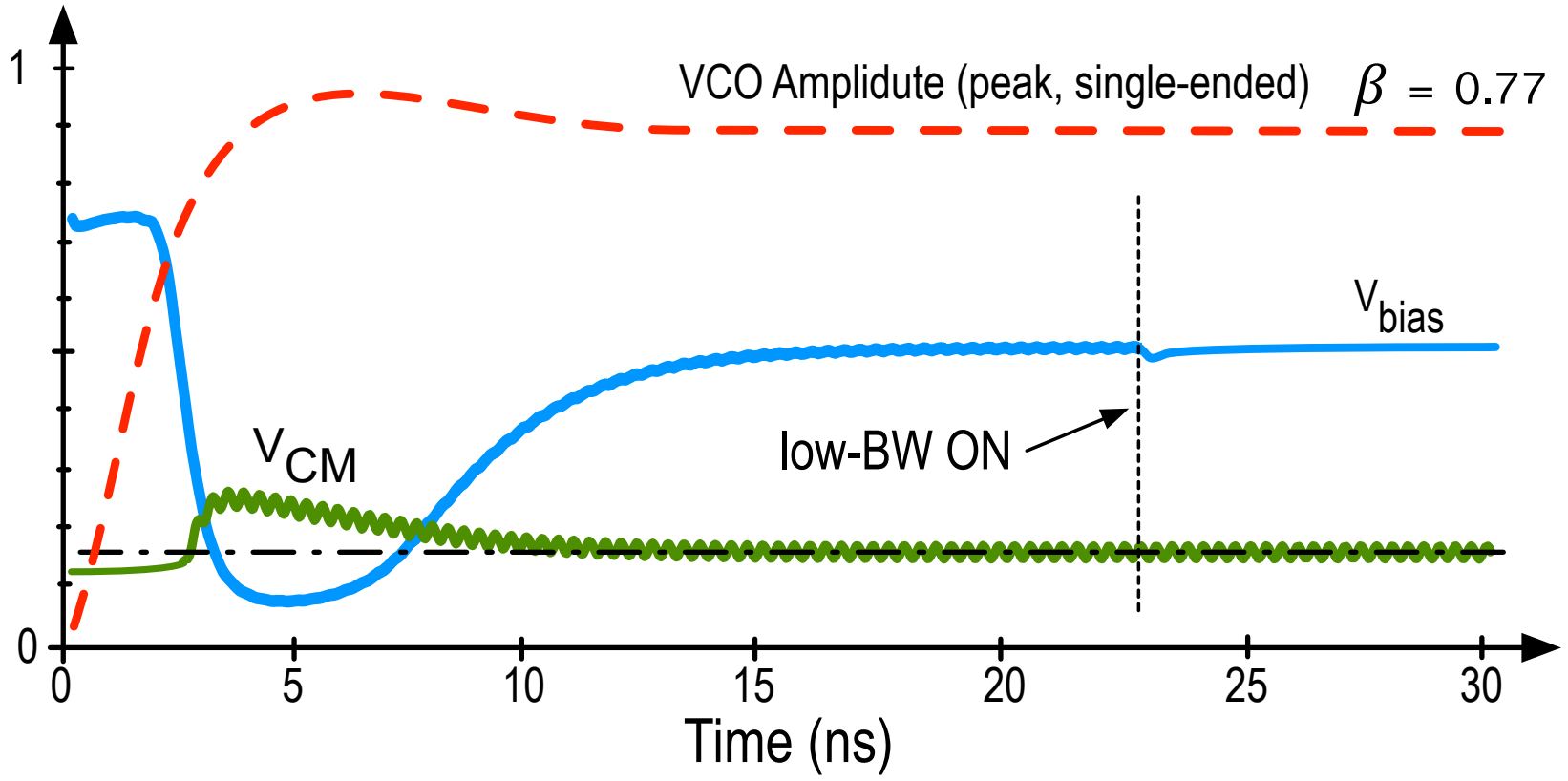
The start-up condition **limits** the lower value of $\mathbf{V_{bias}}$

Dynamic-bias class-C VCO



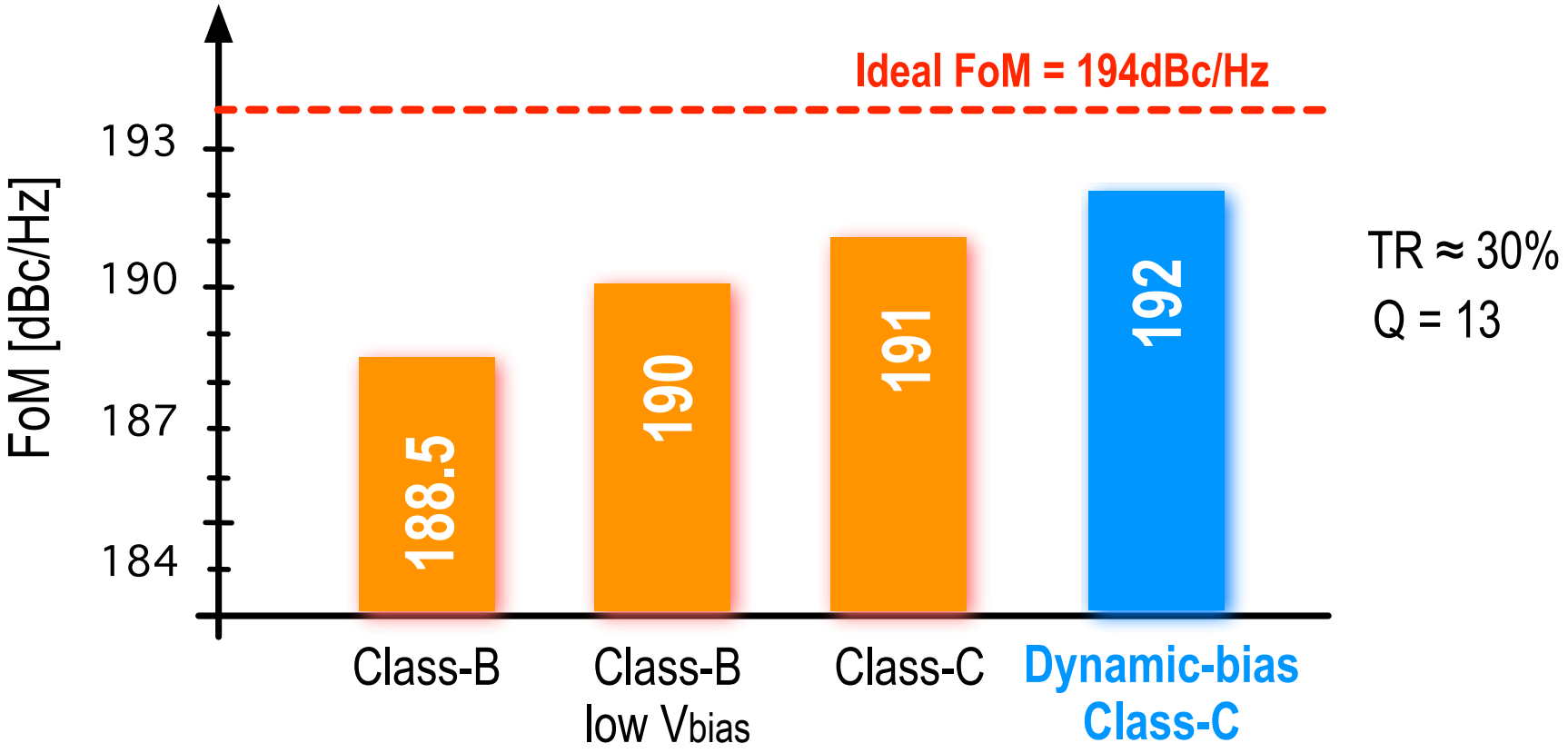
- Feedback keeps constant voltage drop across M_{tail} both during start-up and steady state
- The opamp has a minor impact on phase noise if the VCO works in class-C
- M_3 changes the bandwidth of the feedback loop

Transient waveforms

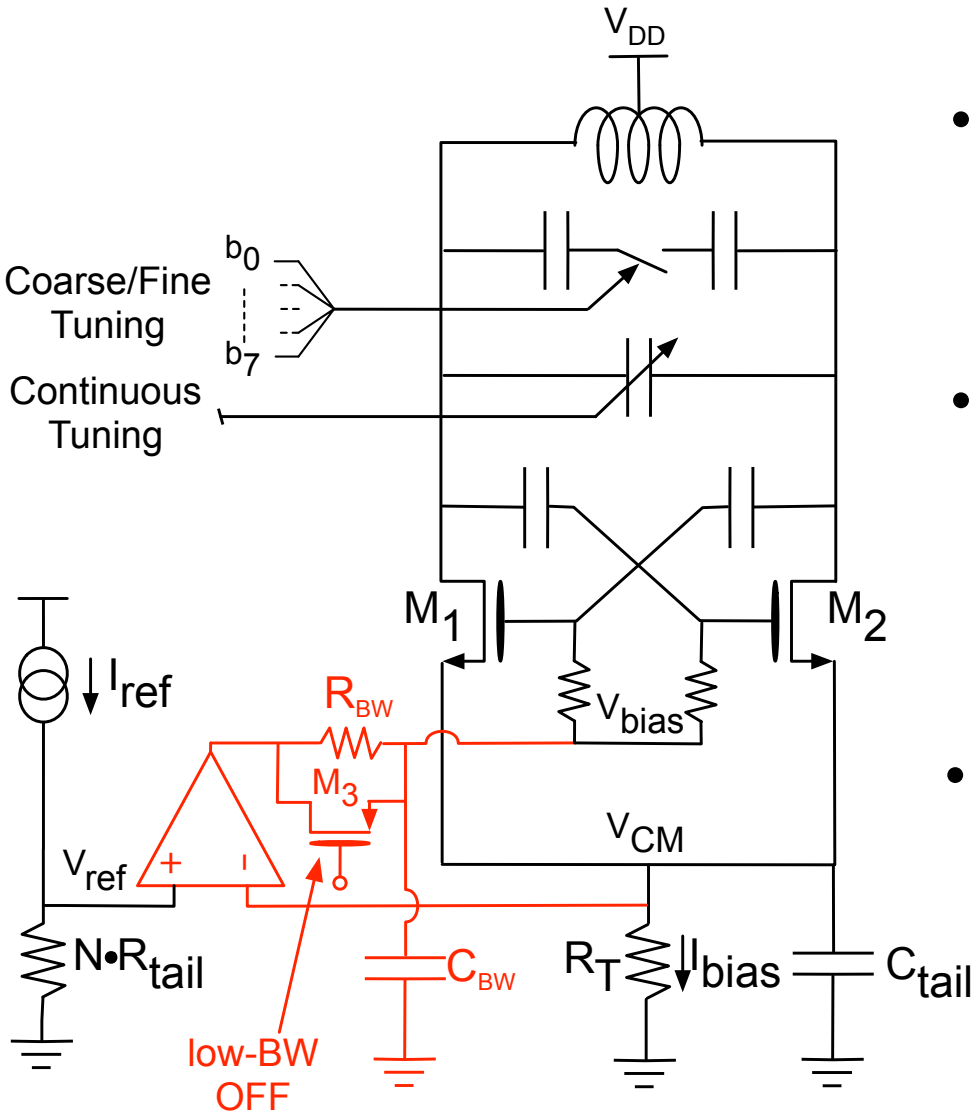


The low feedback-generated V_{bias} maximizes the oscillation amplitude, optimizing the phase noise performance

From class-B to dynamic-bias class-C

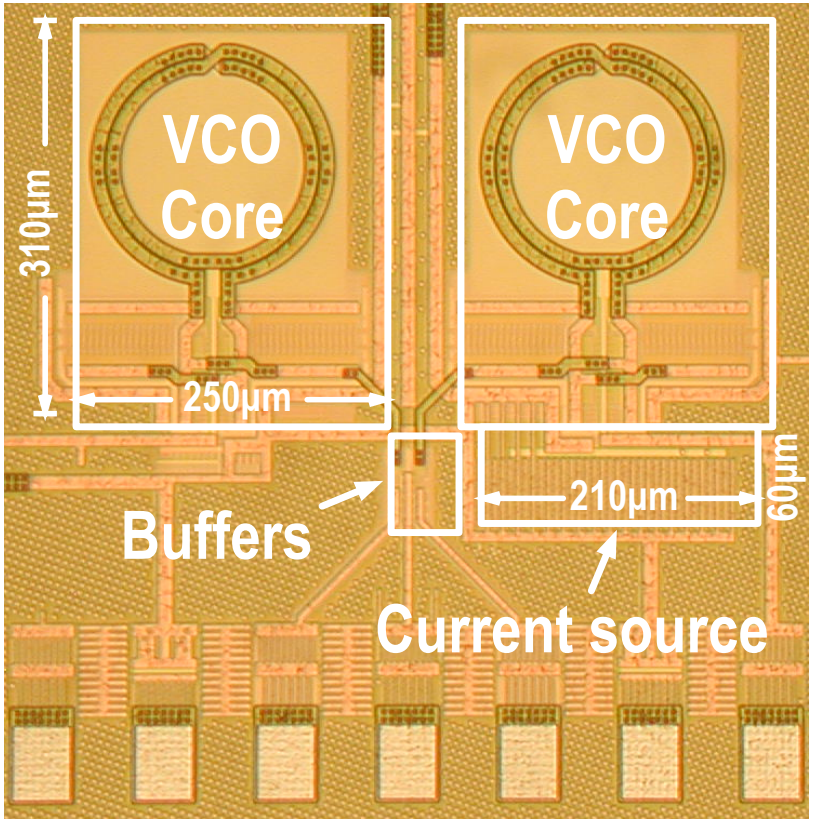


Dynamic-bias class-C with tail resistor



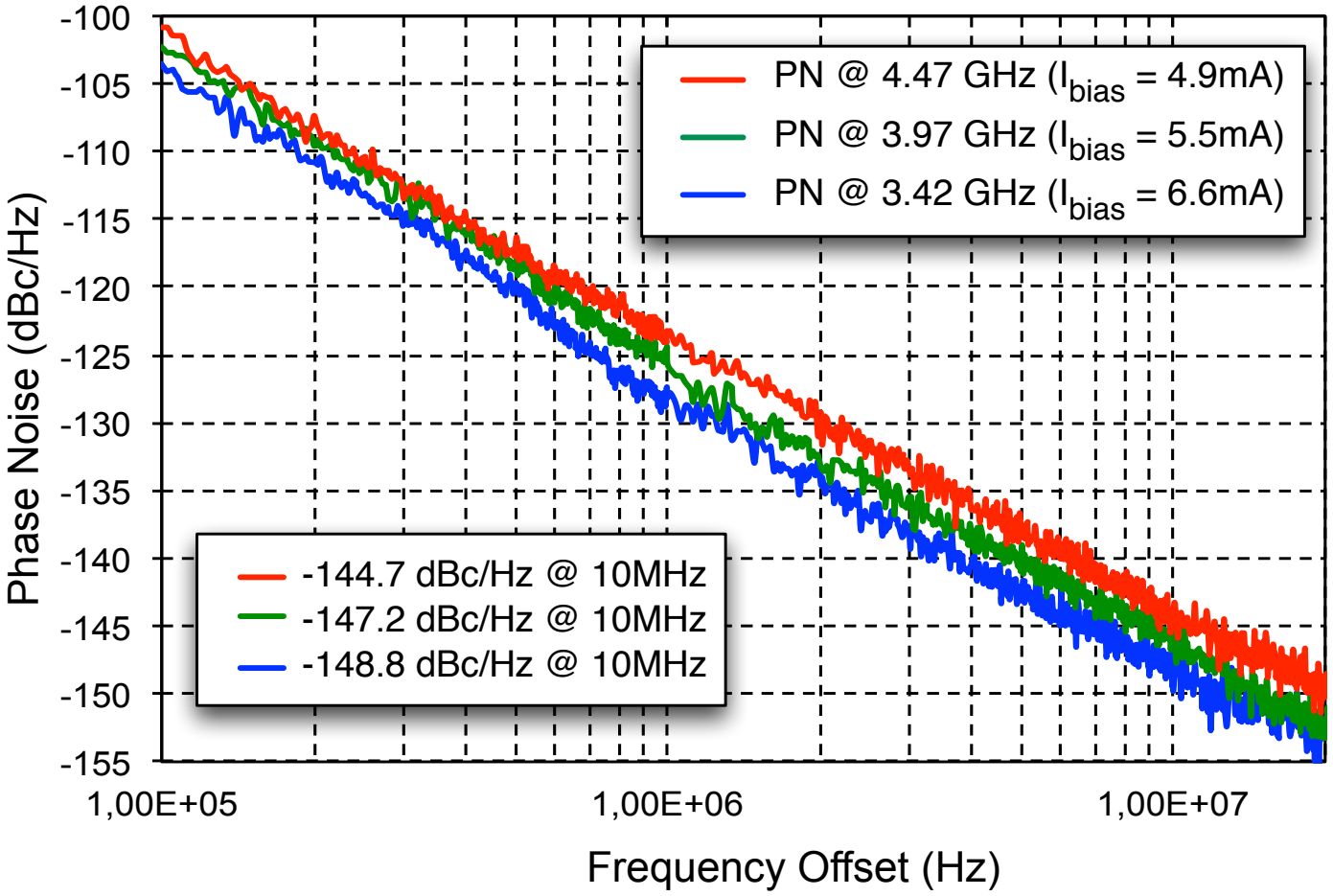
- Feedback sets the bias current equal to V_{ref} / R_T
- The absence of a current source saves area and eliminates an important 1/f noise source
- The low impedance R_T slightly increases the impact of opamp noise and M_1-M_2 1/f noise

Chip photograph



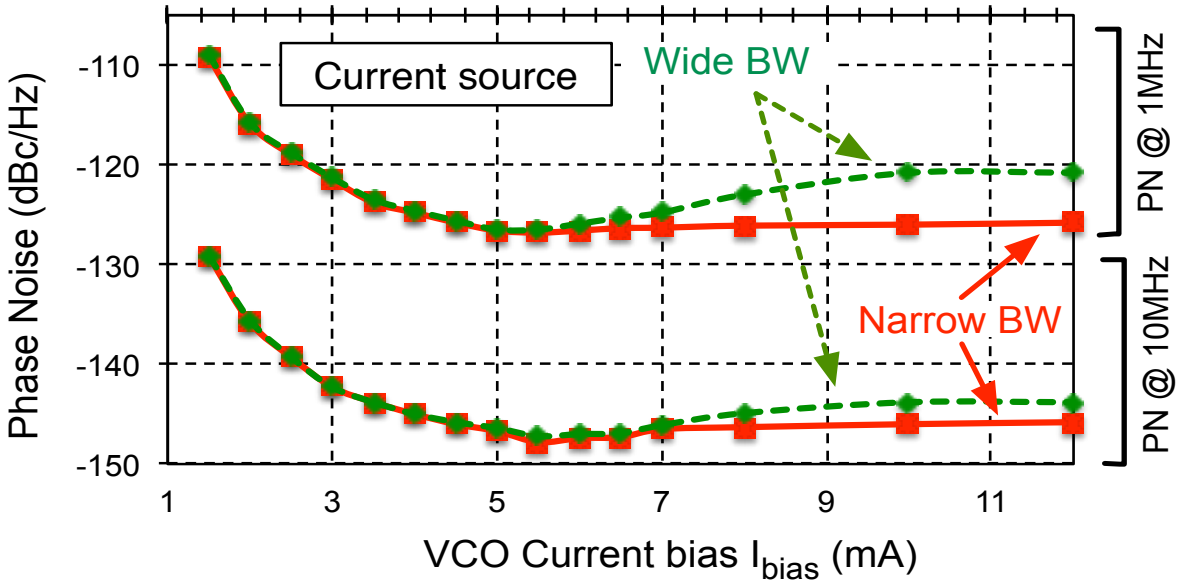
- 90nm CMOS process with thick top metal
- Inductor: 1nH with Q = 17 @ 4GHz
- Tank: $Q_{tank} \approx 13$ along all tuning range between 3.4GHz and 4.5GHz (28%)
- 0.065mm^2 active area for tail-resistor VCO
- 0.078mm^2 for tail-current-source VCO
- Voltage supply: 1.2V

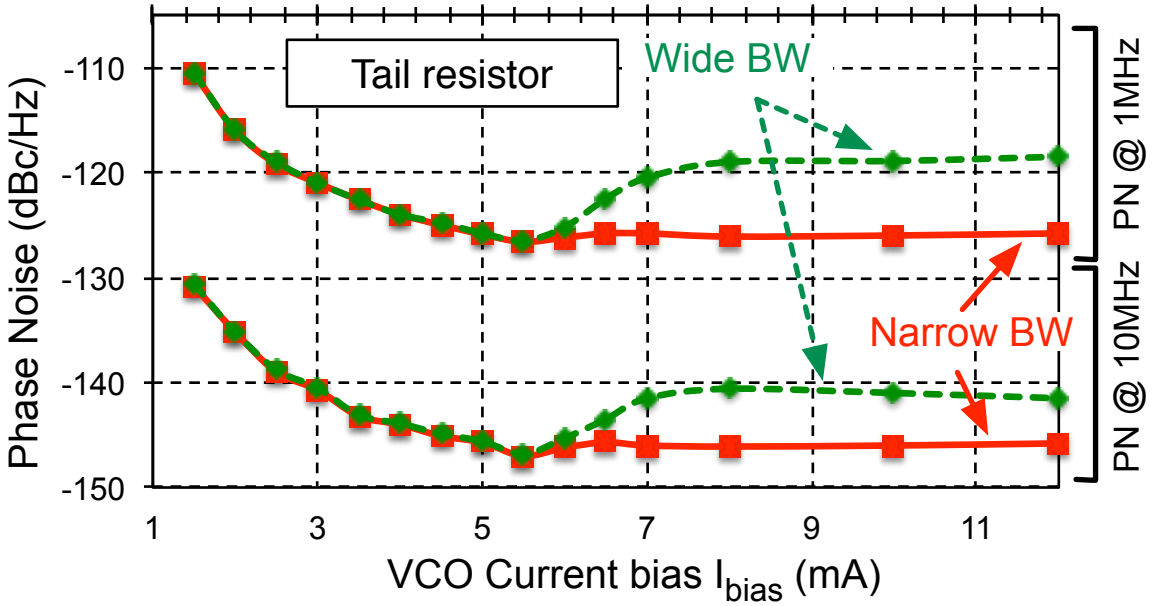
Phase noise



With I_{bias} = 5.5mA, FoM = 191dBc/Hz

Phase Noise vs. I_{bias}





The narrow loop bandwidth filters the opamp noise when the VCO starts working in class-B

The low impedance at the switching pair source increases the opamp noise

State of the art

	Area (mm^2) (Tech.)	Frequency (GHz)	Phase Noise (dBc/Hz)	PDC (mW)	FoM (dBc/Hz)
Fanori *ISSCC12*	0.39 (55nm)	6.7-9.2 (32%)	-137 @ 2MHz (a)	27	188/189
Andreani *JSSC11*	(90nm RF)	2.6-4.1 (46%)	-156 @ 20MHz	22.8	188
Liscidini *ISSCC12*	0.49 (55nm)	6.5-9.0 (33%)	-135 @ 2MHz (a)	36	185
Hung *JSSC06*	0.44 (90nm)	3.3-4.0 (19%)	-149 @ 3MHz (b)	25.2	186
Dal Toso *JSSC10*	0.06 (65nm)	13-15 (15%)	-133 @ 3MHz (b)	8.4	185
Visweswaran *ISSCC12*	0.19 (65nm)	7.3-8.0 (10%)	-142 @ 3MHz (a)	25.8	190
Ruippo *MWCL10*	0.37 (130nm)	2.9-5.4 (60%)	-126 @ 1MHz	13.5	185/190
Li JSSC2012	0.29 (65nm)	2.5-5.6 (76%)	-157 @ 20MHz	9.8	188/192
This work	**0.08/0.09 (90nm)**	**3.4-4.5 (28%)**	**-147 @ 10MHz**	**6.6**	**191**

(a) After divider by 2 (b) After divider by 4

Conclusions

- Cellular TX demands a low phase noise with a low power consumption
- Dynamic-bias class-C VCO exhibits the best performance compare the other topologies, close to the theoretical maximum class-B FoM
- Measurements on a 90nm CMOS prototypes match closely the simulation results, reaching a FoM of 191dBc/Hz