ECO Flow Integration Based on Mask-configurable Logic and Conformal ECO

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Agenda

- What is an ECO : Why it is mandatory
- Programmable logic : How does it work
- Conformal ECO + Gate-Array Cells: A Perfect Duo
- Examples

ECO

- Engineering Change Order (ECO) is the process of making local changes to the design netlist without re-running the entire synthesis and P&R from scratch.
- ECO Types:
  - Functional ECO
    - Change the functionality of the design
  - Non-functional ECO:
    - Fix timing, cross talk
- Stage:
  - Pre-masks
    - Usage of standard cells to implement the modifications
  - Post-masks
    - Base layer taped-out, metal fix using spare cells

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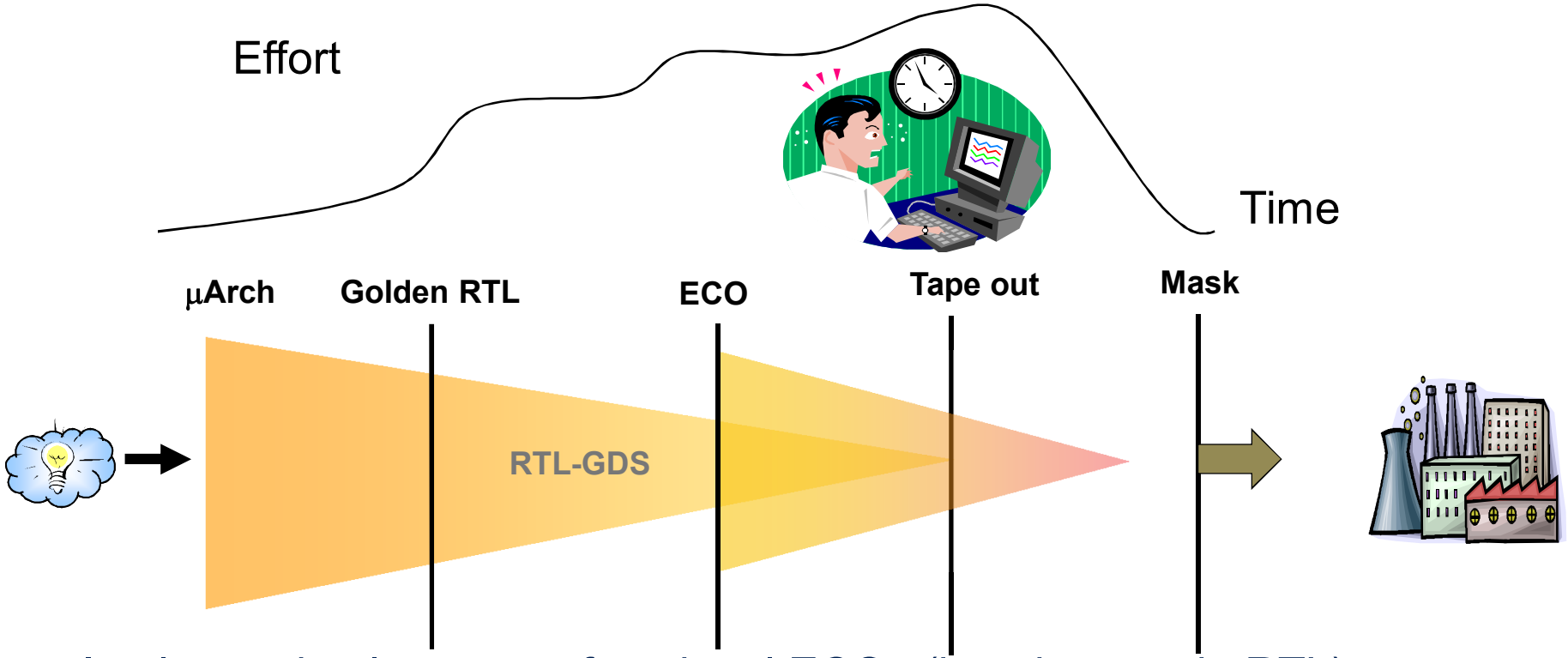
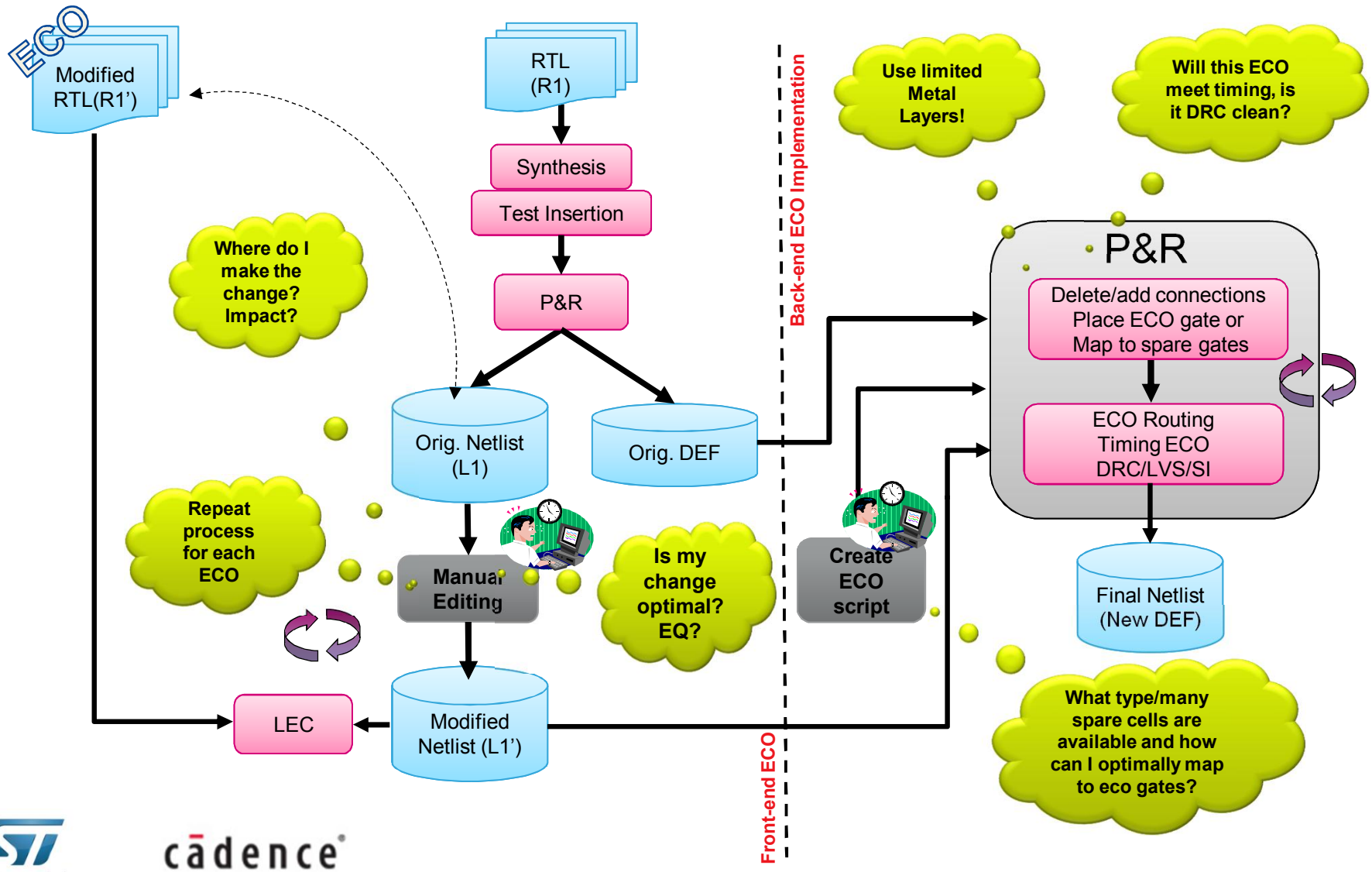
Motivation



- Implementing late stage functional ECOs (i.e. changes in RTL) are often stressful to designers and managers, unpredictable, and can lead to costly project slips

Manual ECO Challenges



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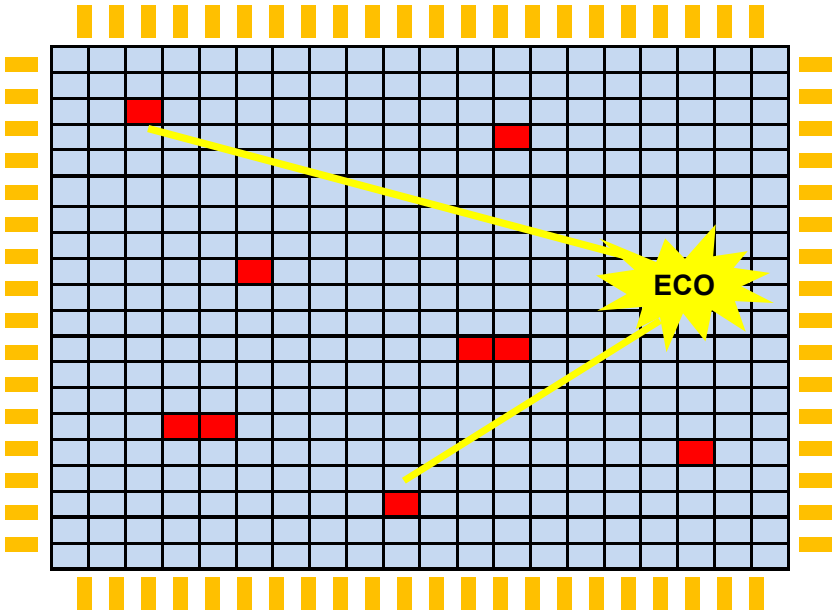
Traditional ECO



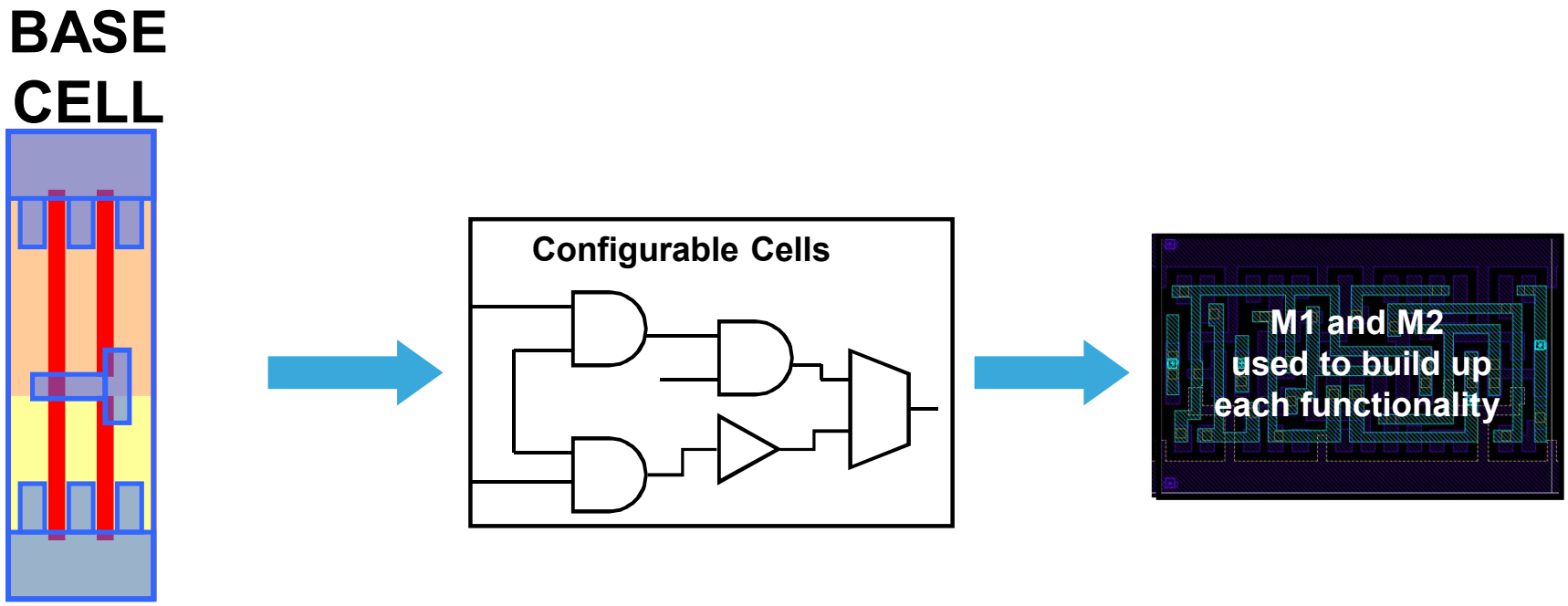
- Traditionally spare cells are inserted early in the P&R flow
- ECO using spare cells is limited by:
  - predefined functions
  - at predefined locations

Need more flexibility

Programmable Logic : How does it work ?

- Mask programmable logic
- Filler cells
- Configurable ECO

Mask Programmable Logic



- ***Base Cell*** defined up to contact layer.
- All functionalities defined using ***higher metal & via layers*** on Base cell.
- Functionalities include ***Combinational*** logic, ***Sequential*** logic.

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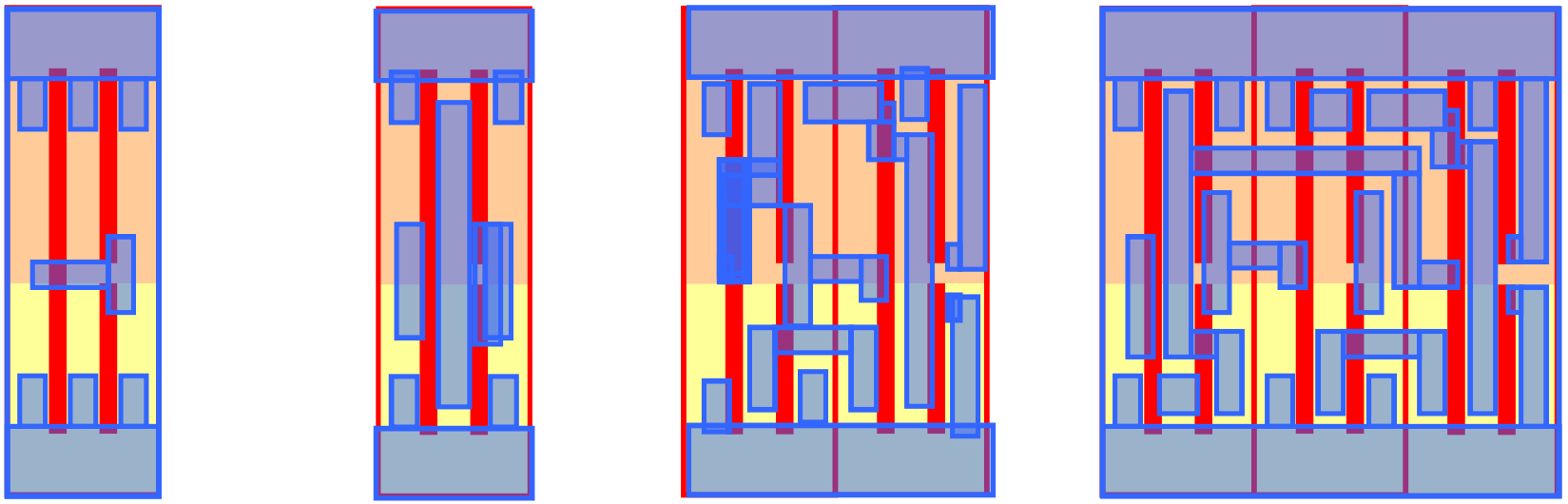
Mask-configurable cells: how it works

Base Cell **Function A** **Function B** **Function C**



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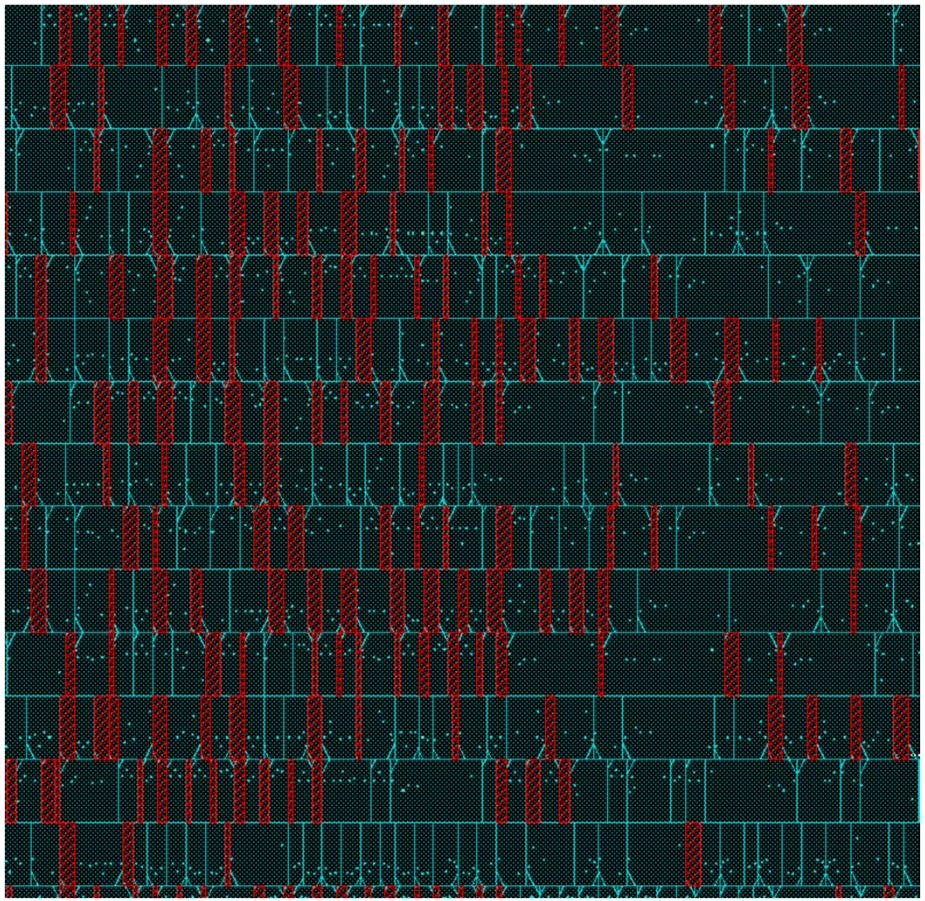
Filler cells



- fill remaining holes in the rows to ensure continuity of:
  - power/ground rails
  - N+/P+ wells in the rows

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Configurable ECO

To **overcome** the traditional ECO limitation of
Predefined function at predefined location
By **providing flexible spare cells** and
using the filler cell area also
for ECO purpose

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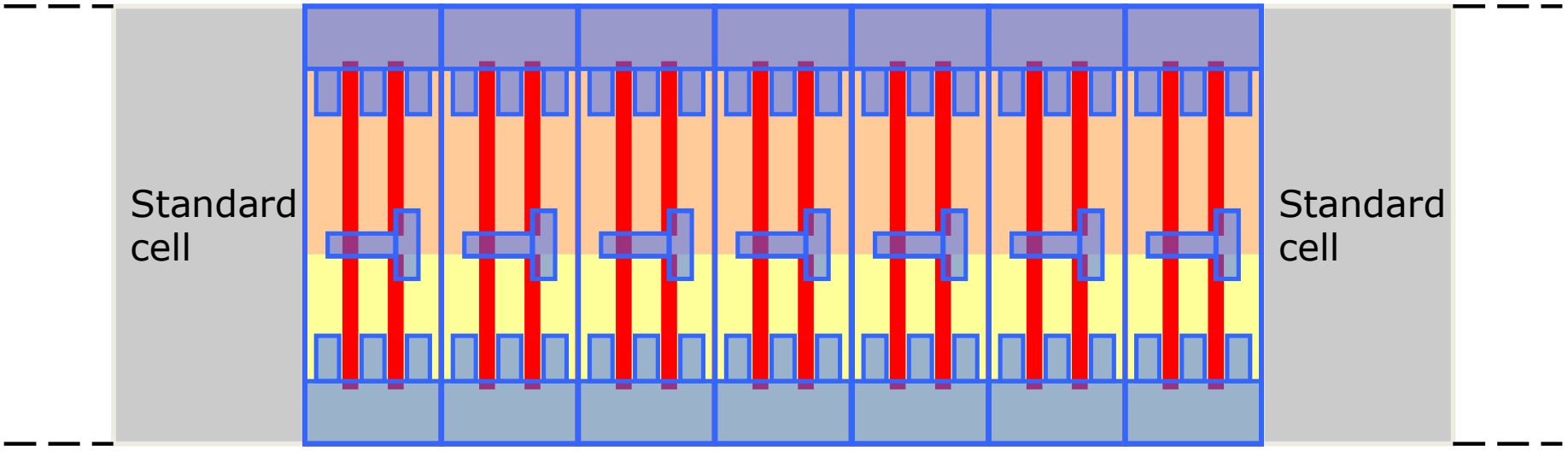
Configurable ECO: base cells insertion

- During P&R
  - Pre-place base cells in order to ensure Configurable ECO implementation capability also in very high dense design
  - Replace standard filler cells with base cells



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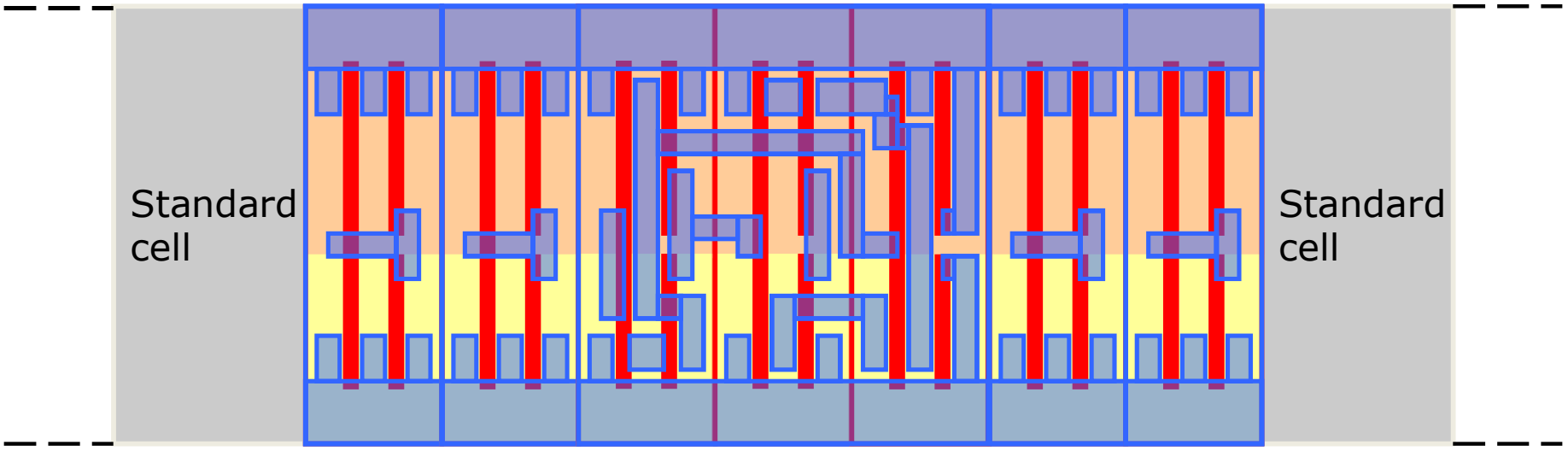
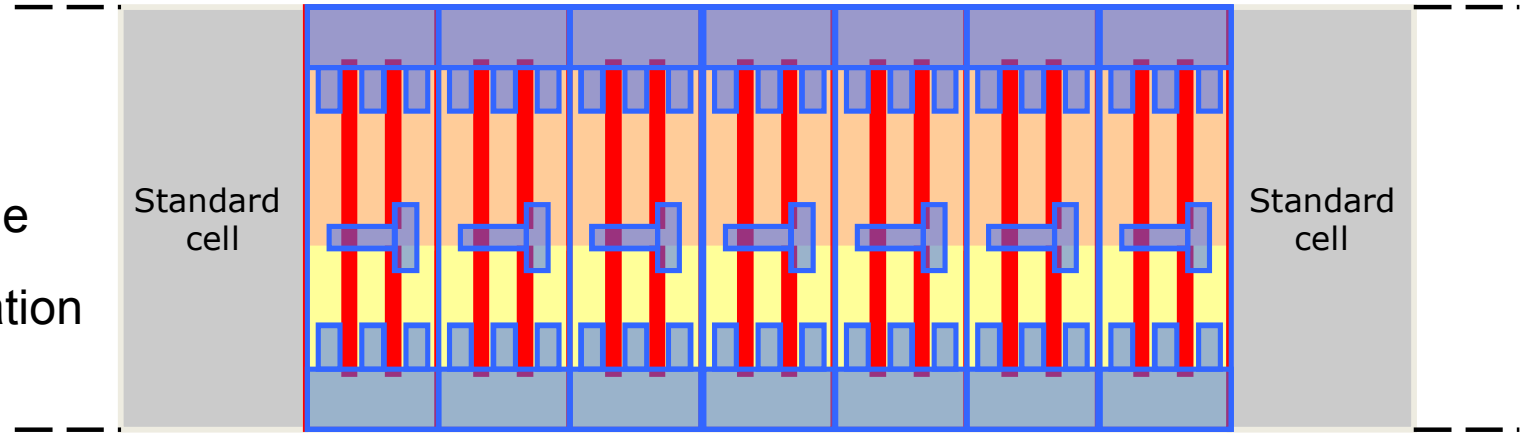
Configurable ECO: cells configuration

- Steps to be followed as part of the current CAD Flow and based on existing functionalities:
  - Remove base cells
  - Place mask-configurable functional cells
  - Fill in empty spaces with base cells

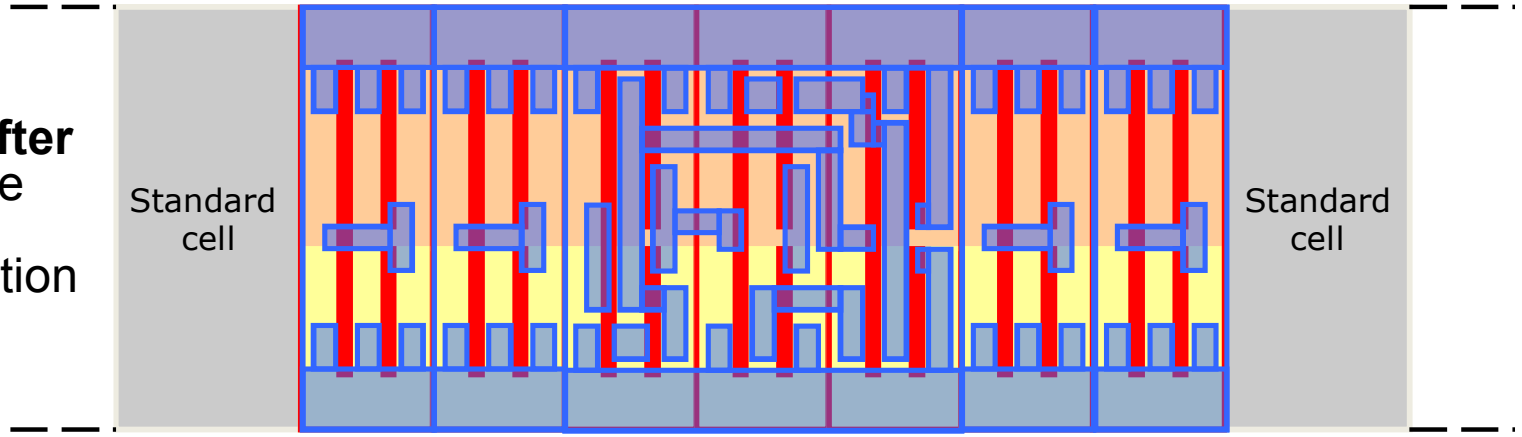


Configurable ECO: Results

- Database **before** Configurable ECO implementation



- Database **after** Configurable ECO implementation



  - Same base layers
  - Different metal layers

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Conformal ECO + Gate-Array Cells , perfect duo

- Conformal-ECO, design change identification
- Automate RTL ECO Implementation

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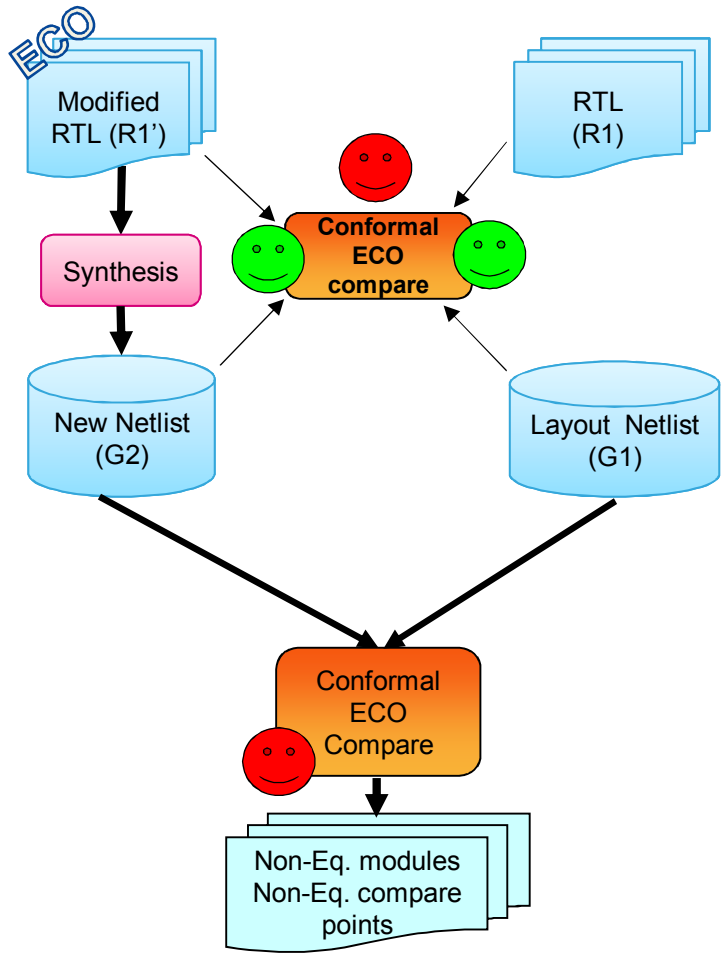
Conformal ECO Flow
Design Change Identification

- Compare R1 vs. modified RTL R1'
  - Identify non-equivalent (ECO) modules and compare points
- Compare R1 to layout netlist G1
  - Make sure it's equivalent (that's your starting point); incremental EC is ok
  - Identify if ECO modules exist in G1
- Synthesize modified RTL R1'
  - Use same synthesis tool and version
  - Provides a structurally similar netlist for Conformal ECO
- Compare R1' to synthesized netlist G2
  - Should be equivalent
- Compare G1 to G2 (hierarchically)
  - Identify non-equivalent ECO modules
  - Identify non-equivalent logic cones
  - Check against R1 vs. R1' results



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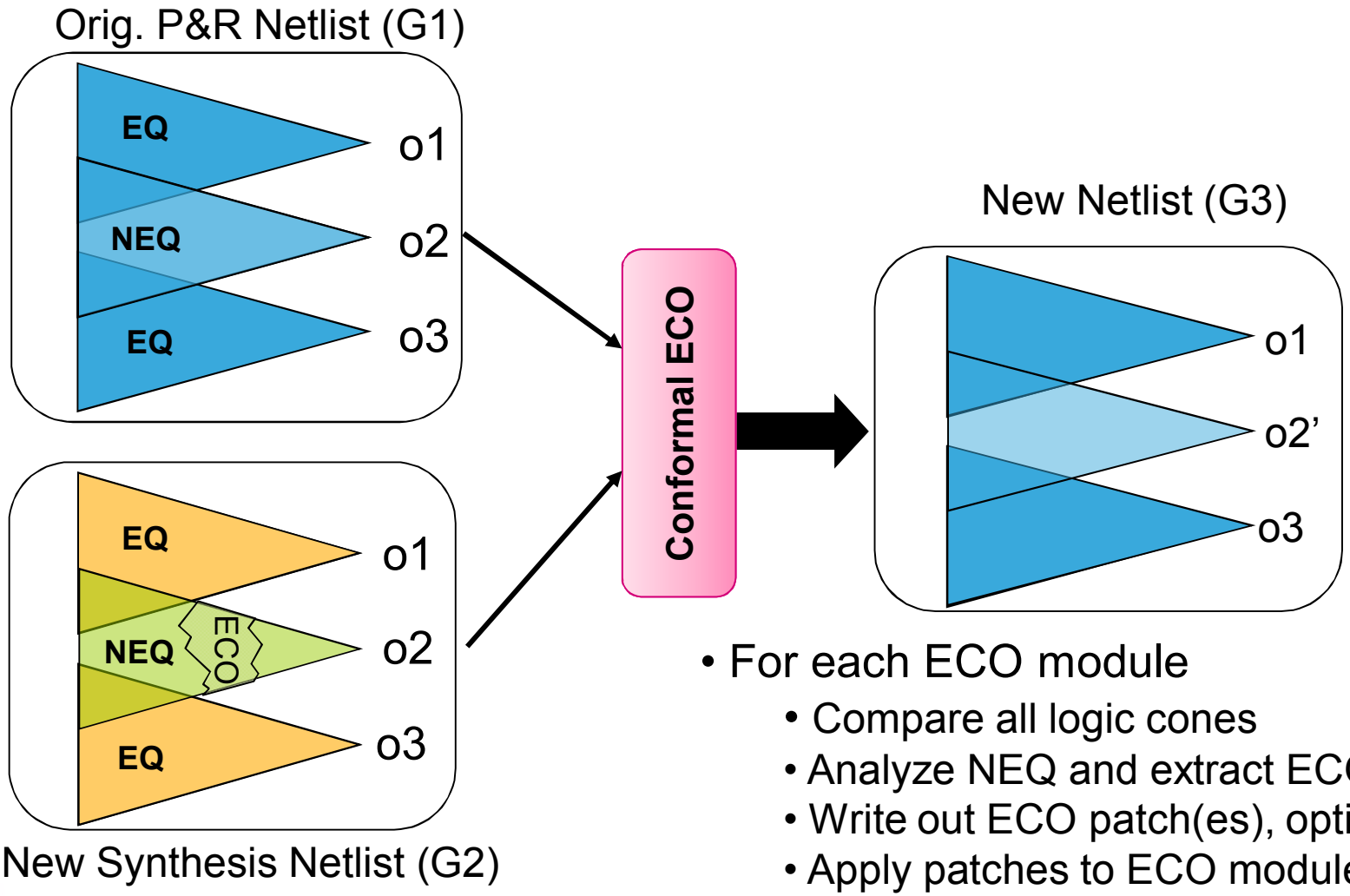
Conformal ECO Flow
ECO Analysis and Patch Generation



- For each ECO module
  - Compare all logic cones
  - Analyze NEQ and extract ECO
  - Write out ECO patch(es), optimize
  - Apply patches to ECO module

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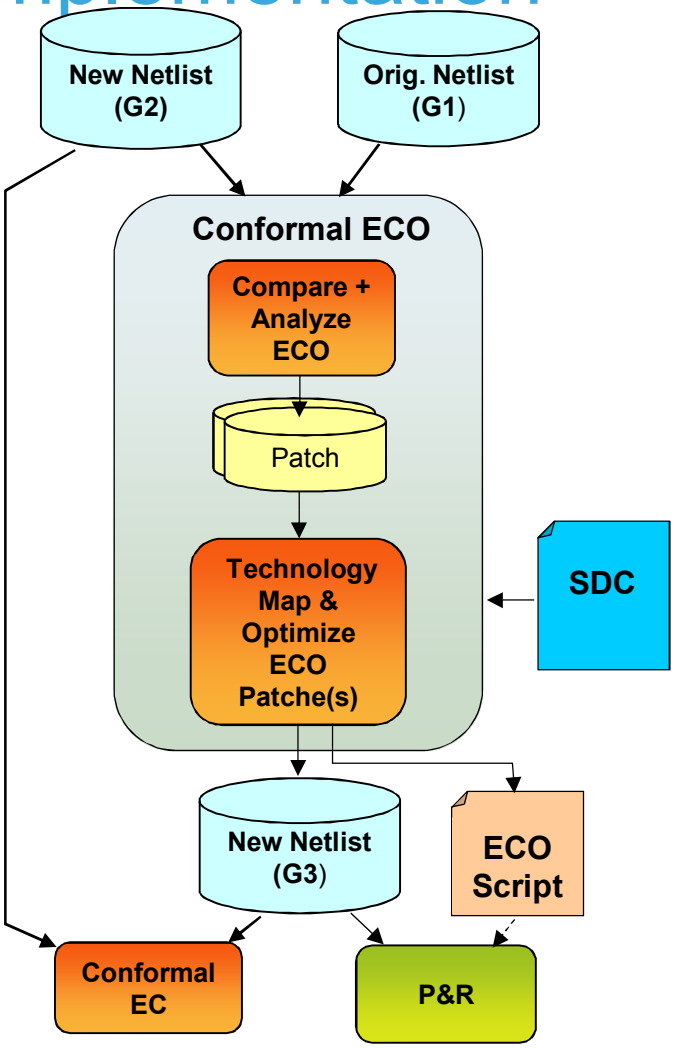
Conformal ECO Designer
Automates RTL ECO Implementation

- Provides automation to implement functional ECOs
  - Uses proven formal engines
- Primarily targets Pre-mask ECOs (does not consider physical information)
- Generates the minimal functional change
  - Preserves the rest (clock trees, scan chains)
- Uses best in class synthesis technology to optimize the ECO logic (RC under the hood)
- Generates a verilog (G3) netlist or an ECO change script for down steam physical implementation tools
- Benefits: Provides faster turnaround time
  - Minimizes manual intervention
  - Provides high value in the design cycle when schedule delays are highly visible
  - Reduces costs in resources



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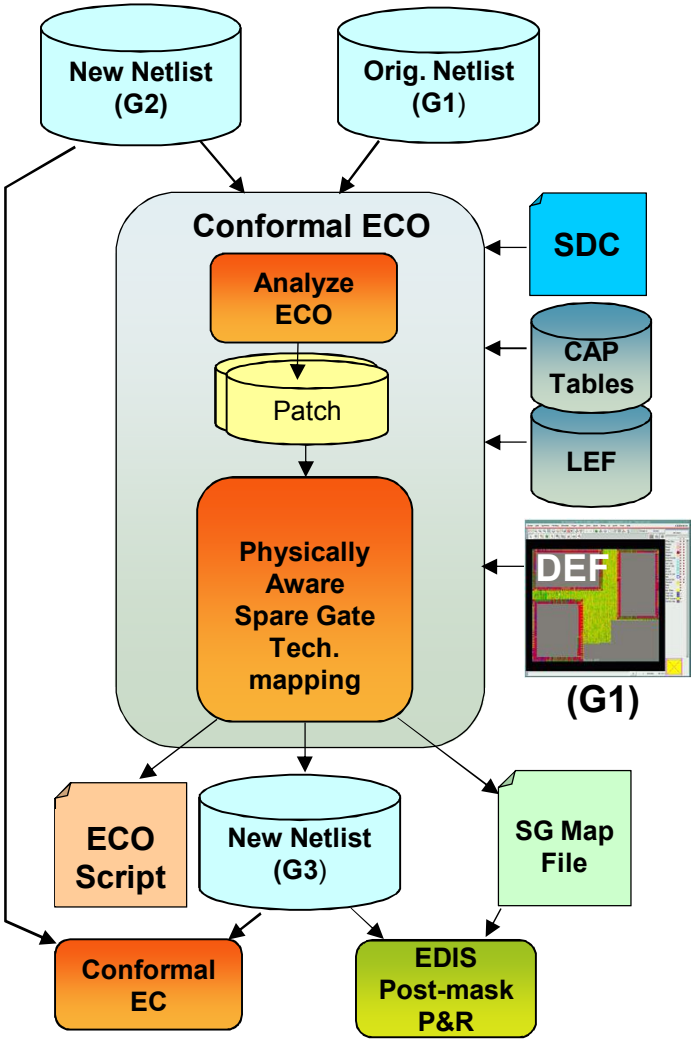
Conformal ECO Designer
Post-mask ECO

- Builds upon Conformal ECO XL capabilities
  - Performs ECO analysis and implementation (Is timing and physically aware)
- Uses best in class physical synthesis technology (RCP) to map one or more ECO into available standard cell and GA spare gates
- Generates a spare gate mapping guidance file for EDIS and PnR tools
- Key Benefits: Reduces mask costs and improves designer productivity
  - Provides early estimate of ECO feasibility based on spare gate resource availability
  - Re-uses freed-up cell along with spare gates
  - Can handle sequential and combinational ECOs



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Several Example

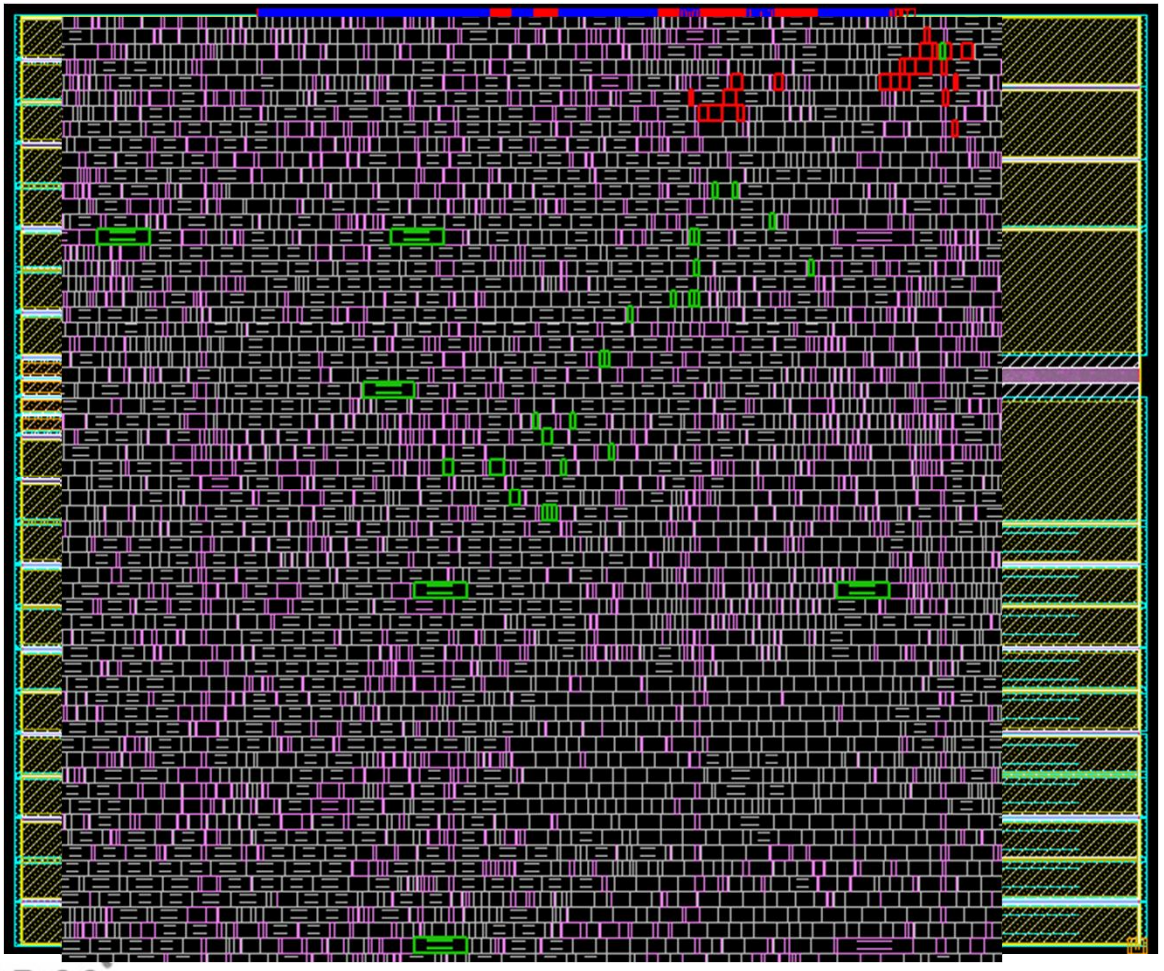
- Automotive 65LP Project
- 40LP Sub System
- Other Applications…
- Important ECO Changes Can Happen?

Automotive 65LP Project: ECO modifications

- Post Mask netlist modification
- ECO Detail:
  - Sub-module replacement
  - New sub-module implemented using only mask-configurable cells
    - composed by **25 combinational cells**
  - FF added to each input signal of the new module
    - **Total number of added flip flops: 6**

Automotive 65LP Project: ECO Place

- Mask-configurable cells (green) placed closed as much as possible to the original standard cells (red) location



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Automotive project: ECO CTS

- Mask-configurable flops added on **mclk** clock
  - **Skew and latency under control**

Before ECO flow

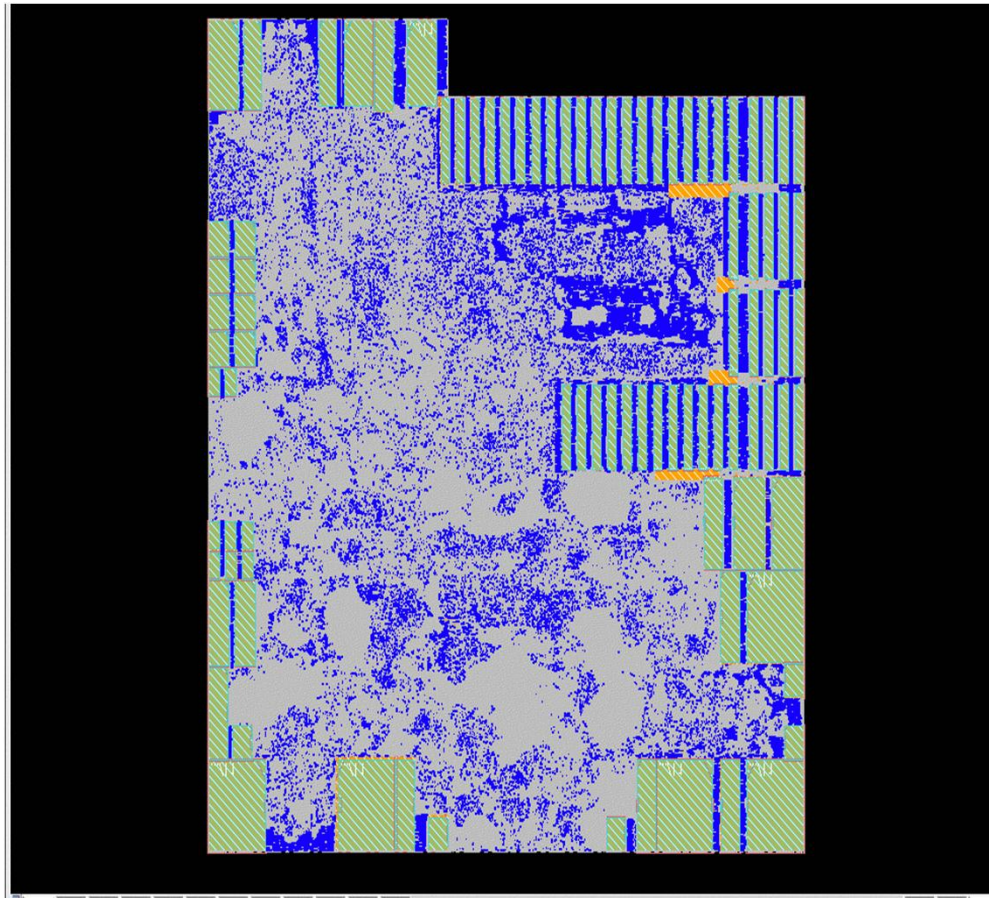
Clock	Skew	Longest Path
mclk	0.332	2.179
galgps_rfclk	0.215	1.956
clk_bmp	0.014	1.024
pipe_clk	0.013	0.743
tst_clk0	0	0
tst_clk1	0	0
PERIPH_BB_CLK	0.333	1.307
clk16f_bb	0.082	0.790

After ECO flow

Clock	Skew	Longest Path
mclk	0.328	2.11
galgps_rfclk	0.227	1.91
clk_bmp	0.017	0.964
pipe_clk	0.015	0.721
tst_clk0	0	0
tst_clk1	0	0
PERIPH_BB_CLK	0.302	1.268
clk16f_bb	0.048	0.772

40LP Sub System1/2

- Technology node **40nm**
- Filler insertion strategy adopted
  - only mask-configurable base cells
  - 50% of available free space



Mask-configurable base cells are in blue color

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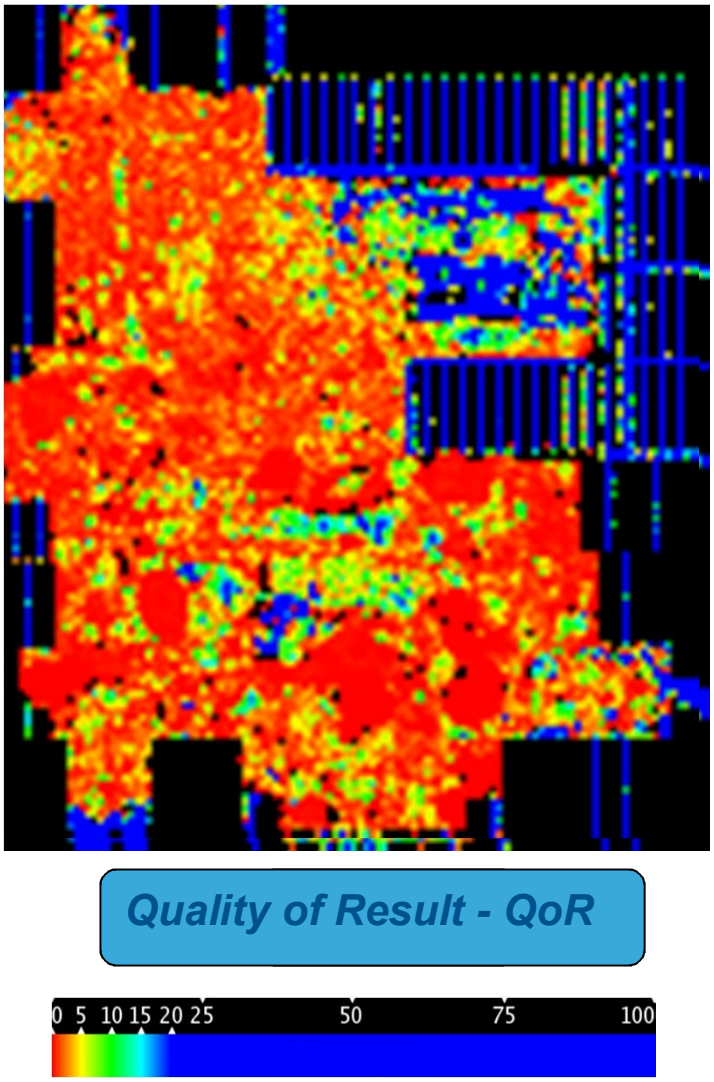
40LP Sub System 2/2

- Cells Insertion analysis
  - **Coverage 11,6%**
  - **Quality of Result – QoR 6,87%**
    - quality of base cell sites distribution
    - QoR increase if the number of clusters composed by at least 32 sites increase
      - with 32 sites is possible to implement any functional cell
    - Ideally 6,87% of core area can be modified by mask-configurable ECO



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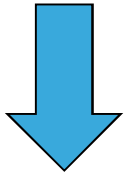
Other Applications…

- Mask-configurable ECO can also be used for design timing closure
  - Computer & Comm. Infrastructure project – 65nm techno
    - After base layers tape-out
      - Timing closure
      - Functional fixes
  - Automotive project – 65nm techno
    - After base layers tape-out hold violation has been discovered and fixed thanks to mask-configurable cells

Important ECO Changes Can Happen?

When digital IPs are not 100% finalized (still under development)…

When specifications are supposed to be changed during the product life cycle…



… we may need to perform more important ECOs

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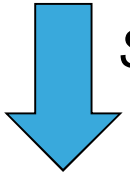
How to Address Important ECOs?

- Standard flow address only few % changes
- Metal-programmable solutions (e.g. Gate Array) are more flexible than required → not-so-justified overheads
- Manual ECO not applicable at all!



Something new is needed!

- Basic Idea:
  - Use a mix of standard cells and configurable GA cells to map the first revision of the design

    e.g. 70% std.cell + 30% GA to smooth overheads
  - Use Conformal ECO GXL to map the revised versions using both GA cells and freed standard cells.

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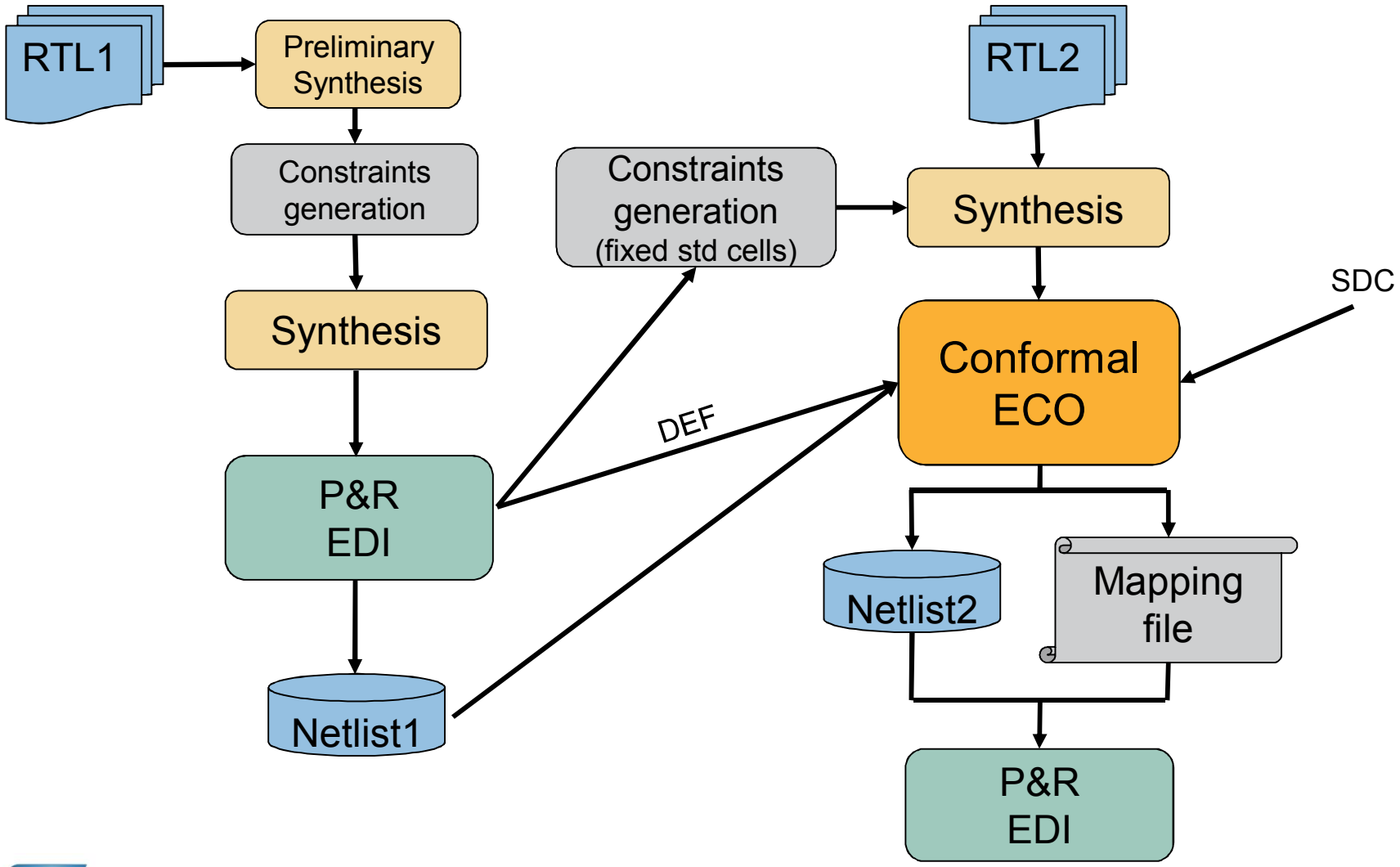
Remap Flow Overview



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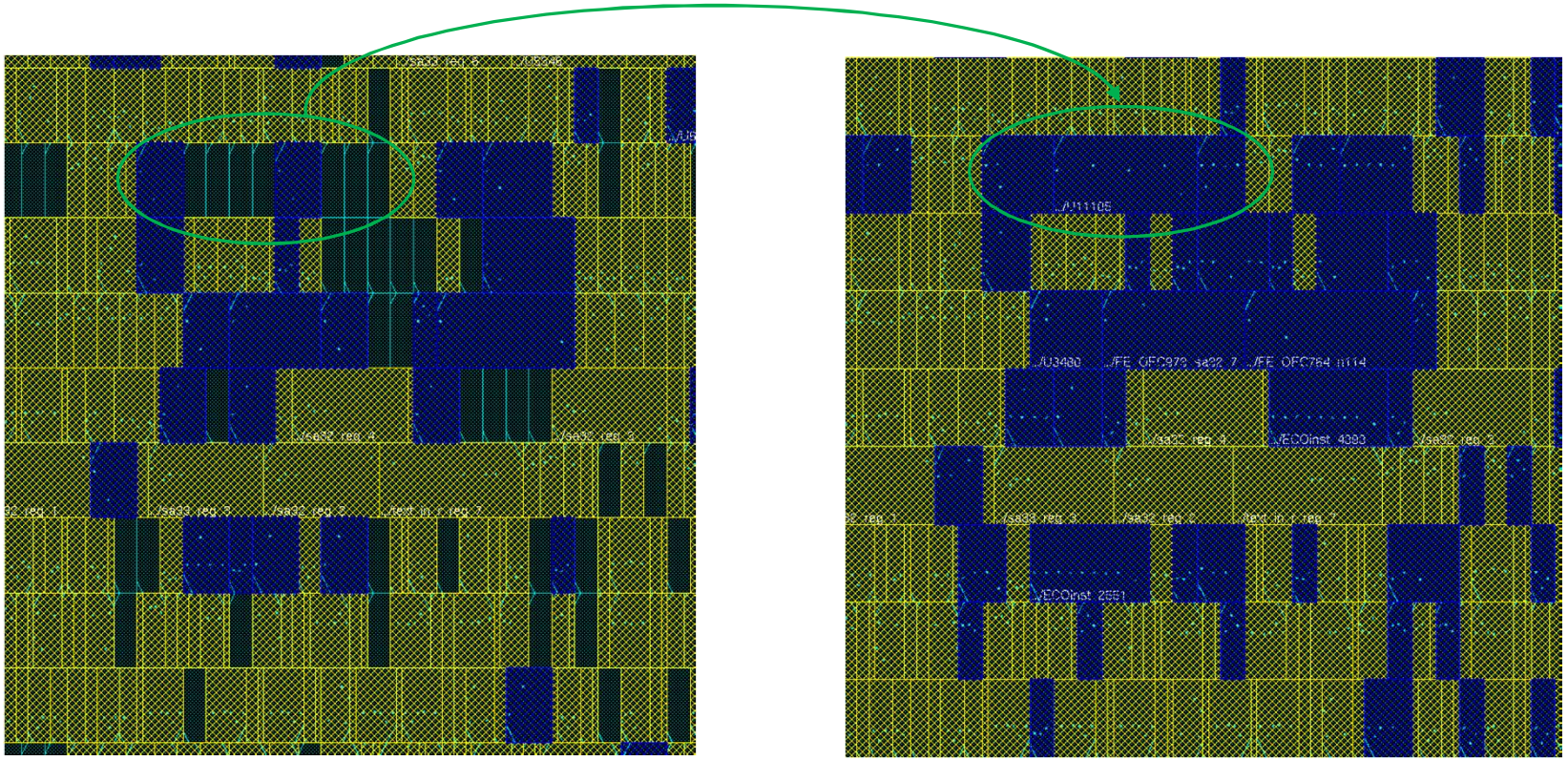
AES Test Case

- 128-bit AES encryption/decryption (source opencores.org)

- First revision:
  - 50K gates
  - Target frequency 200MHz
  - Technology: CMOS 65nm
  - Target core utilization: 70%
  - 80% std.cell + 20% GA

ECO Remap



First implementation

Mapped ECO

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AES Test Case

- RTL Modifications:
  - MixColumn polynomials
- Results:
  - Design Functionality changes: 10%
  - Std cells reuse: 1.5% (15% of the patch)
  - Remapped netlist placed and routed

Conclusion

- Methodology acceptable for important ECOs up to few tens percent.
  - Traditional ECOs are 3-4%
  - Conformal ECO well integrated in the flow

- Requirement for bigger modifications:
  - Use more Gate-Array cells for first implementation
  - Consider other solutions like Configurable Array using only GA cells.
  - Cannot be considered as ECO anymore

Acknowledgements

- Thanks for the Lund University to have selected and invited us
- Thanks for the Cadence Marketing team for his help on reviewing this presentation
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Thanks, Tak, Grazie, Merci

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