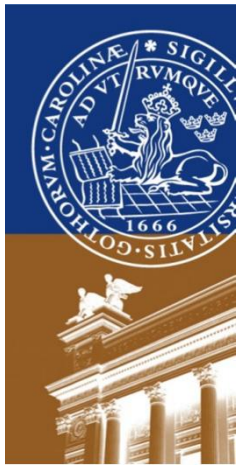
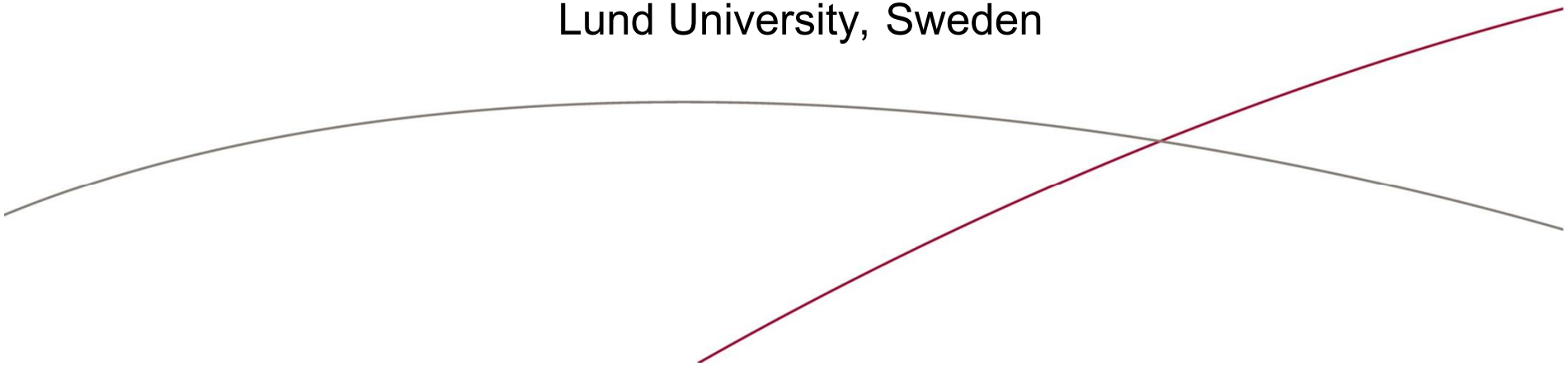


Ultra Low Power Circuit and System Design

Henrik Sjöland
Department of Electrical and Information Technology
Lund University, Sweden



People Involved in Ultra Low Power

Henrik Sjöland
John B Andersson
Oskar Andersson
Pietro Andreani
Carl Bryant
Rohit Chandra
Ove Edfors
Anders J Johansson
Nafiseh Seyed Mazloum
Reza Meraji
Babak Mohammadi
Peter Nilsson
Dejan Radjen
Joachim Rodrigues
Yasser Sherazi
Viktor Öwall

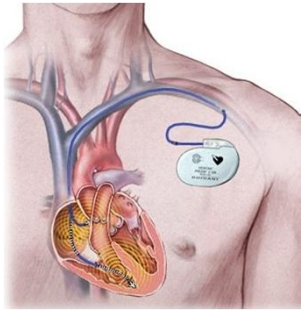
Outline

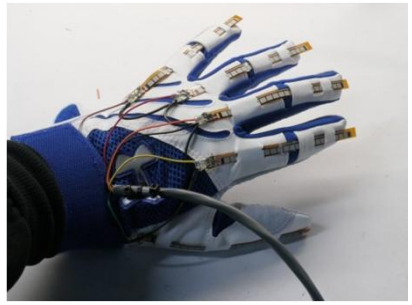
- System Design
  + SSF UPD project overview
  + Transceiver
- Circuit Design
  + Receiver front-end
  + Dual threshold gates
  + Sub-V_T memories
- Questions

Project Overview: Wireless Communication for Ultra Portable Devices

Applications

- Medical implants
- Hearing aids
- Pacemakers
- Watches
- Video game controls
- Active RFID tags
- Remote controls
- Keys
- Body area networks
- Sensor networks
- etc.





In some applications the battery must last the equipment lifetime!

State-of-the-art

Press Release March 2012:
“Leading hearing solutions company – GN ReSound – is using the Nordic nRF24L01+ in its award-winning ReSound Alera hearing aid to stream audio direct from TVs and other consumer devices such as computers and home cinema systems”

www.nordicsemi.no :
nRF24L01+, Single-chip 2.4GHz transceiver
-94dBm @ 250kb/s, 12.6mA from 1.9V = 24mW

Targets

- 1mW in active mode
- 1uW in standby
- 1mm^2 chip area in 65nm CMOS
- 250 kbit/s

- Receiver chain from antenna to decoder
- Medium Access Control (MAC)
- Propagation in bio-applications

- Final goal: Demonstration of antenna + chip in medical implant mock-up

System Parameters

Frequency band: 2.4GHz ISM
+ Wide band, many channels
- Lot of disturbances

Modulation: Wideband FSK
+ Efficient transmitter
+ Low spurious emissions
+ Fits homodyne receiver

Transmit power: -10dBm

Sensitivity: -97dBm (125kbit/s mode)

Can handle up to 87dB path loss
+ Required for body area network
+ 80dB worst case loss ear2ear @ 2.4GHz

Sjöland, et. al, ”A Receiver Architecture for Devices in Wireless Body Area Networks”, IEEE JETCAS, 2012

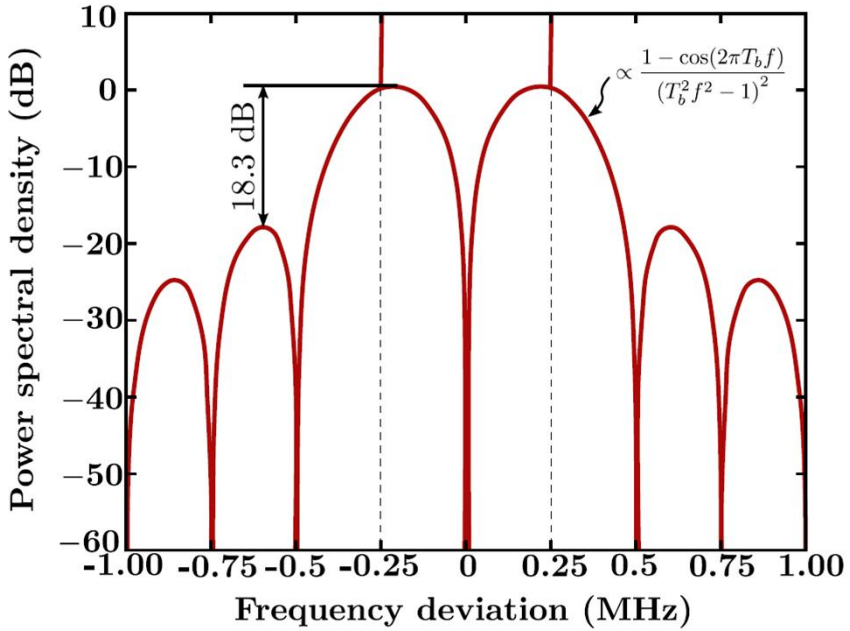
Modulation

Wideband FSK

+ Efficient transmitter
+ Low spurious emissions

Parameters

* 250kb/s
* Δf = +/- 250kHz

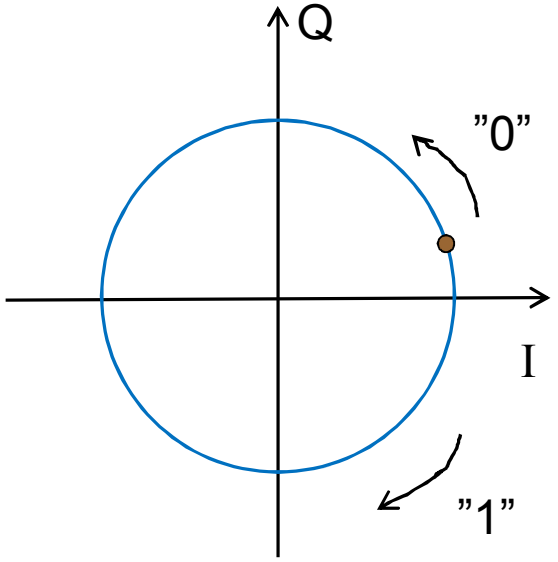


Spectrum of modulated signal (unfiltered)
PLL loop filter further suppresses sidebands

Observe mid band null => Fits homodyne receiver

Modulation, in IQ-baseband

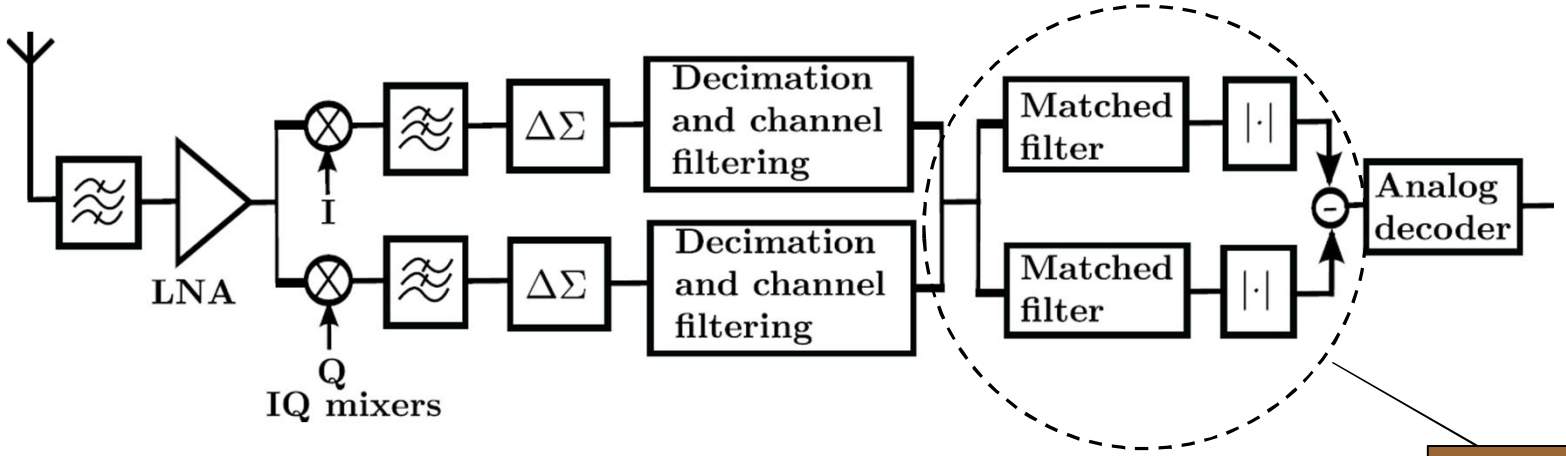
Wideband FSK
* 250kb/s
* Δf = +/- 250kHz



One full turn per symbol
Direction depends on databit

How to demodulate?

Receiver



Demodulation Structure

4 samples/bit used => matched filter for ”0” = 1, -j, -1, j
”1” = 1, j, -1, -j

Easily implemented

Magnitude comparison of matched filter outputs => decision
+ No AGC or information about absolute phase needed

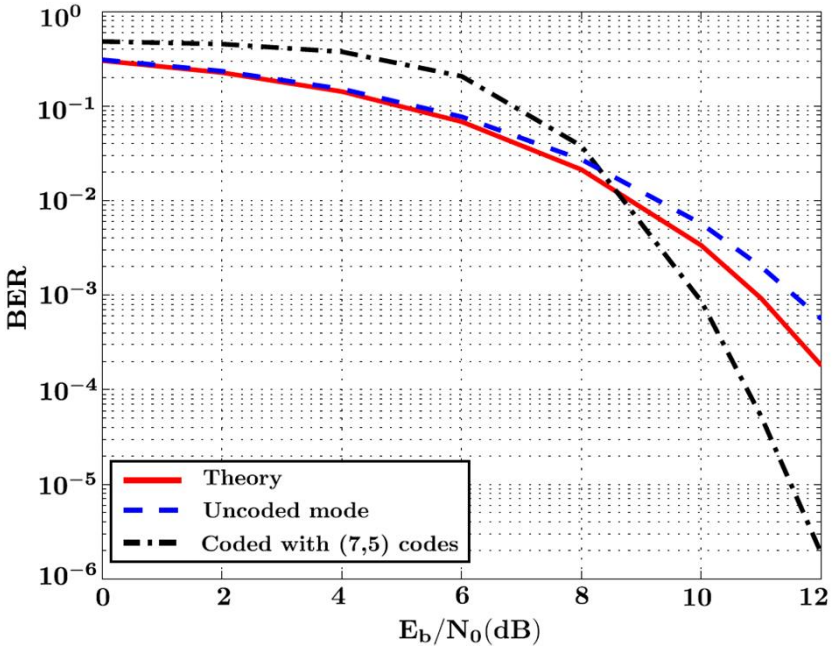
Soft information for analog decoder: magnitude difference

Tap sum = 0 =>
Zero DC gain

Sensitivity

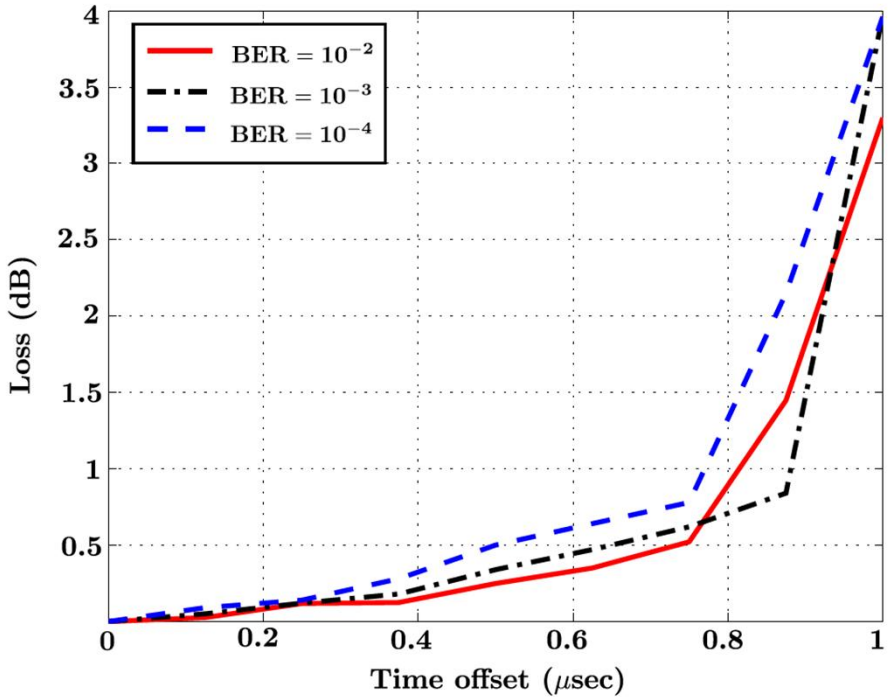
Decoder on:
Thermal noise: -174dBm/Hz
Noise Figure: 13dB
Eb/No: 10dB
Datarate: 125kbit/s
SAW filter loss: 3dB
Sensitivity=-174+13+10+dB10(125k)+3=
-97dBm

Decoder off:
Thermal noise: -174dBm/Hz
Noise figure: 13dB
Eb/No: 12dB
Datarate: 250kbit/s
SAW filter loss: 3dB
Sensitivity=-174+13+12+dB10(250k)+3=
-92dBm



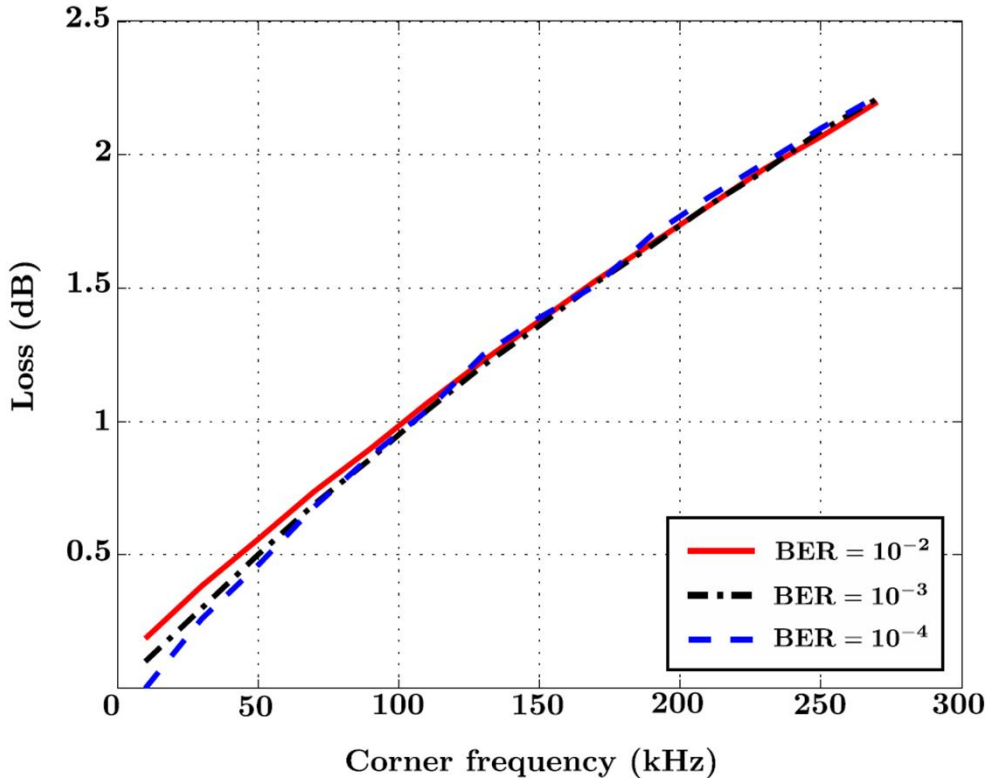
BER in thermal noise

Impact of Imperfections – Time offset



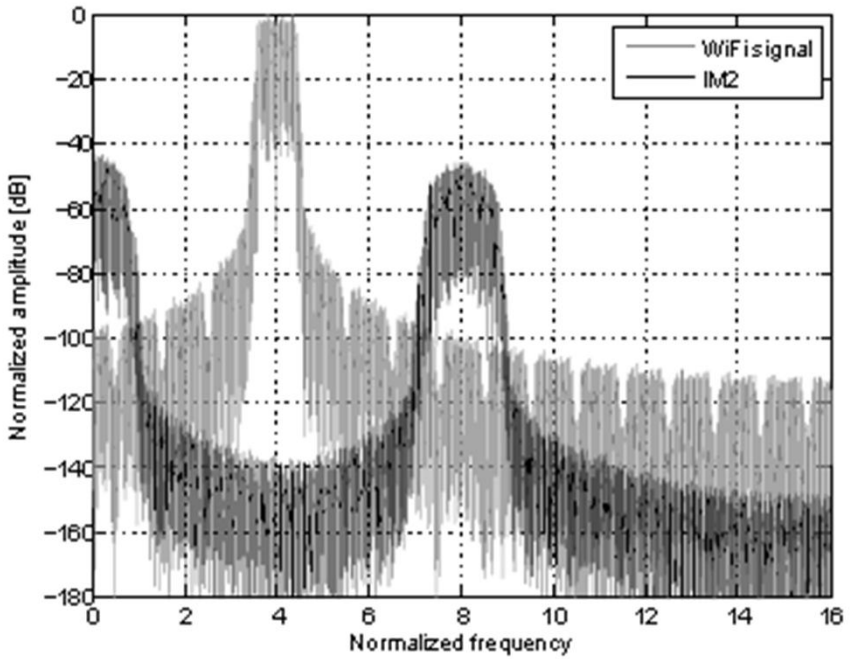
4 samples/bit = 1MS/s = 1us resolution
Max error = 0.5us
Maximum loss = 0.3dB @ BER .001
Bit synch: Selection between 4 time delays sufficient

Impact of Imperfections – 1/f noise



50kHz 1/f noise corner => 0.5dB degradation

Impact of Imperfections – IM2



Spectrum of interfering WiFi signal and the 2nd order intermodulation

With IIP2 = 0dBm, a -37.5dBm WiFi interferer will desensitize by 3dB

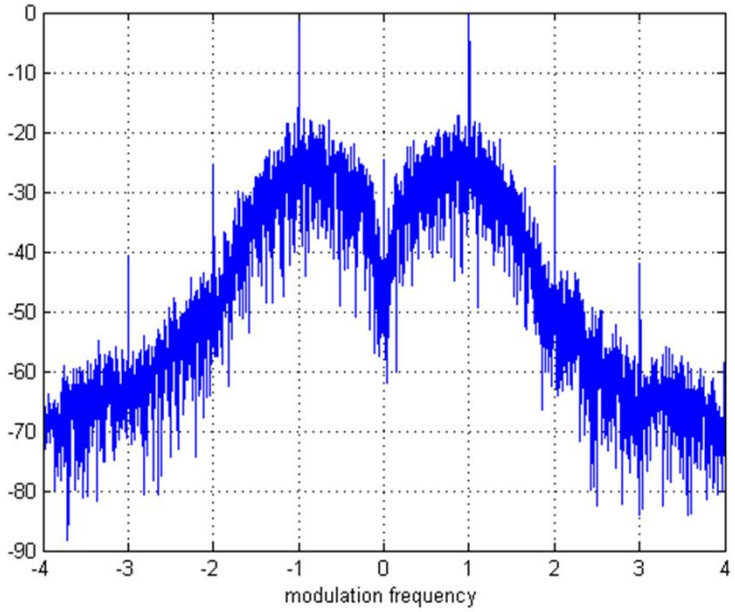
More System Aspects

Can be found in the journal paper:

H. Sjöland, J. B. Anderson, C. Bryant, R. Chandra,
O. Edfors, A. Johansson, N. Seyed Mazloum, R. Meraji,
P. Nilsson, D. Radjen, J. Rodrigues, Y. Sherazi, V. Öwall,
"A receiver architecture for devices in wireless body area networks",
IEEE Journal on Emerging and Selected Topics in Circuits and Systems, JETCAS, 2012

Transmitter

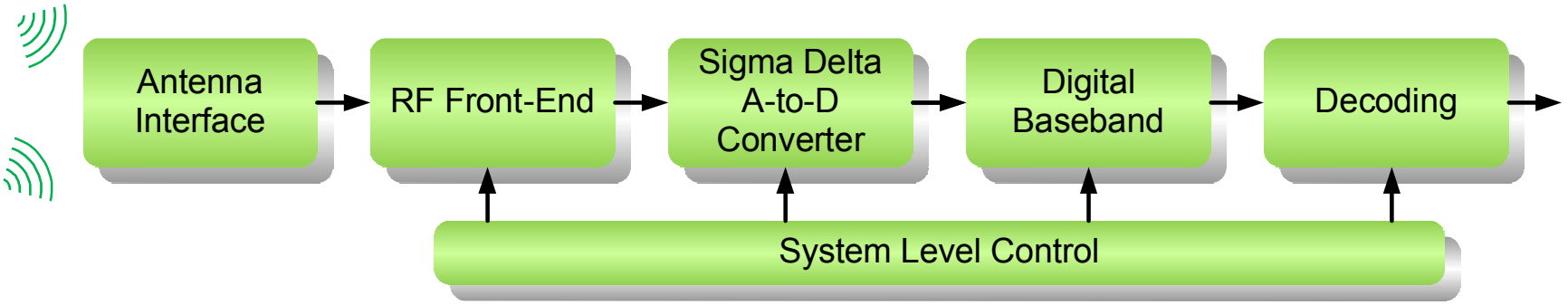
- Project course for PhD students
- PLL based
- FSK modulation
- Full integration
- Fast settling
- Low power
- Taped out in June => Circuits back soon



System simulation of transmitter output

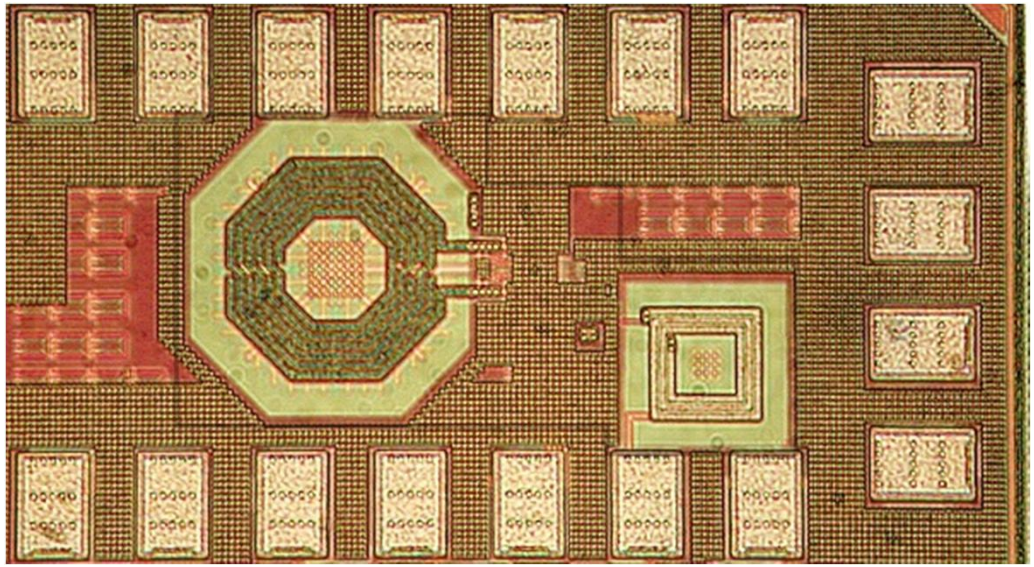
Poster session tomorrow

Poster on progress in each sub-project



Carl Bryant

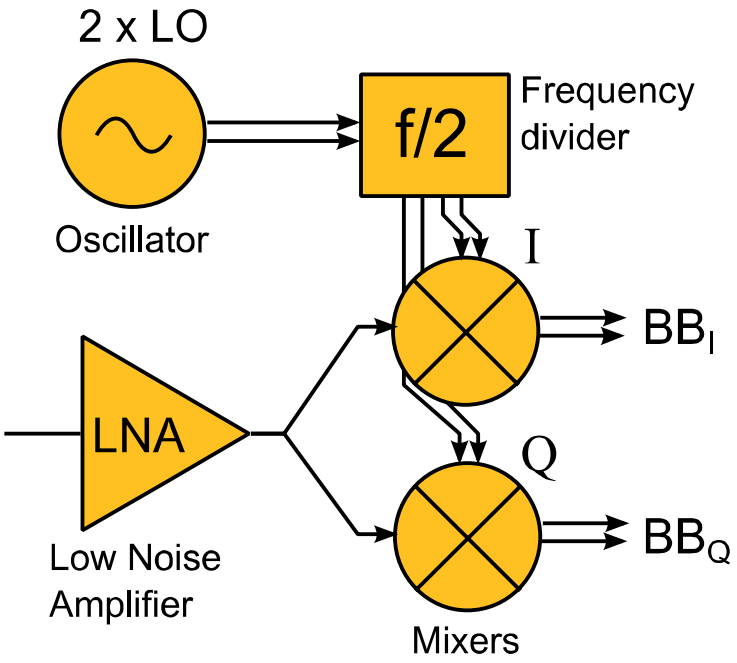
A 2.45GHz Ultra-Low Power Quadrature Front-End in 65nm CMOS



0.61x0.39mm

IEEE RFIC 2012 Montréal, Canada June 17-19

Block schematic



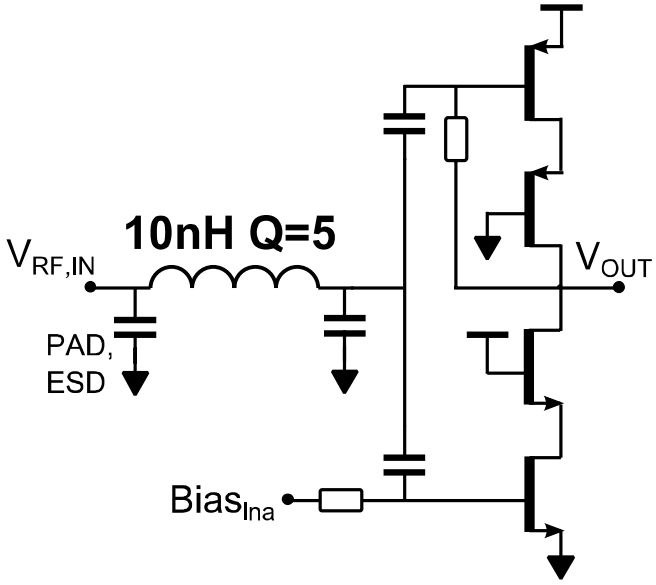
- Single VCO at 2x frequency = compact
- Passive mixers, zero IF

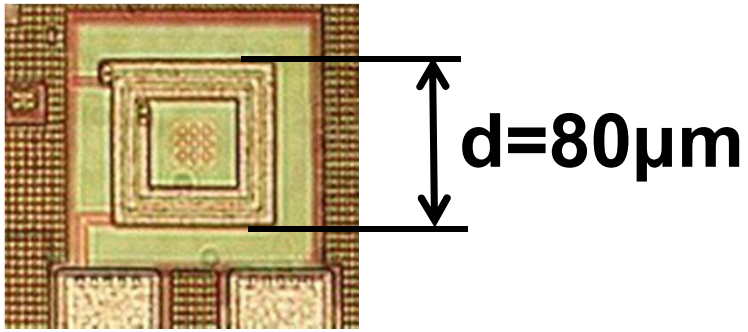
Circuit Design - LNA

- 50Ω input impedance
- Low Q inductor
  - Match to parasitic R
  - Provides voltage gain
  - Compact 4 layer design

    10 turns

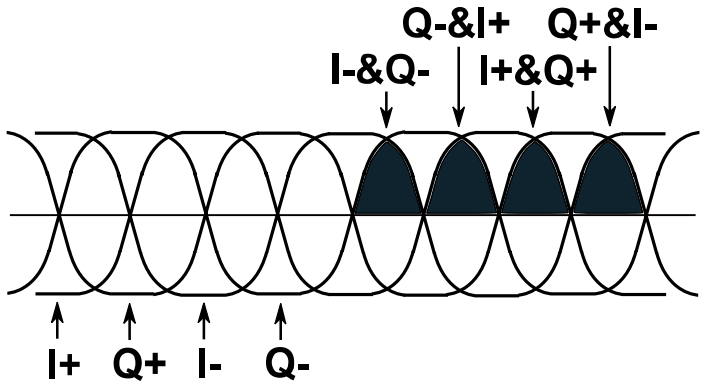
    d = 80µm

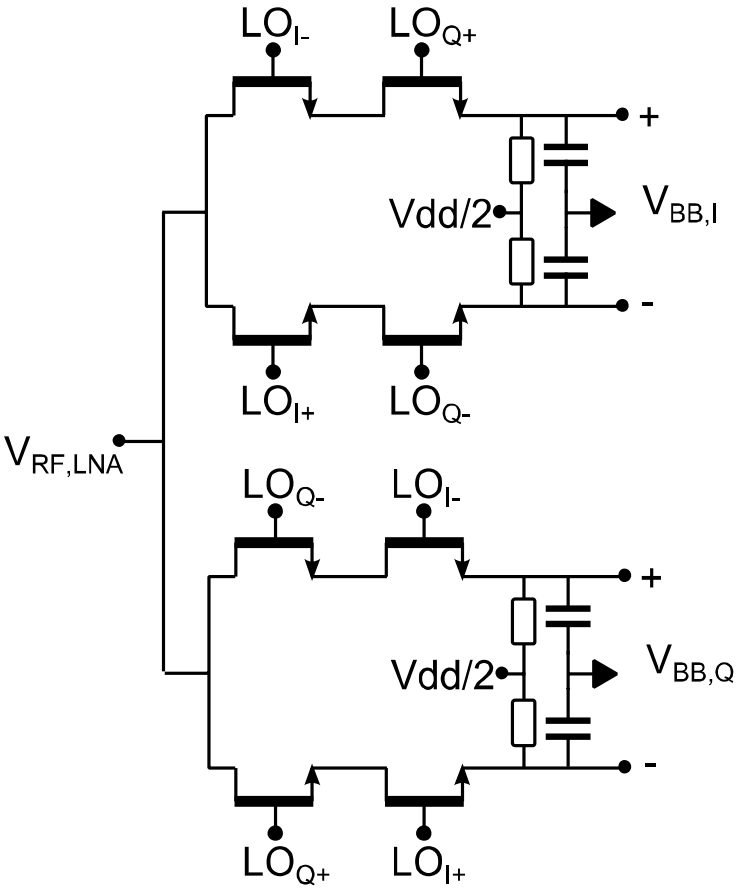




Circuit Design - Mixers

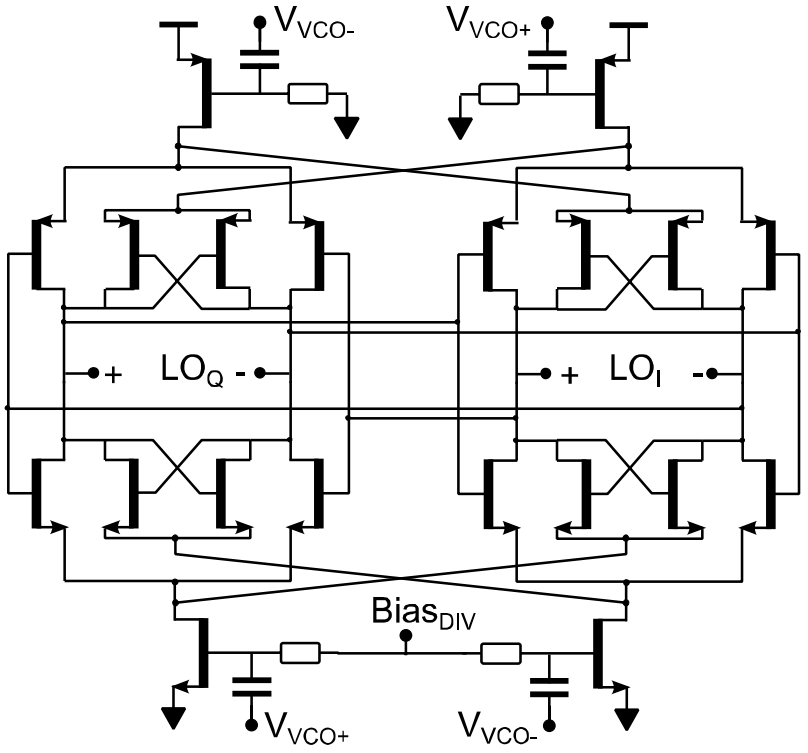
- Passive mixers provide RF filtering
- Avoid conduction overlap
- AND-function
- 25% effective duty cycle





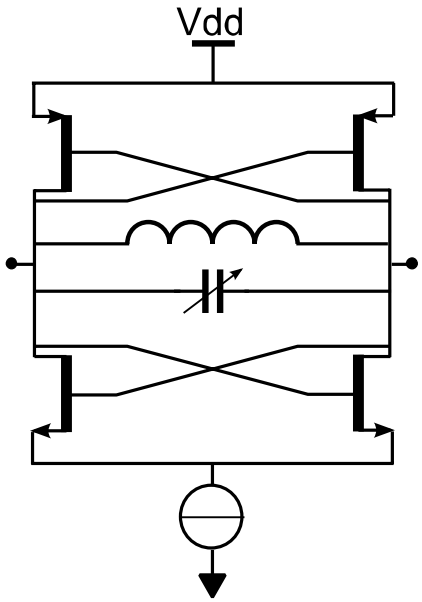
Circuit Design - Divider

- Similar to standard CML divider
- Fully complementary
- No constant bias current
- Each part driven by both VCO outputs
- Reduced sensitivity to VCO imbalance

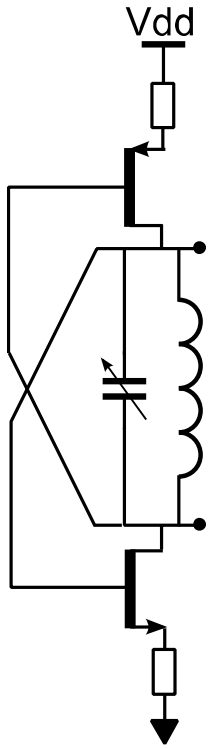


Circuit Design - VCO

- Operating from single 0.8V supply
- Current reuse techniques:



Complementary push-pull

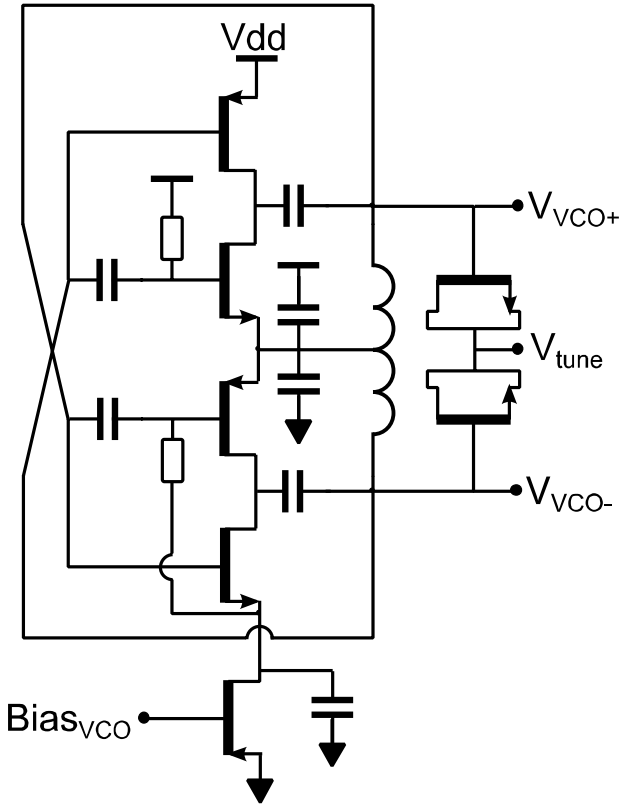


Current reuse by stacking

Circuit Design - VCO

Combine both techniques:

- Efficient current use
- Low loss in tail source
- Better balanced than single stacking



Results

- Manufactured in 65nm CMOS
- Bonded to PCB
- External amplifiers at output (to 50Ω)
- Measured 3 samples

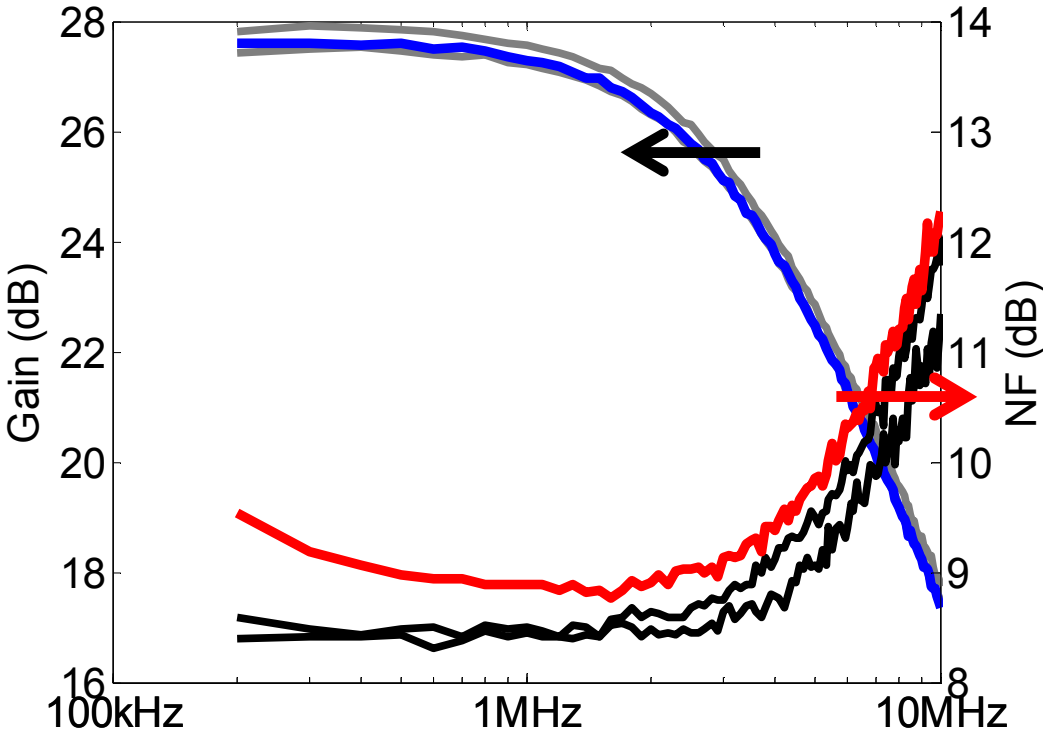
Power consumption:

LNA	VCO	Divider	**Total**
100µW	65µW	230µW	**395µW**

Results

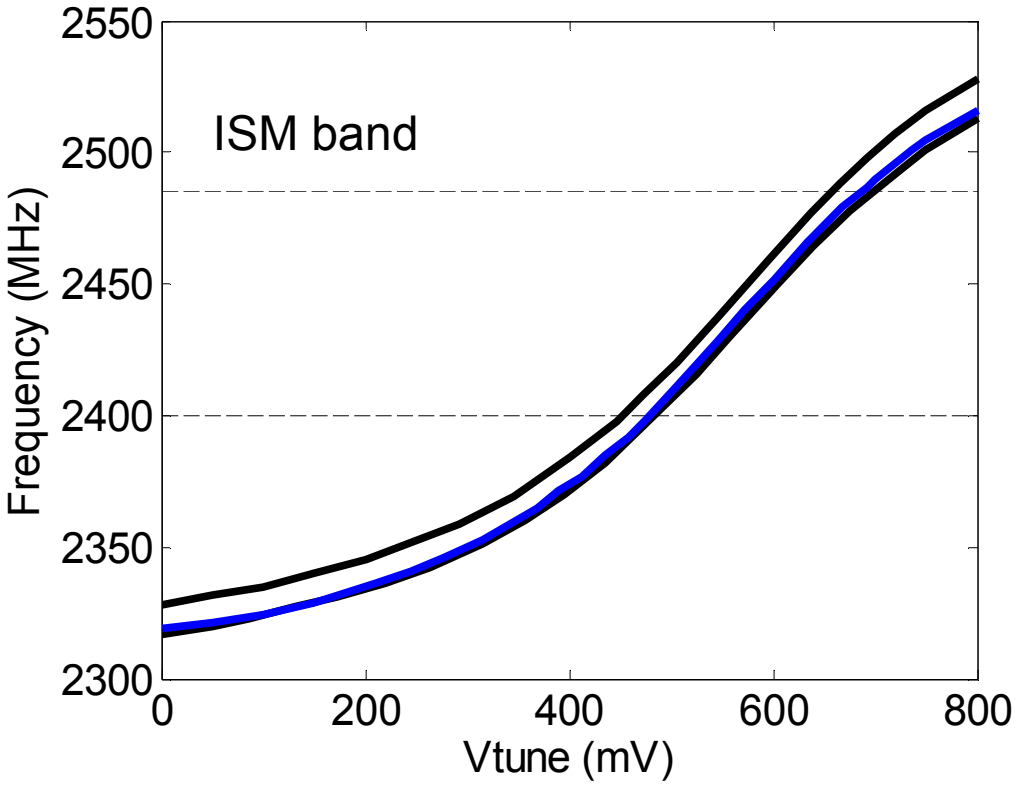
Gain = 27.5 dB

NF = 9dB

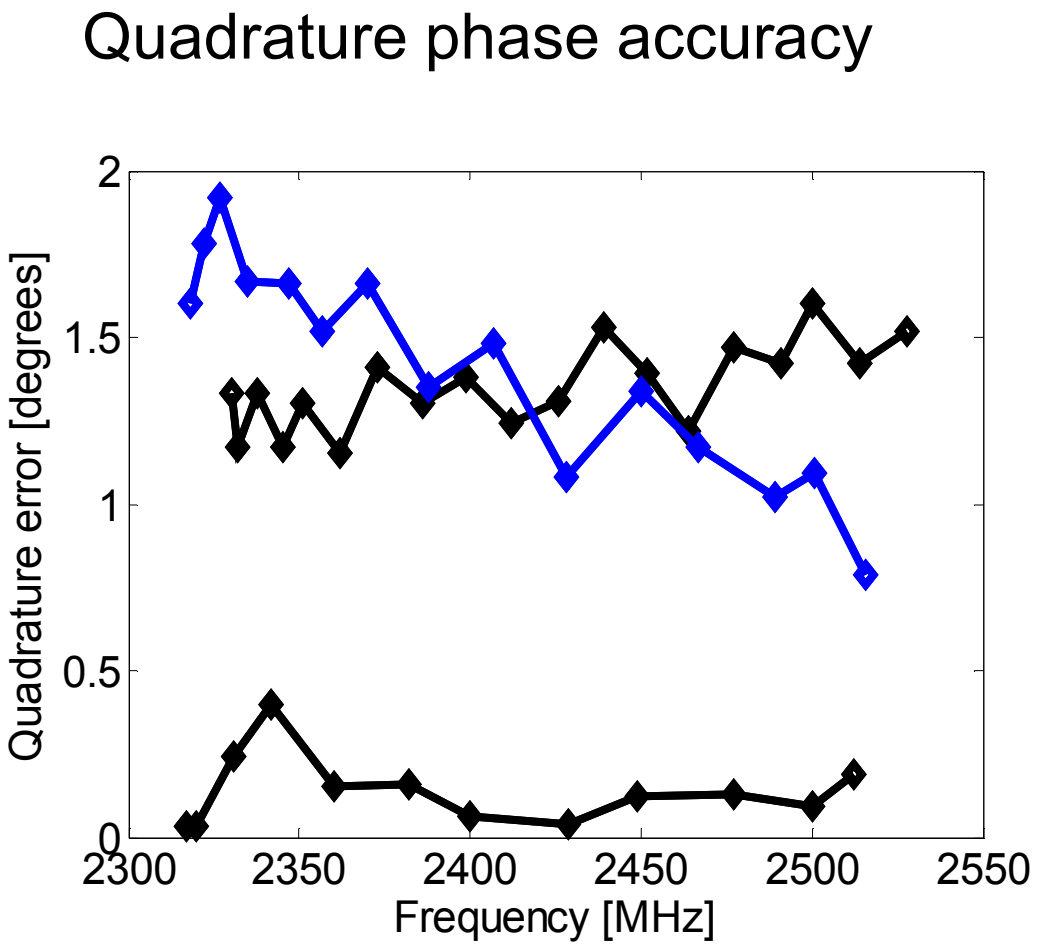


Results

8% Tuning range



Results


Quadrature phase accuracy
Quadrature error [degrees]
2
1.5
1
0.5
0
2300
2350
2400
2450
2500
2550
Frequency [MHz]

Results

	This work	[5] JSSC 11	[6] AICSP 11	[7] JSSC 10
Node (nm)	65	130	90	130
Frequency (GHz)	2.45	1.6	2.2	1.6
Power (μW)	400	352	1300	2000
NF (dB)	9	7.2	13	6.5
Gain (dB)	27.5	41.8	27	42.5
IIP3 (dBm)	-24.5/-21	-35.8	-14_a	-30
IIP2 (dBm)	>0/5	-	-	-
Active area (mm^2)	**0.08**	1.7	0.24	0.57

$_a$Est.

Babak Mohammadi

Dual-V_T Gates for Sub-V_T Circuits

Problems

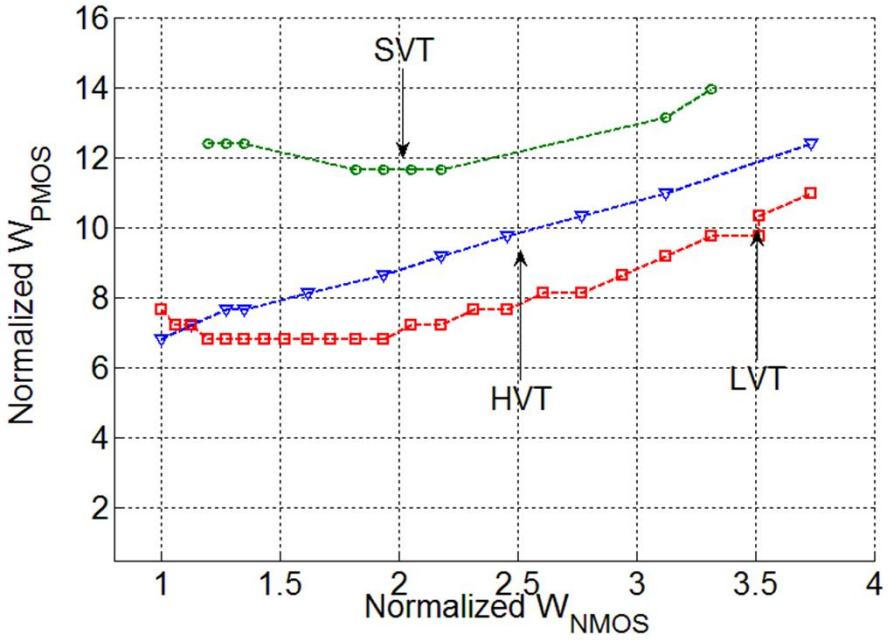
Technologies are not designed for Sub-V_T.

- Large mismatch **between PUN and PDN.**
- **Reduced Noise-Margins**.
- Reduced reliability, and timing properties.
- Transistor sizing is not effective
  - Large area overhead
  - Excessive power consumption.

B1

Transistor sizing

Not as effective as for Super-V_T



Required NMOS and PMOS Width to have balanced driving strength at V_{DD}=300 mV.

Balancing is not feasible with transistor sizing in Sub-V_T!

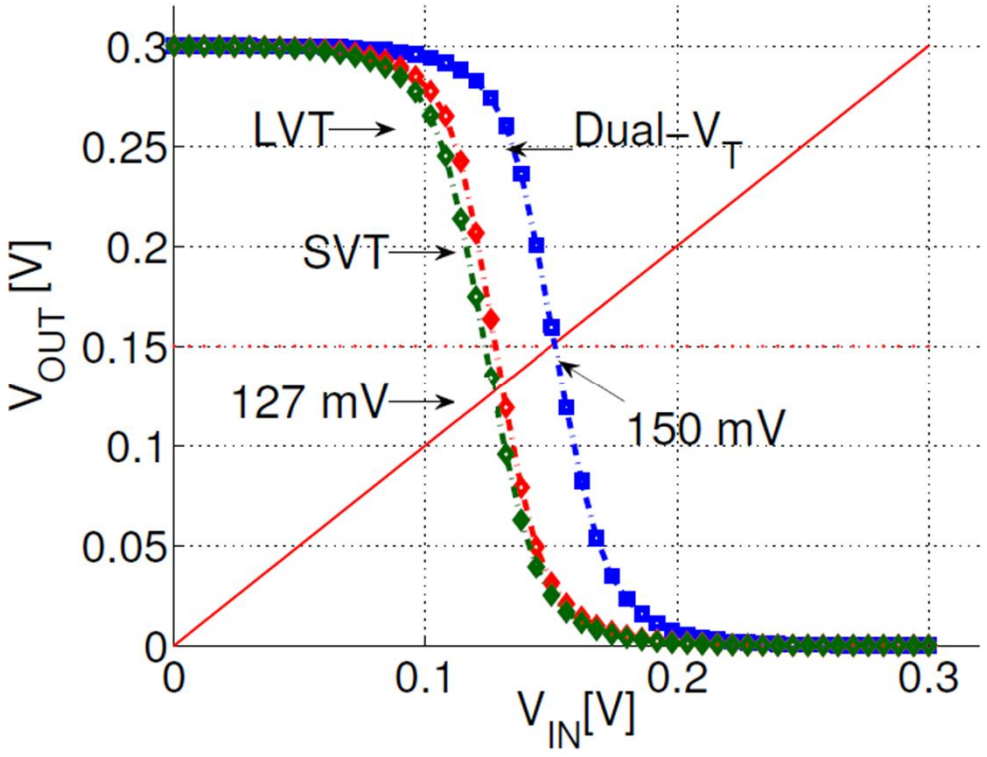
B1 Sub-micron technologies include transistors with different threshold options.

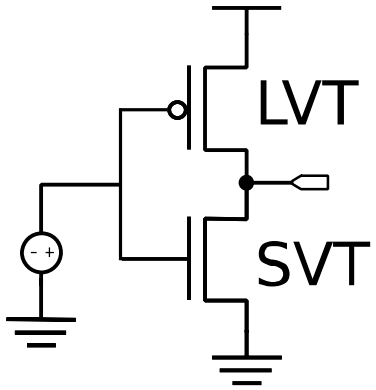
Workflow: Replace the transistors in weak network (PDN or PUN) with low-V-T transistors. The right choice of threshold option depends on the gate's architecture and supply voltage.

Result: Improved Noise-margins, improved timing properties (balanced rise/fall time, tPHL tPLH), improved performance (compared to pure high-VT gates), lower leakage (compared to pure low-VT gates).

BABEK; 2012-09-19

Transfer of inverters



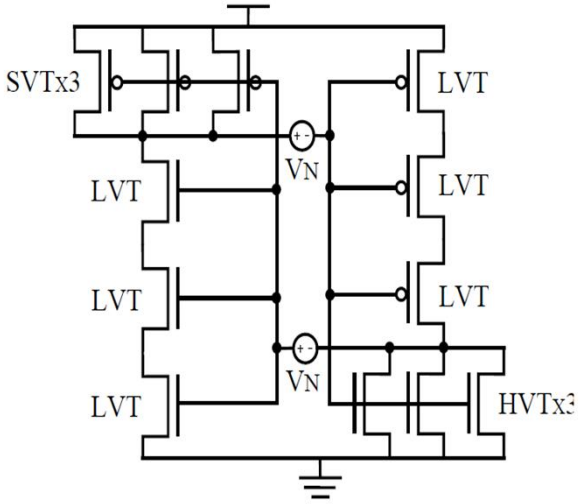


Employing Dual-V_T in inverter.

Noise Margins, Simulation Setup

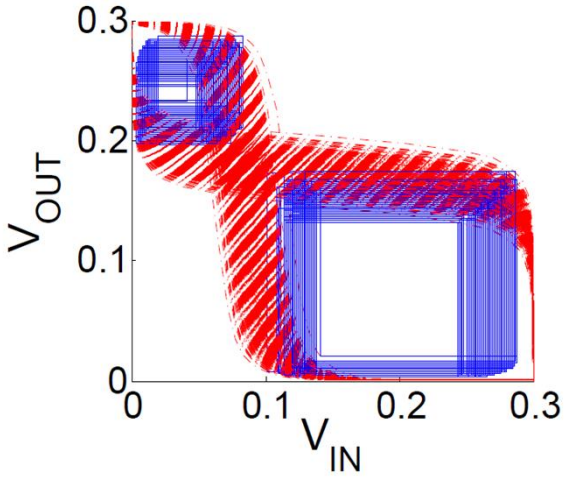
Monte Carlo simulation of NAND3 and NOR3 pair
+ 1000 point, TT corner, V_{DD} =300mV, Temp.=27°C

Schematic

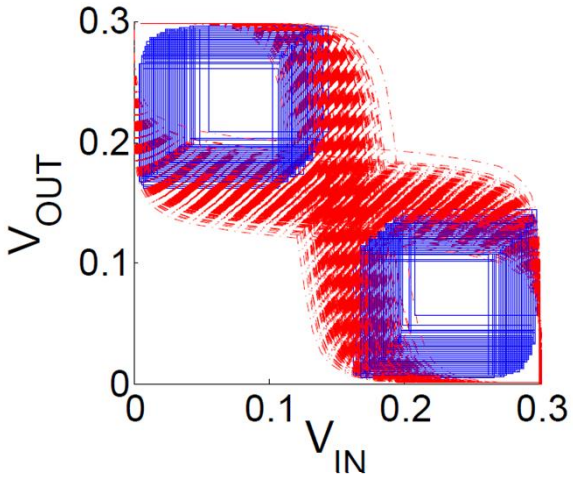


NAND3, NOR3

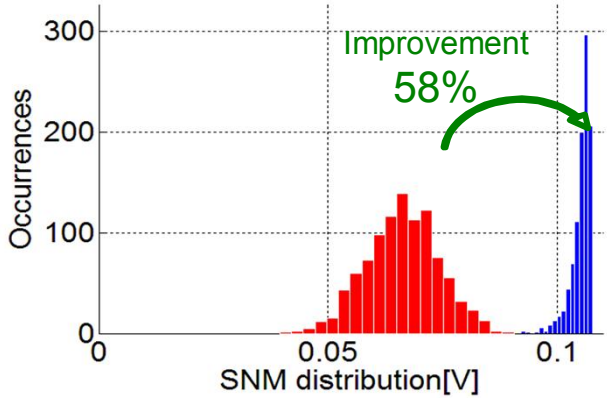
Noise Margins, Results



Standard Cell



Dual V_T
(DVT)

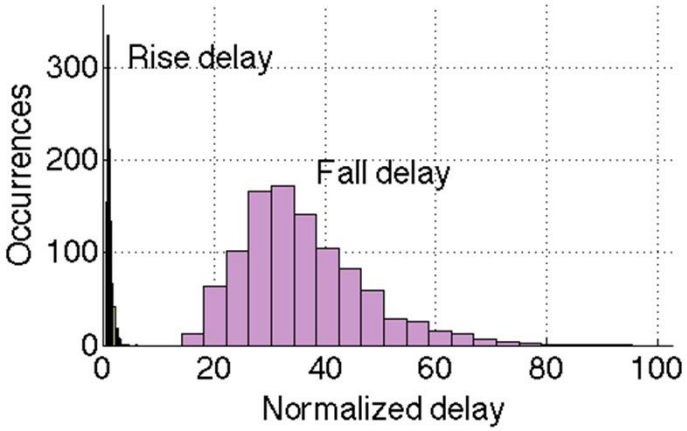


Dual V_T:

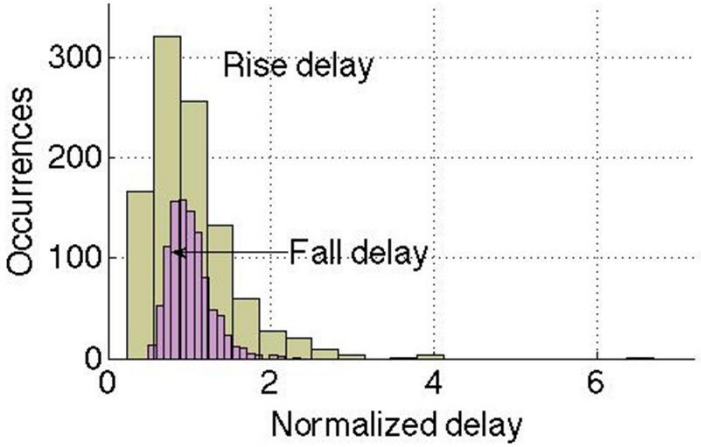
- Higher NM
- Lower NM variation
- Smaller area

Delays

Simulated delay in NAND3
+ 1000 point MC, VDD 300mV, 27°C, TT corner, Fan-out=4



Standard cell



Dual-V_T

Dual-V_T
- Equalized rise/fall delays
- Higher performance

Slide 35

B3 The rise time and fall time of standard cell gates in sub-vt are not the same.
The figure in left shows that DVT has an identical rise-fall delay. But the one in right shows that fall delay is almost 20 times slower than rise delay @ 300mV. Fall delay of HVT NAND3 is 40 times slower than its rise time. These numbers change by supply voltage.
Also, the worst case of DVT is 6 times slower than its mean rise delay. But in figure right, it is 40. It means that we have to run it 40 times slower to consider its worst-case
Babek; 2012-09-21

Summary

Pros
- Increased reliability
- Improved performance
- Reduced area
- Reduced energy dissipation

Cons
- Voltage dependent
- Full-custom

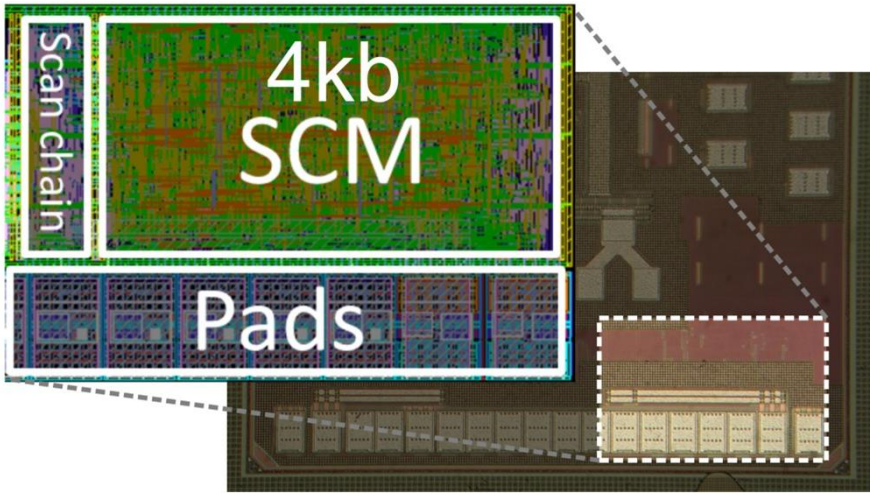
Slide 36

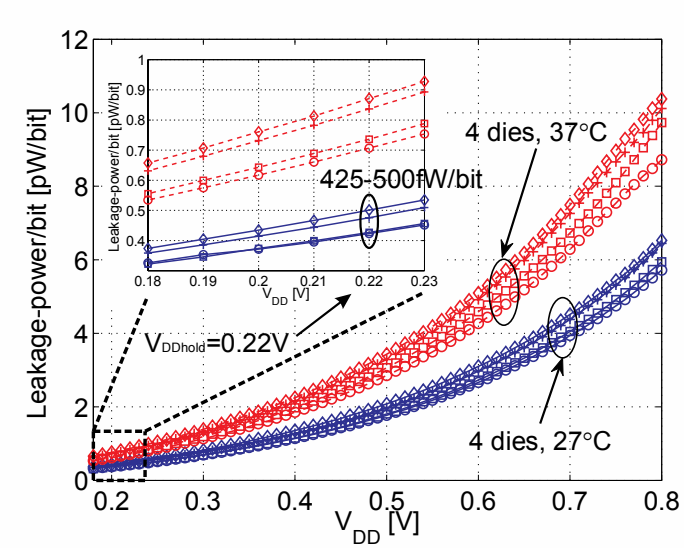
B4 The rise time and fall time of standard cell gates in sub-vt are not the same.
The figure in left shows that DVT has an identical rise-fall delay. But the one in right shows that fall delay is almost 20 times slower than rise delay @ 300mV. Fall delay of HVT NAND3 is 40 times slower than its rise time. These numbers change by supply voltage.
Also, the worst case of DVT is 6 times slower than its mean rise delay. But in figure right, it is 40. It means that we have to run it 40 times slower to consider its worst-case

Babek; 2012-09-21

Oskar Andersson

65-nm Semi-Custom Sub-Threshold Memories





- Increasing demand for memories in ULV/ULP devices.
- Commerical SRAM (6T bitcell) are not operational.
- SRAM for Sub-V_T are costly in engineering effort and power.

Outline

- System Design
  + SSF UPD project overview
  + Transceiver
- Circuit Design
  + Receiver front-end
  + Dual threshold gates
  + Sub-V_T memories
- Questions

Questions