NANO ELECTRONICS GROUP

A single III-V nanowire CMOS inverter

by Anil W. Dey, Johannes Svensson, B. Mattias Borg, Martin Ek, and Lars-Erik Wernersson

Lund University, Sweden
anil@eit.lth.se

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Advantages using nanowires

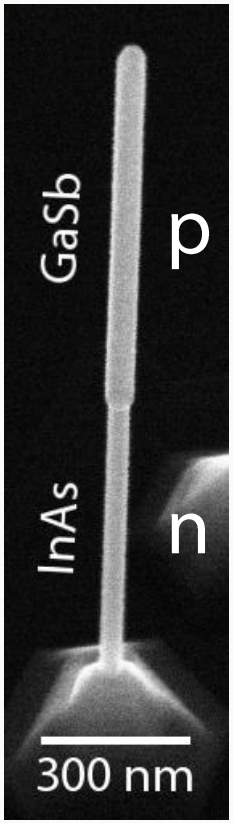
Nanowires offer ideal electrostatics

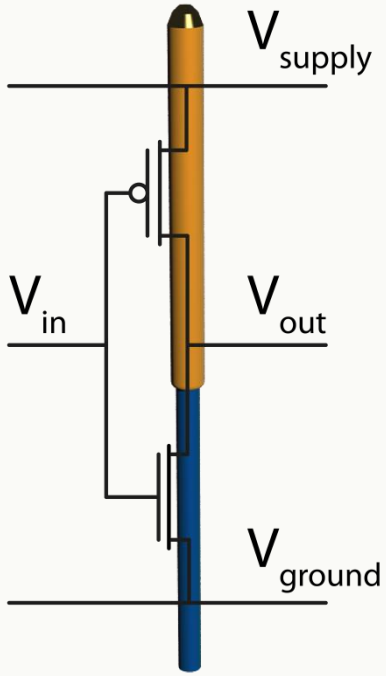
Do not suffer from drawbacks of lattice mismatch

N- and p-type in the same nanowire

Anil W. Dey, Lund University, Sweden
anil@eit.lth.se

CMOS in nanowires





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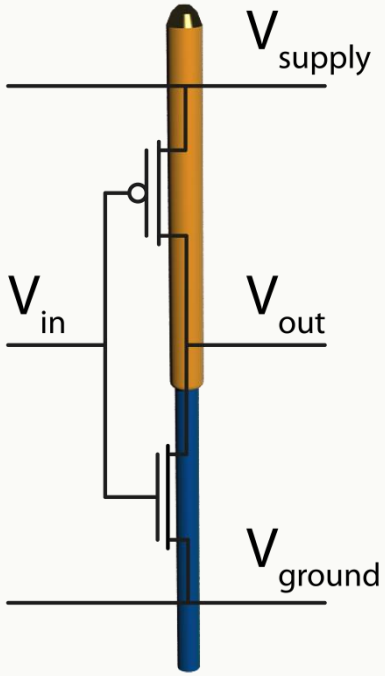

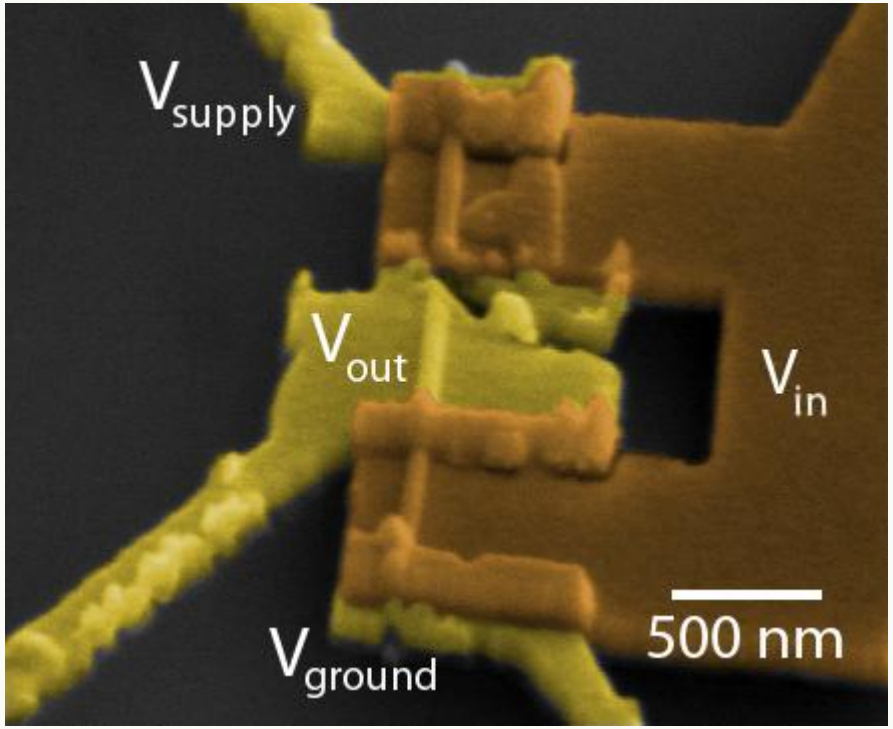

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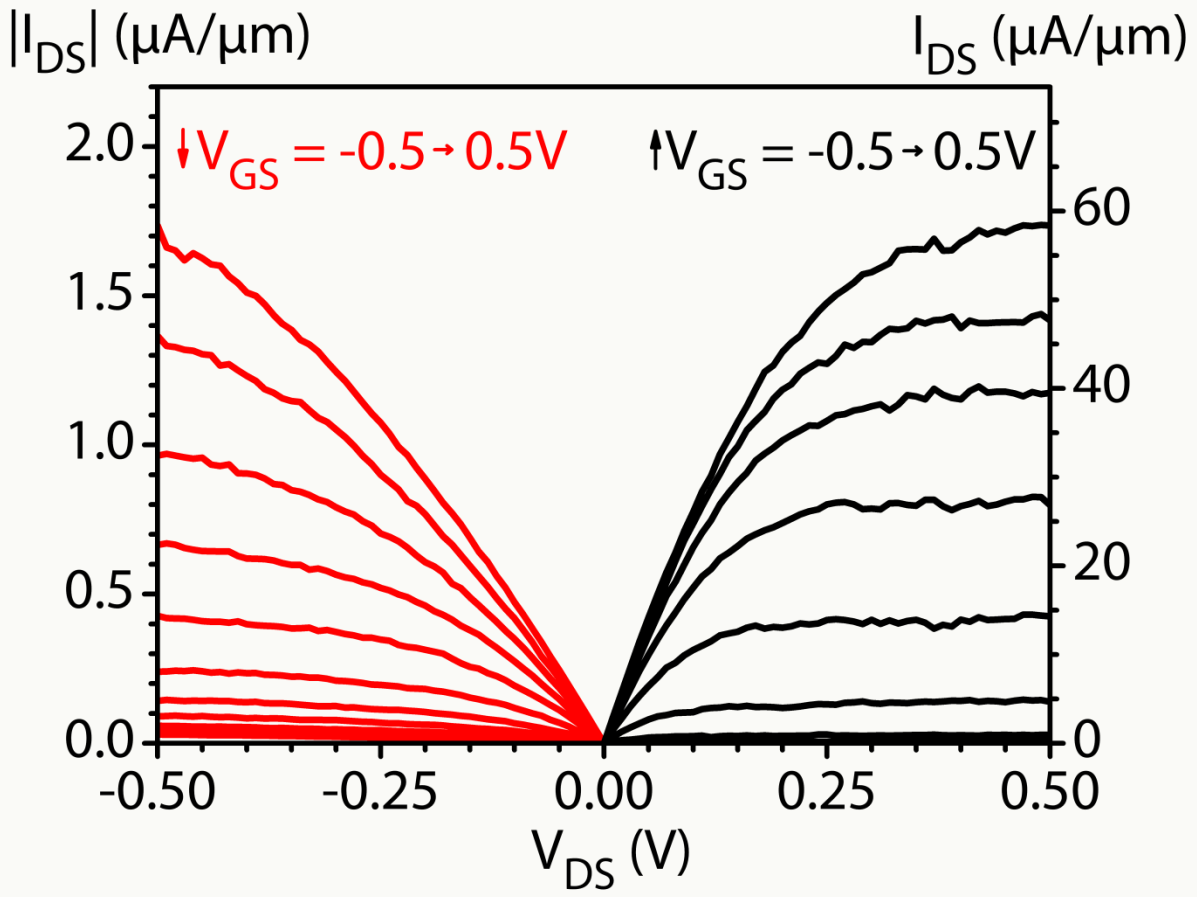
Electrical characterization



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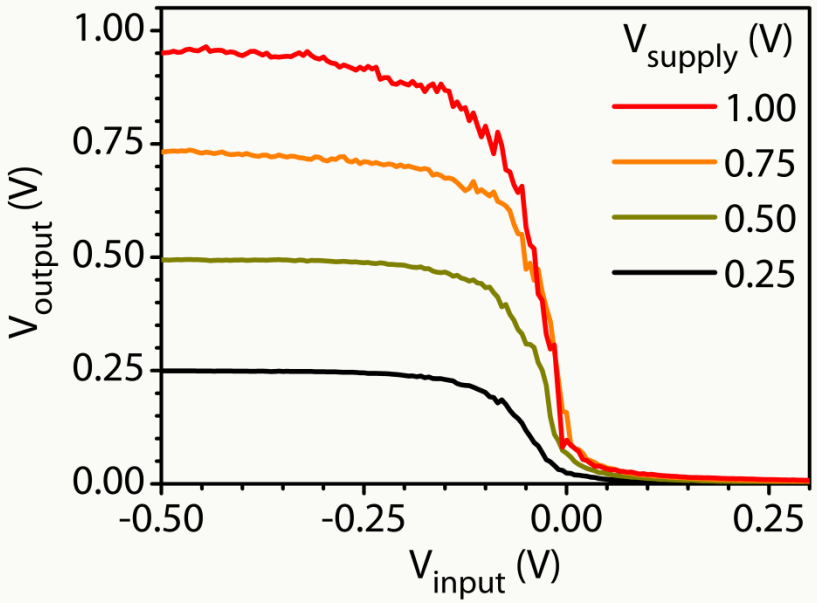
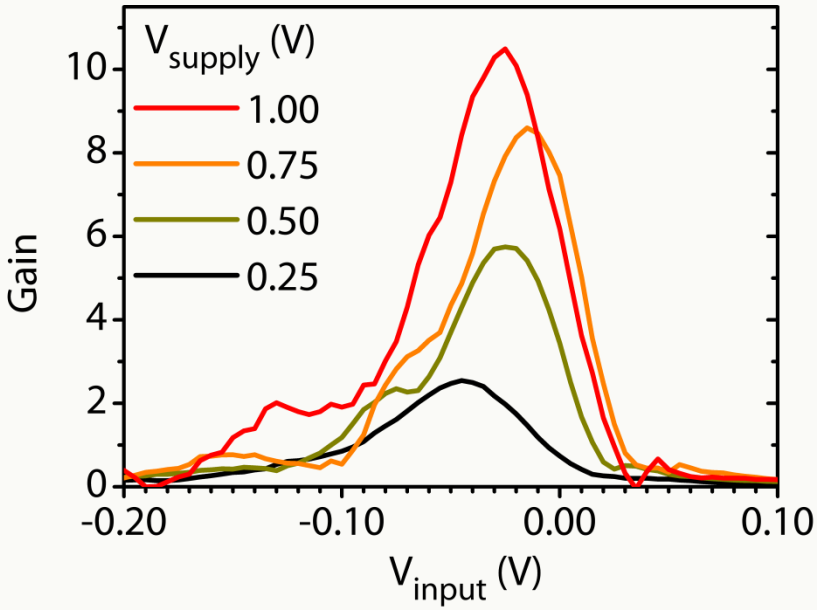
Inverter characteristics





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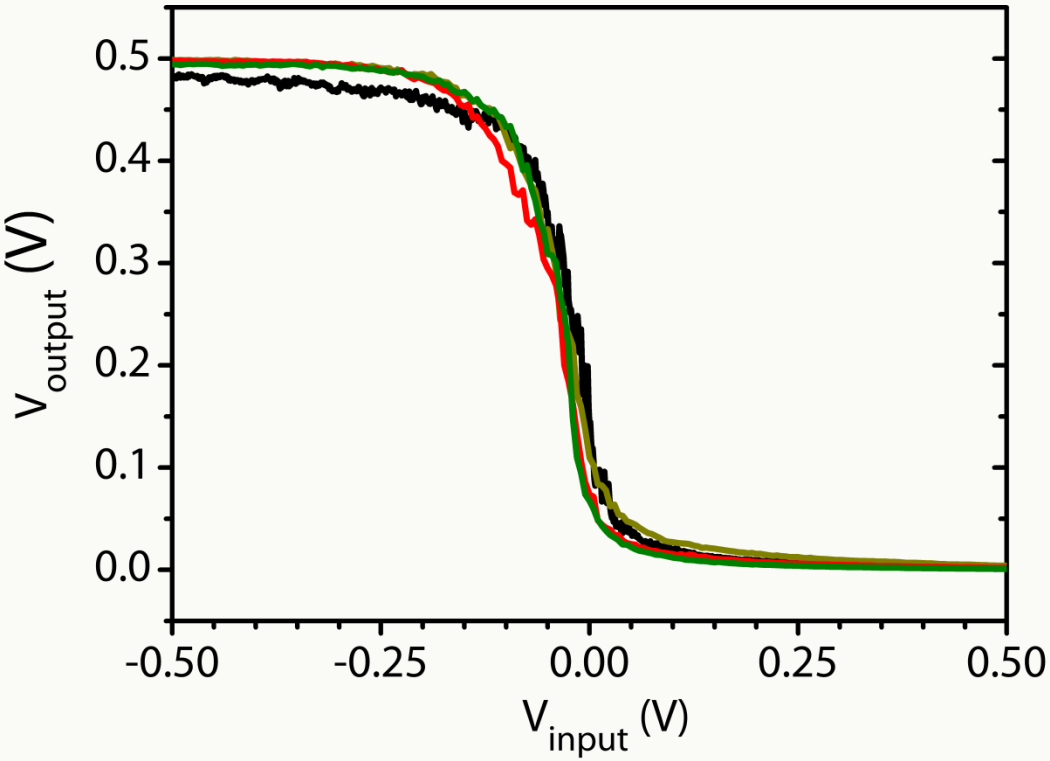
Device variability



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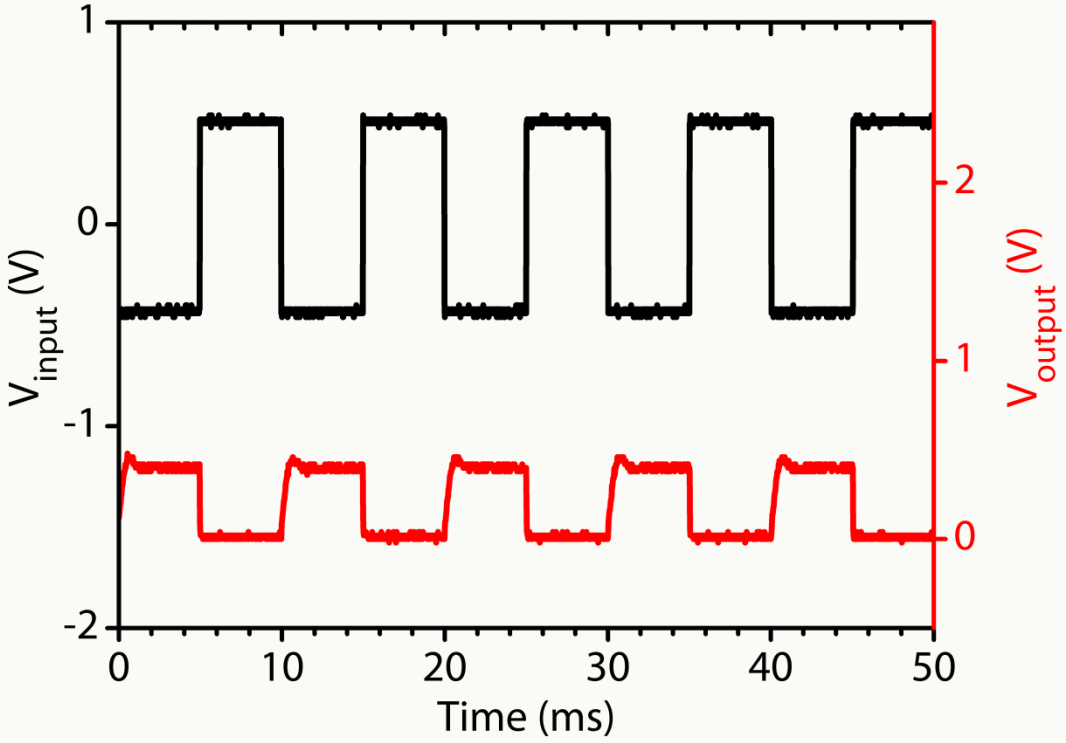
Time-resolved measurements



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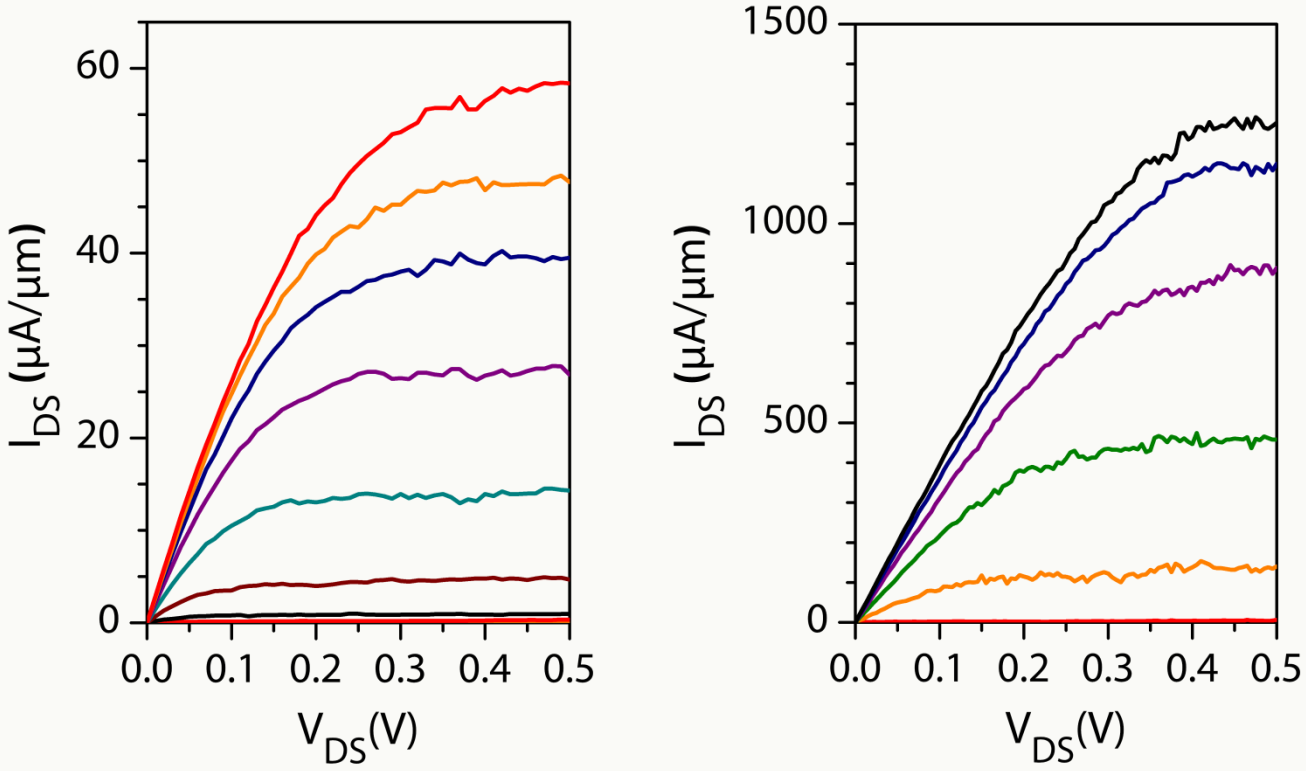
Device scaling



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Outlook

Implementation in a vertical geometry

Reduce parasitics. Scale the devices

Match the pull-up to the pull-down network

Anil W. Dey, Lund University, Sweden
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Thank You.

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anil@eit.lth.se