Low-Power InAs MOSFET RF Circuits

- 60 GHz and Beyond

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Talk Outline

Motivation

Fabrication

- Processing

Measured Data

- Benchmark

Nanowire Roadmap

- Overview
- Benchmark

Simulated Model

- VS Model
- Gate Length and Spacing

Conclusion

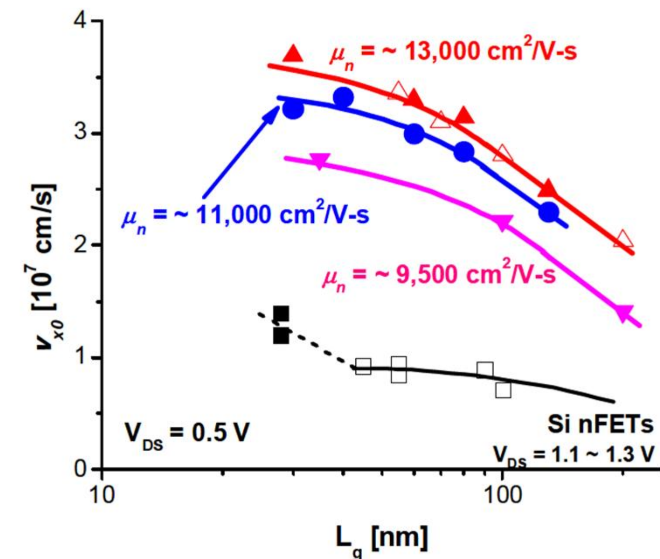
Motivation

NW structure

- Electrostatic scaling advantageous
- Can be grown on Si with a thin buffer

InAs

- High v_{inj} at low V_{DS}
  - High frequency, low power applications
- Formation of excellent ohmic contact
- High current density for thin channels
  - 15 nm InAs NW FET: 1.23 mS/µm (cirumference norm.) and 140 mV/decade at V_{DS} = 0.5 V†



†) A. Dey et al., *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 791-793, Jun 2012
‡) D.-H. Kim, et al., *IEDM 2009*, vol., no., pp. 35.4.1 - 35.4.4, 7-9 Dec. 2009.

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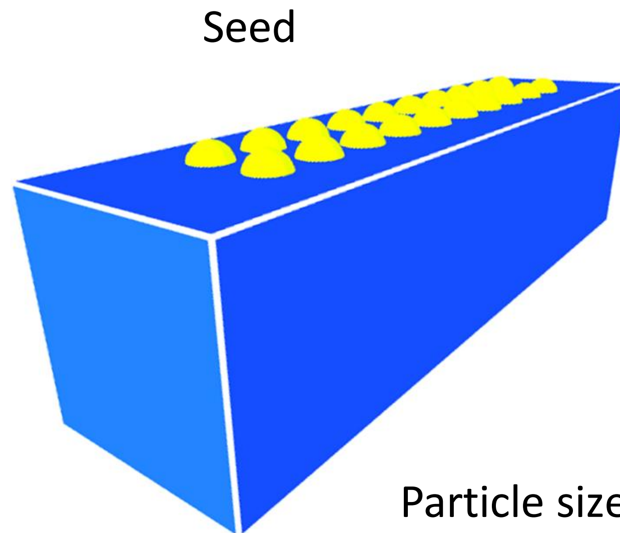
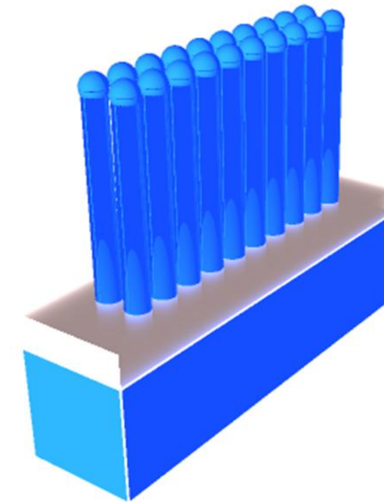
Bottom Up

$n_{NW} = 20$
D = 50-15 nm

Seed



Growth



Particle size
Particle placement

$W = n_{NW}\pi D$

…and the rest is conventional top down.

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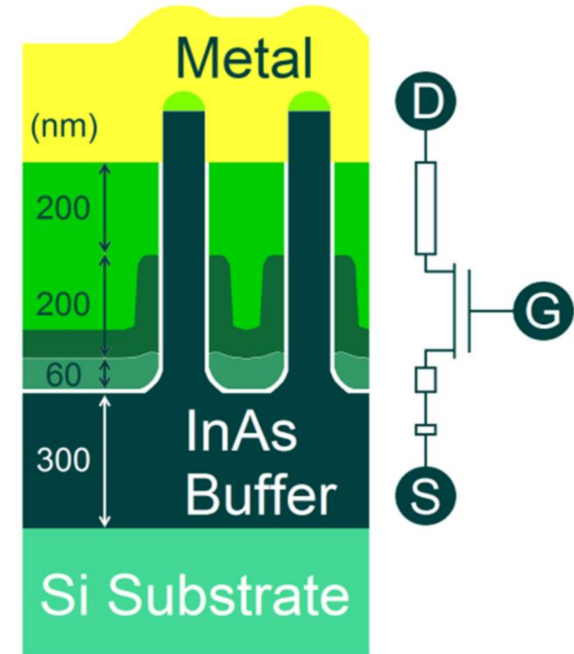
Schematic Fabrication

Seed and Growth

High-κ ALD

Si_3N_4 PECVD

Sidewall Removal

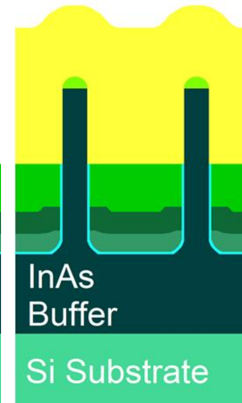


W Sputtering

Gate Definition

Resist Coating

Top Metal Sputtering



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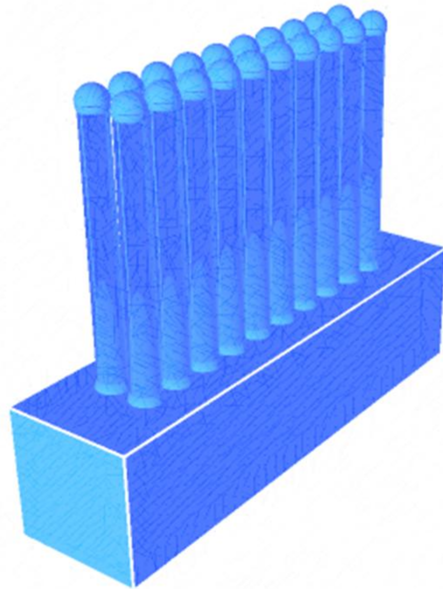
Single NW Performance

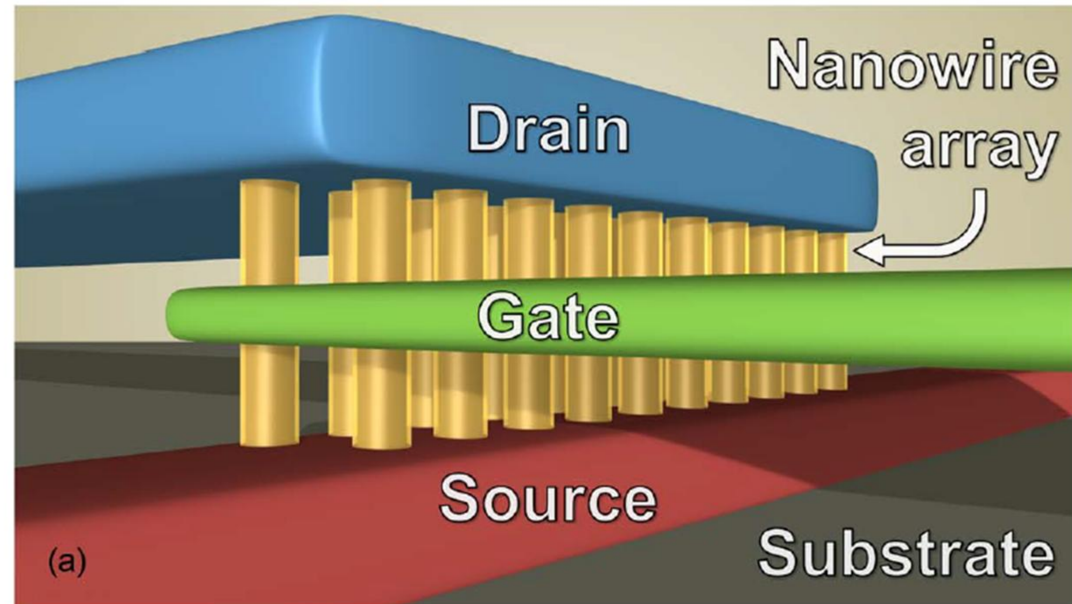
State of the Art Technologies @ V_{DS} = 0.5 V

D (nm)	L_G (nm)	I_{ON} (mA/µm)	$g_{m,max}$ (mS/µm)	SS (mV/dec)	Tech	Reference
28	200	0.058	0.15	140	vertical NW	This work
45	200	0.67	1.19	560	vertical NW	This work
15	100	0.6	1.23	140	lateral NW	A. Dey et al EDL 2012
10	30	0.7	1.9	80	HEMT	D.-H. Kim et al EDL 2008
30	250	0.12	0.56	120	FinFET	J. J. Gu et al APL 2011
10	75	0.55	1.75	95	QWFET	M. Radosavljevic et al IEDM 2009
25	170	0.4	0.8	260	radial NW	X. Jiang et al Nano Lett 2007
13	230	0.9	1.72	180	XOI	K. Takei et al APL 2011

†) K.-M. Persson, et al., *IEEE Device Research Conference (DRC), 2012*, vol., no., pp. 195-196, 18-20 June 2012.

Nanowire Roadmap

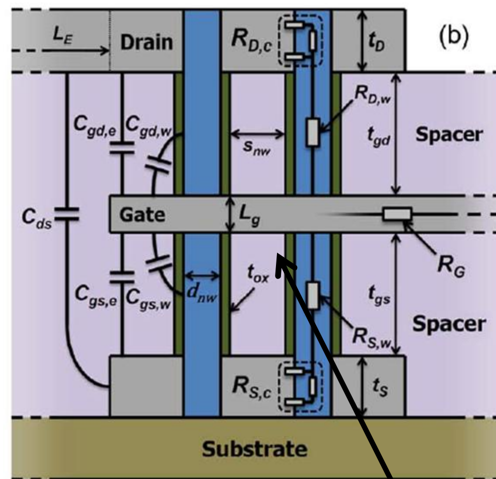


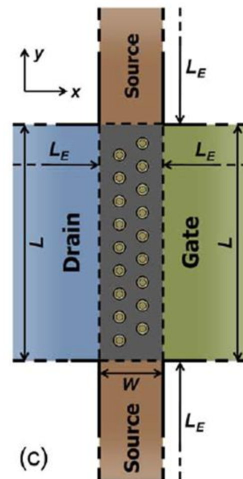


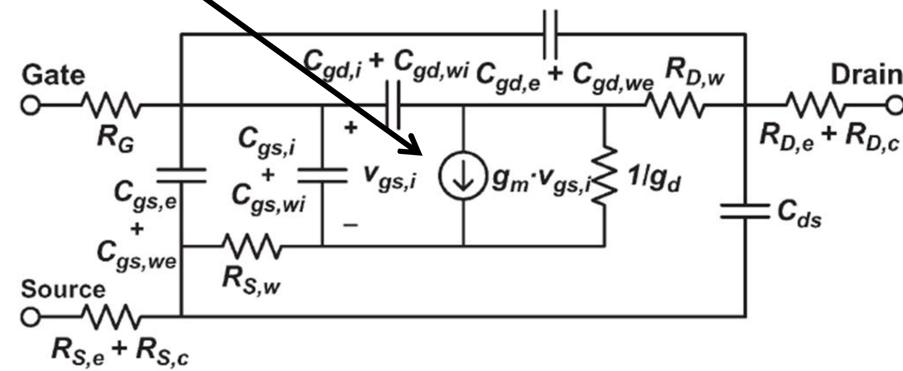
†) K. Jansson, et al., *IEEE Trans. Electron Devices.*, vol. 59, no. 9, pp. 2375–2382, Sep. 2012.

Nanowire Roadmap

Intrinsic perfomance taken from physical simulations made with Tight Binding







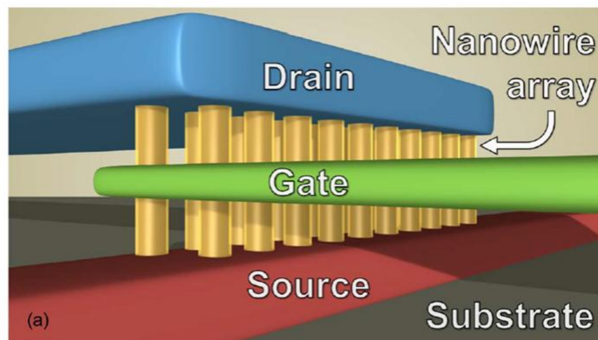
Packing NWs more dense reduces fringing capacitance

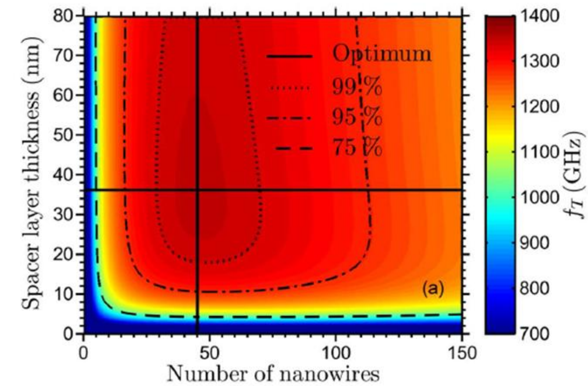
†) K. Jansson, et al., *IEEE Trans. Electron Devices.*, vol. 59, no. 9, pp. 2375–2382, Sep. 2012.

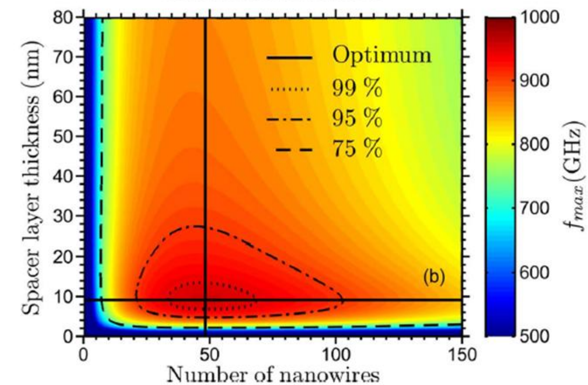
Nanowire Roadmap

TABLE V
ROADMAP OF OPTIMIZED TRANSISTOR STRUCTURES

Node	NWs	L_g (nm)	s_{nw} (nm)	$t_{gs,gd}$ (nm)	$t_{S,D}$ (nm)	f_T (GHz)	f_{max} (GHz)
50 nm	8x8	67.3	60.0	36.5	150	440	380
35 nm	7x8	47.1	42.0	25.6	105	800	640
22 nm	7x7	29.6	26.4	15.8	66	1380	1040
16 nm	7x7	21.5	19.2	11.5	48	1670	1200
12 nm	7x7	16.1	14.4	7.9	36	1730	1230
8 nm	7x7	11.1	10.0	5.1	24	2720	1790







†) K. Jansson, et al., *IEEE Trans. Electron Devices.*, vol. 59, no. 9, pp. 2375–2382, Sep. 2012.

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Nanowire Roadmap

TABLE VI
BENCHMARKING OF PARASITIC ELEMENTS

Node	L_g (nm)	InAs nanowire transistor $C_{gg,i}$ (aF/μm)	$C_{gg,t}$ (aF/μm)	$R_{S,D}$ ($\Omega\mu$m)	ITRS Roadmap[a] $C_{gg,i}$ (aF/μm)	$C_{gg,t}$ (aF/μm)	$R_{S,D}$ ($\Omega\mu$m)
50 nm	67.3	460	770	42	1010	1180	190
35 nm	47.1	360	690	49	770	1010	180
22 nm	29.6	290	620	59	610	850	200
16 nm	21.5	230	570	71	530	740	200
12 nm	16.1	220	570	85	420	600	190
8 nm	11.1	130	500	115	300	480	170

[a] Interpolated data from the ITRS roadmap [26].

†) K. Jansson, et al., *IEEE Trans. Electron Devices.*, vol. 59, no. 9, pp. 2375–2382, Sep. 2012.

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Nanowire Roadmap

TABLE I
INTRINSIC TRANSISTOR PARAMETERS

Node (Diameter)	L_g (nm)	$C_{gg,i}$ (aF/NW)	g_m (S/mm)	g_d (S/mm)	μ_i (cm^2/Vs)
50 nm	67.3	71.4	1.71	0.171	9370
35 nm	47.1	40.0	2.88	0.288	6200
22 nm	29.6	19.7	4.86	0.486	3460
16 nm	21.5	11.8	5.77	0.577	2200
12 nm	16.1	8.20	6.12	0.612	1350
8 nm	11.1	3.20	7.14	0.714	508

†) K. Jansson, et al., *IEEE Trans. Electron Devices.*, vol. 59, no. 9, pp. 2375–2382, Sep. 2012.

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VS Model

Virtual Source Semianalytical Compact Modeling

$$I_D/W = Q_{ix_o} v_{x_o}$$

$$Q_{ix_o} = C_{\text{inv}} n\phi_t \ln\left(1 + \exp \frac{V'_{GS} - (V_T - \alpha\phi_t F_f)}{n\phi_t}\right)$$

Drift and ballistic transport

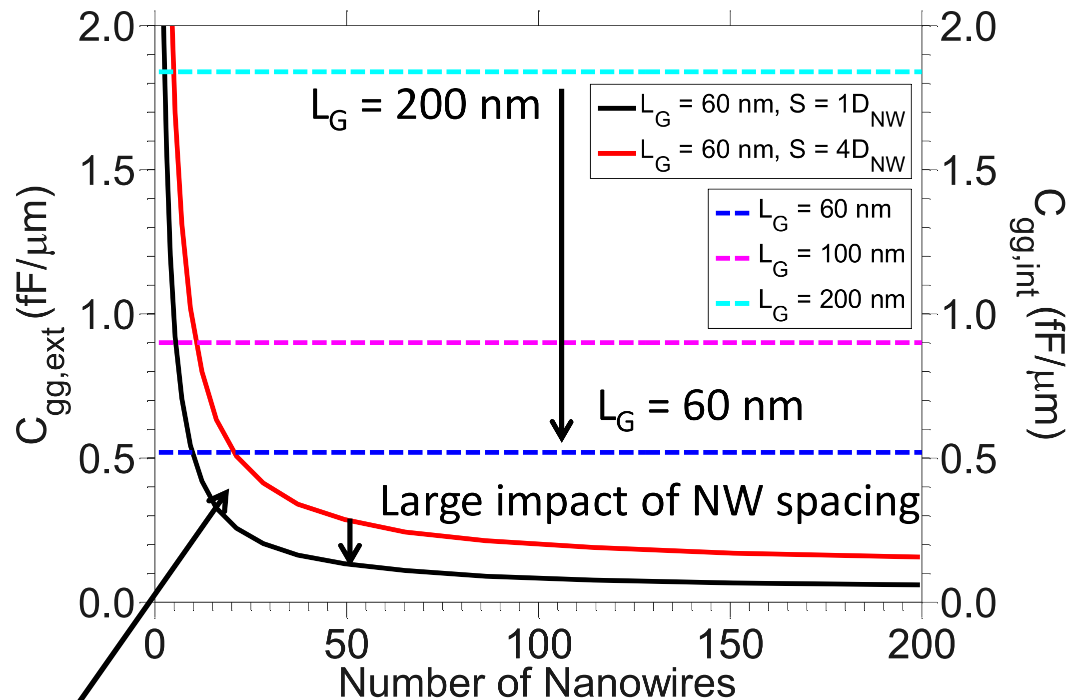
Fitted parameters

- $\mu_{low\text{-}field}$
- R_{series}
- $n \cdot V_{Thermal}$
- v_{inj}

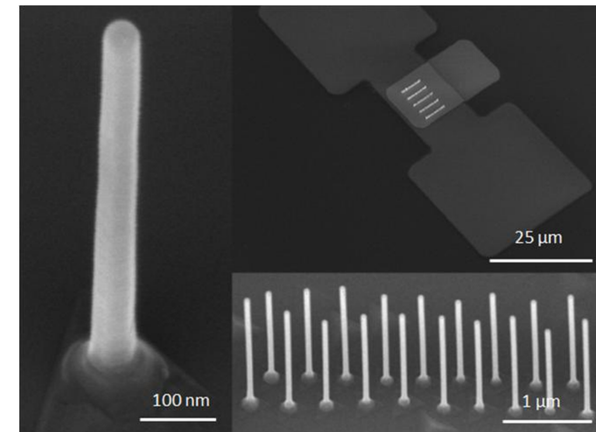
Cadence simulation can be performed with coherent intrinsic C_{gg} computation using an analytical derivative of above expression

A. Khakifirooz et al., *IEEE Trans. Electron Devices*, vol. 56 , no. 8, pp. 1674-1680, Aug 2009

NW Spacing



$C_{gg,ext}$ > 5 fF/µm for 192 NWs



$C_{gg,ext}$ sets lower limit for number of parallel NWs

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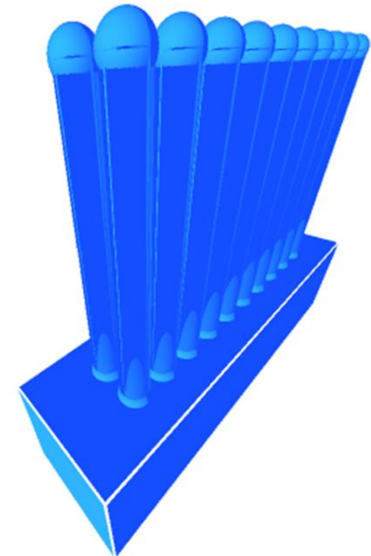
Conclusions

RF Performance

- High frequency 1 dB BW at low power
- Terahertz operation

Down the Road

- NW roadmap suggest packing arrays tight will decrease $C_{gg,ext,}$ making $C_{gg,tot}$ competative with CMOS
- Scaling will further enhance III-V performance as ballistic transport is ruled by v_{inj}



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