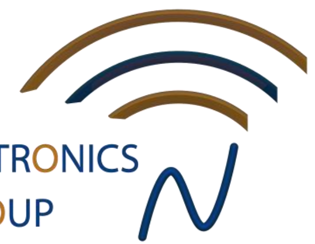
III-V MOSFETs for RF Applications

LARS-ERIK WERNERSSON

Current Trends in Device Scaling

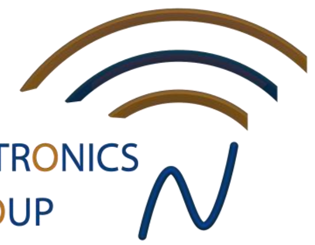


Transistor Innovations Enable Technology Cadence

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

- Strained Silicon
- High k Metal gate
- Tri-Gate

Current Trends in Device Scaling

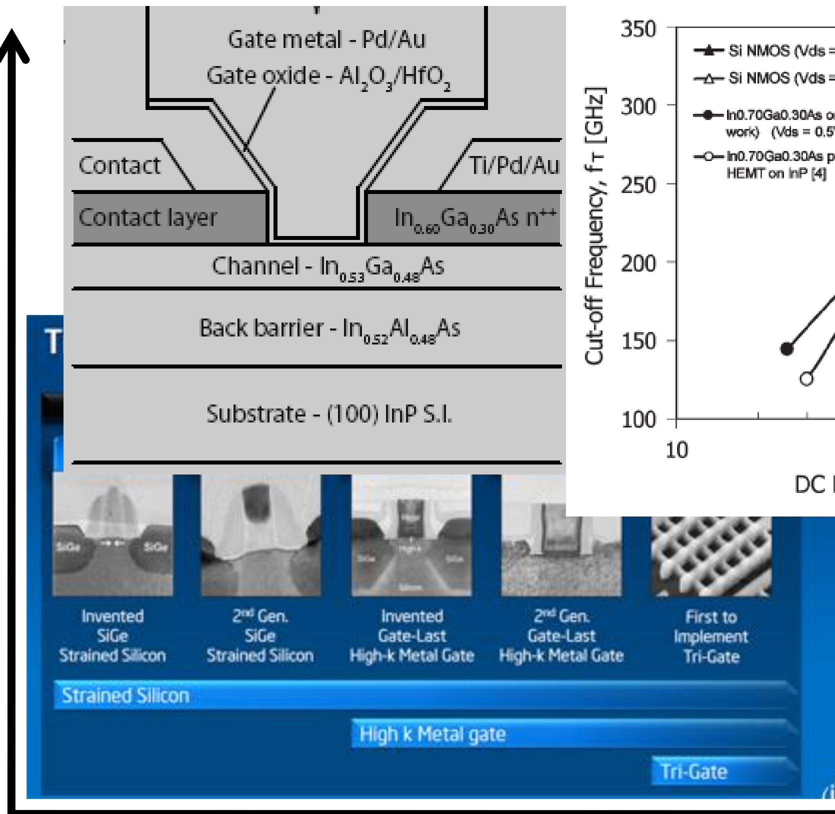


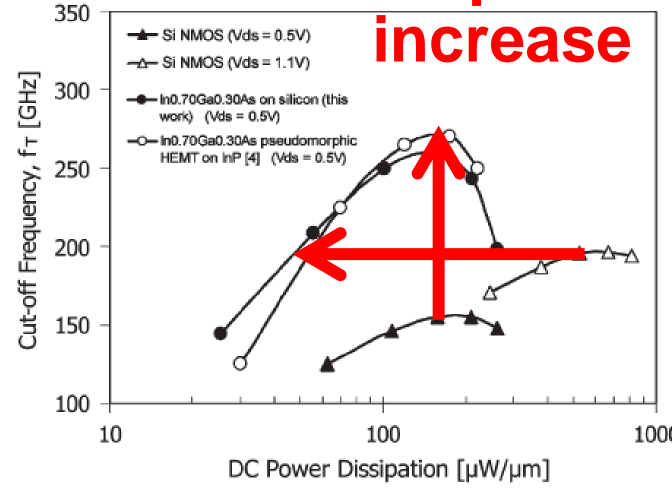
Transport Enhancement

Graphene

III-Vs

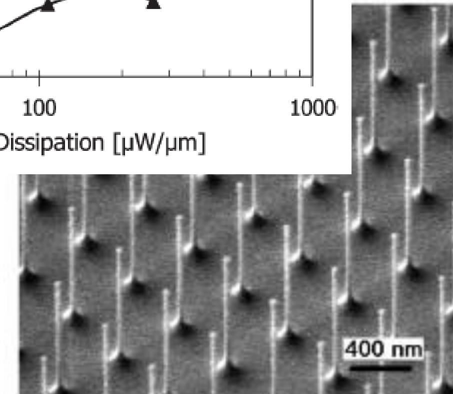
Strained Si





X2 performance increase

x10 power reduction



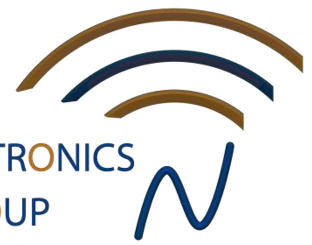
Electrostatics

Planar Technologies

FinFets Trigates

Nanowires

Motivation



- III/V MOSFETs are considered for integration in digital logic
- III/V MOSFETs may have advantages for RF-applications
    - Gate isolation
    - Single supply voltages
    - Reduced Power Consumption *(quantification needed)*
- Drive current is limited by the access resistance
- Scaling scenarios targets R_{access} of 145-228 Ωμm at the15 nm node

=> Need for regrown (MOCVD) source and drain contact layers.

Outline

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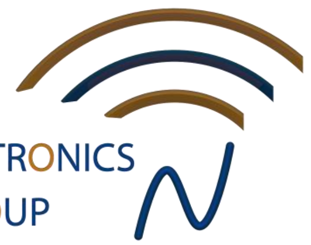
- Motivation
  - MOSFET design criteria
- DC results
- RF characterisation
- Wavelet Generators (mm-Wave Circuits)
- Summary

MOSFET Design Criteria

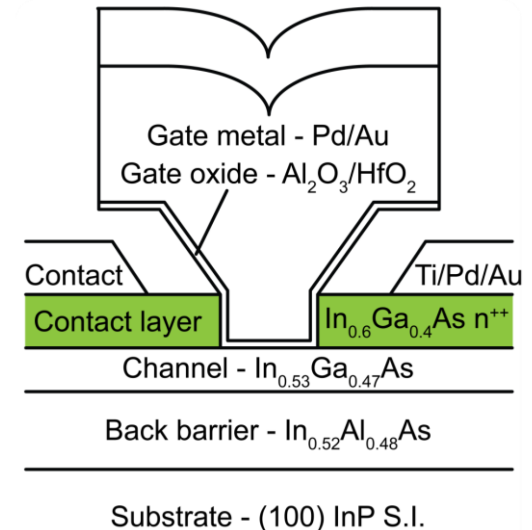


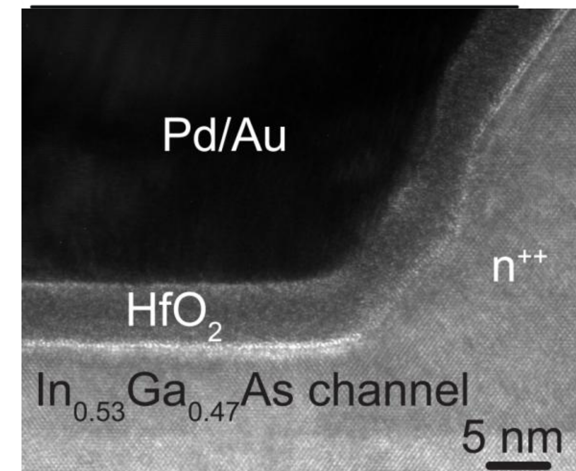
Low on-resistance (R_{ON})

- High injection velocity → $In_{0.53}Ga_{0.47}As$
- Avoid heterostructure access regions → Epitaxial regrowth
- Minimize R_{access} → Self-alignment → Thin S/D spacers
- Scalable L_g → Surface channel
- High-Quality Dielectric → Gate-last process

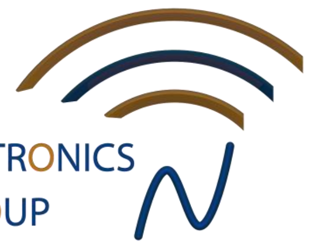
High frequency compatibility

- Trade-off between R_{ON} and $C_{G,par}$

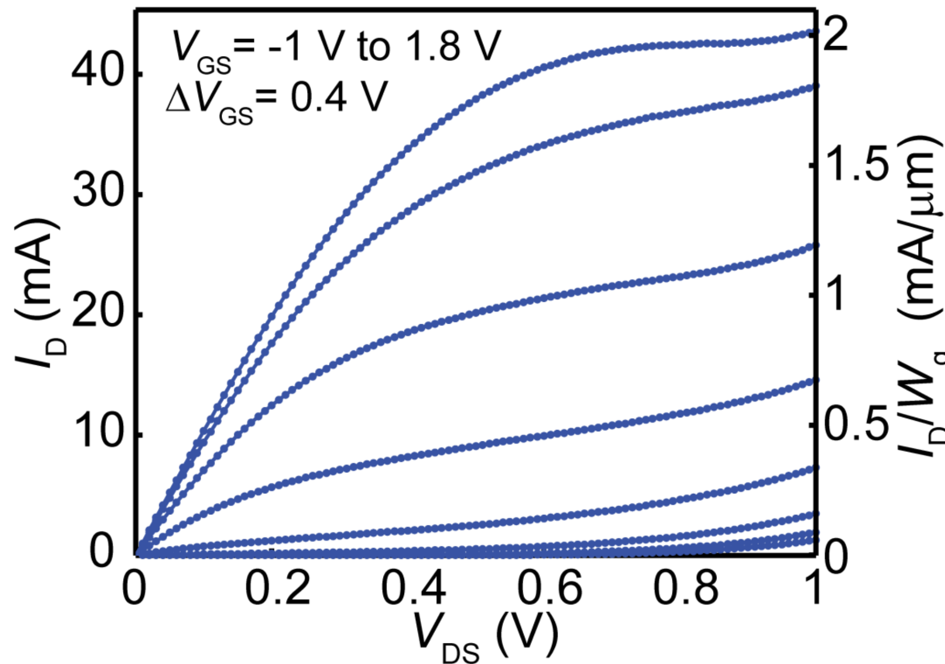




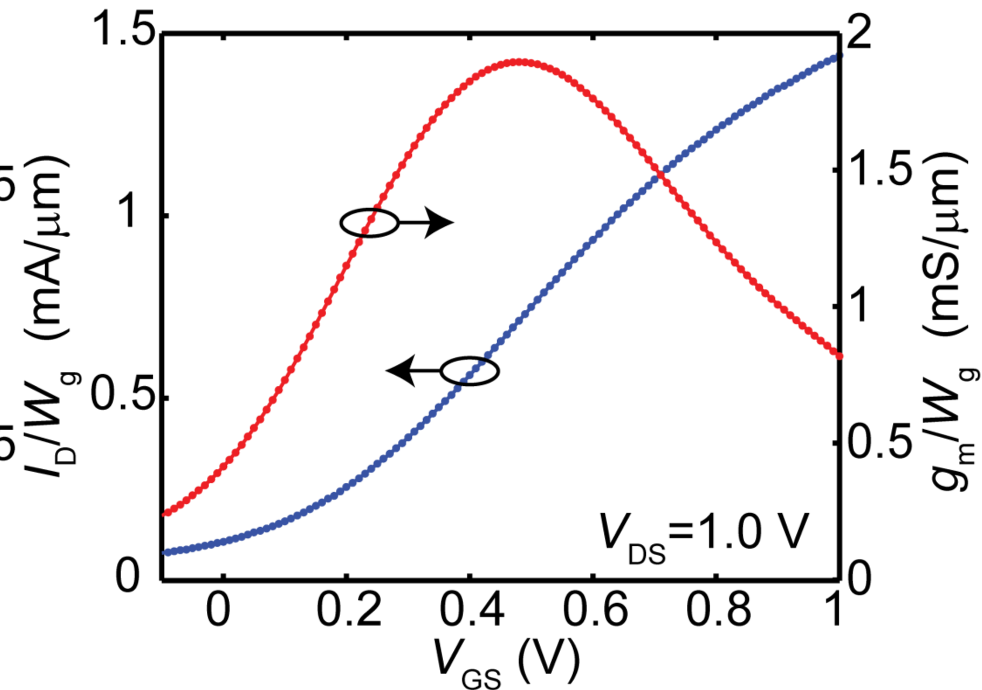
DC Characterization L_g=55 nm



Output characteristics

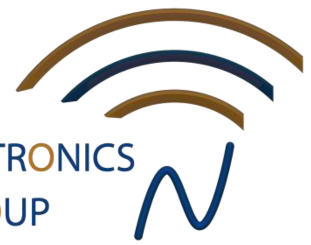


Transfer characteristics

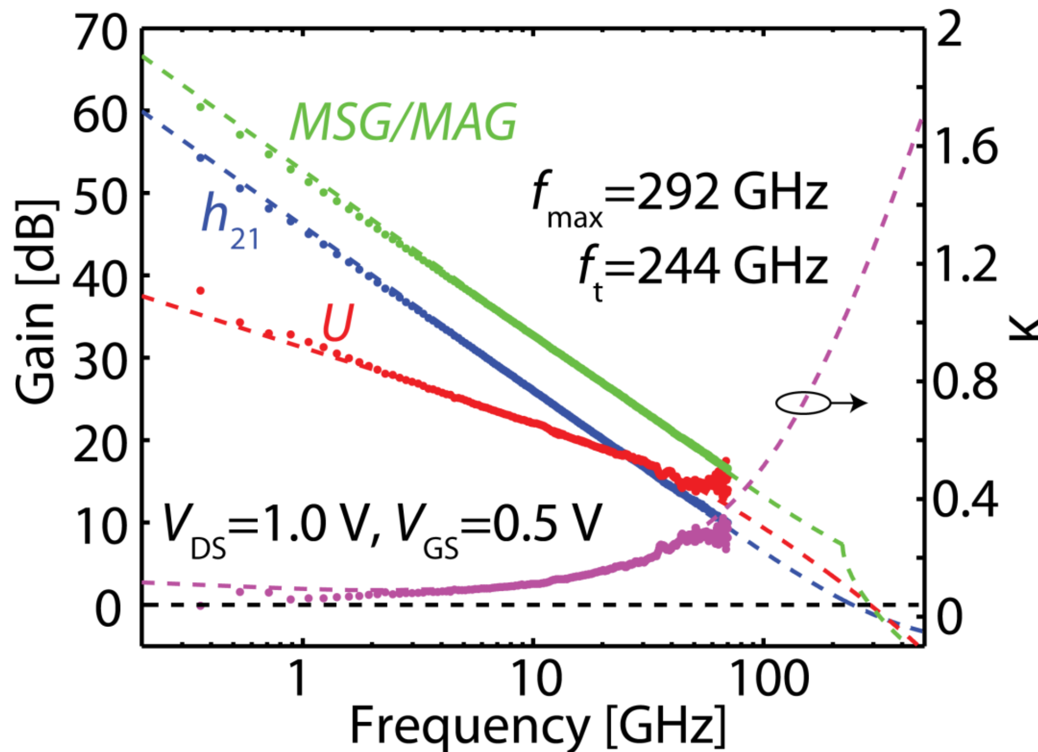


R_{on}=199 Ωµm, max I_d=2.0 mA/µm, max g_m=1.9 mS/µm

S-parameter Characterization



- L_g=55 nm, W_g=21.6 μm device characterized to 70 GHz
- Modeling accounts for impact ionization and border traps



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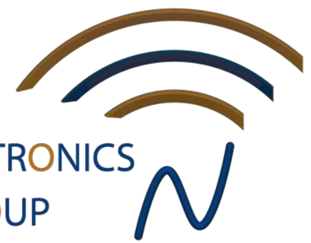
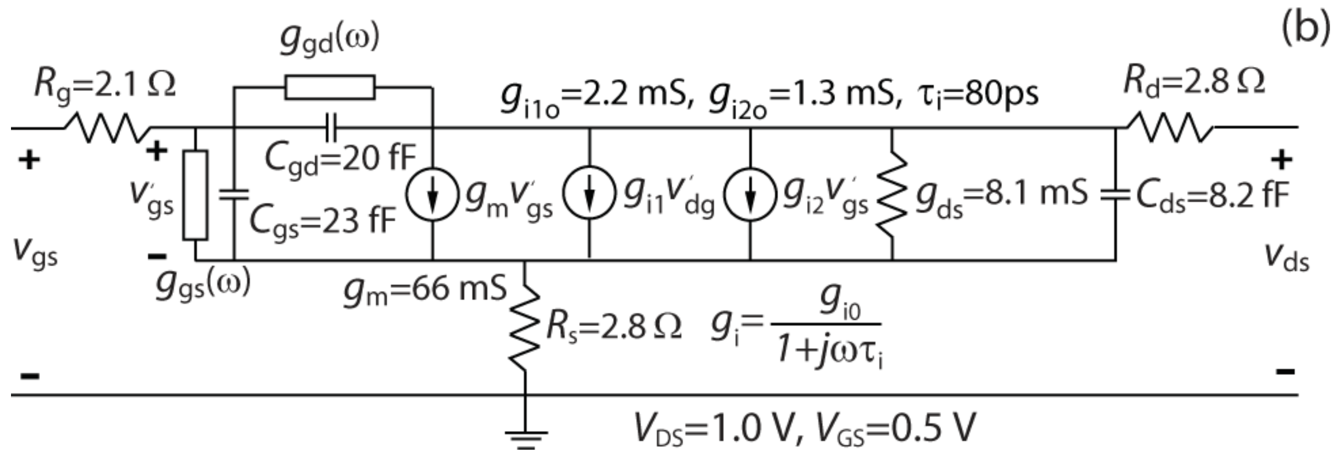
S-parameter Characterization



Small-signal model includes effects related to impact ionization, band-to-band tunneling and conduction via border traps



C_{gd1}=7.2fF

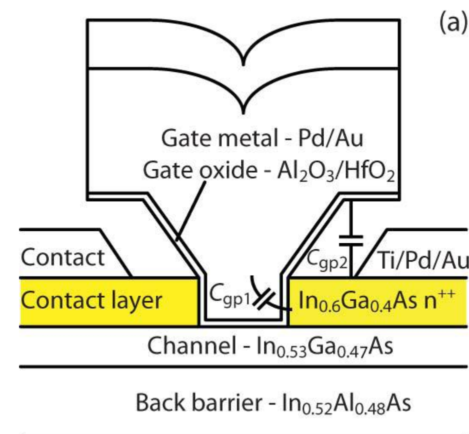
C_{gd2}=19 fF

g_{mint}=3.0 mS/µm

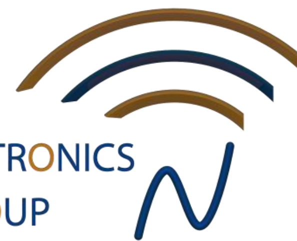
Frequency dependent g_m!

Border traps 9x10^{19} cm^{-3}

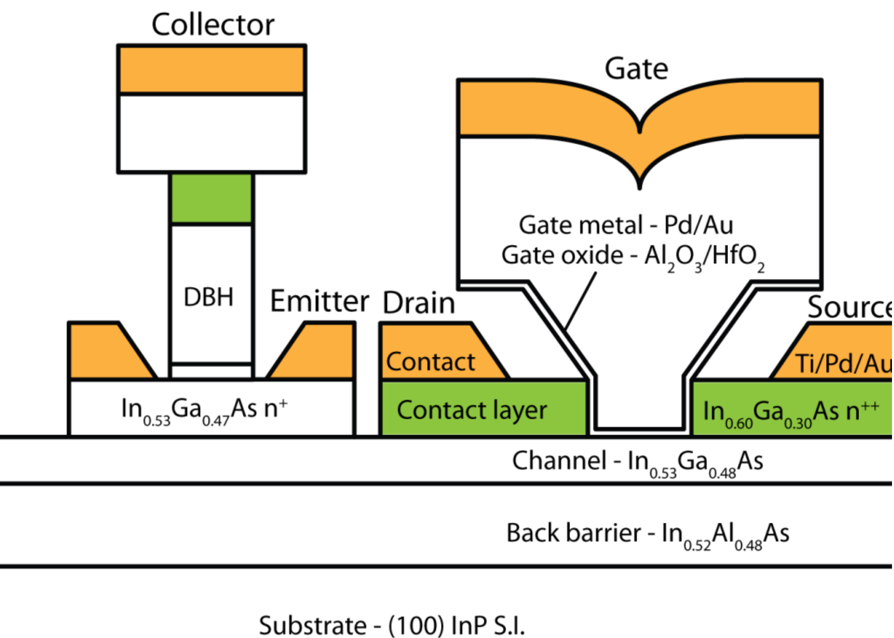
Johansson et al IEEE T-ED 2012 submitted

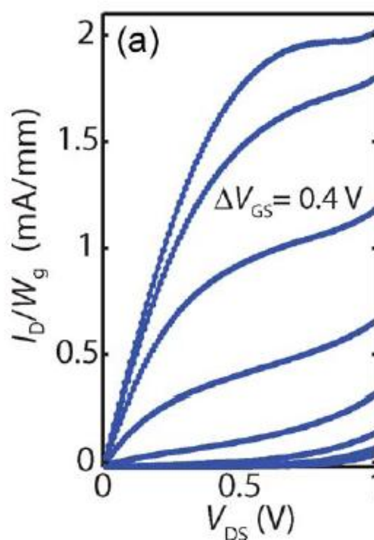


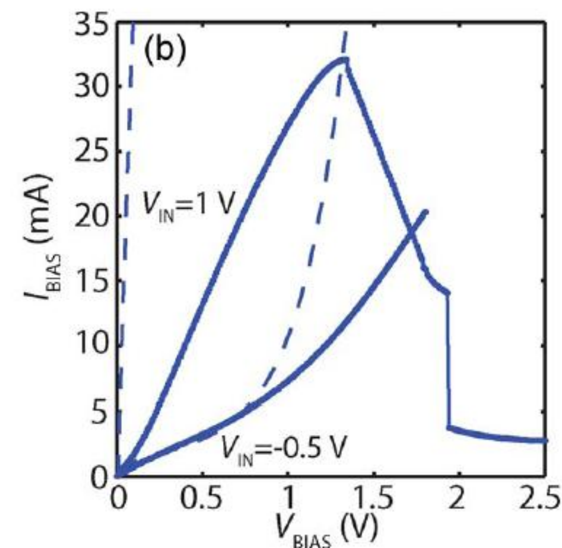
III-V MOSFET/RTD Integration



Co-integration of InP/InGaAs MOSFET and RTD on SI InP Substrate







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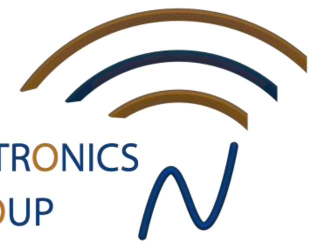
Low R_{on}=199Ωcm

High I_{on}=2.0mA/µm

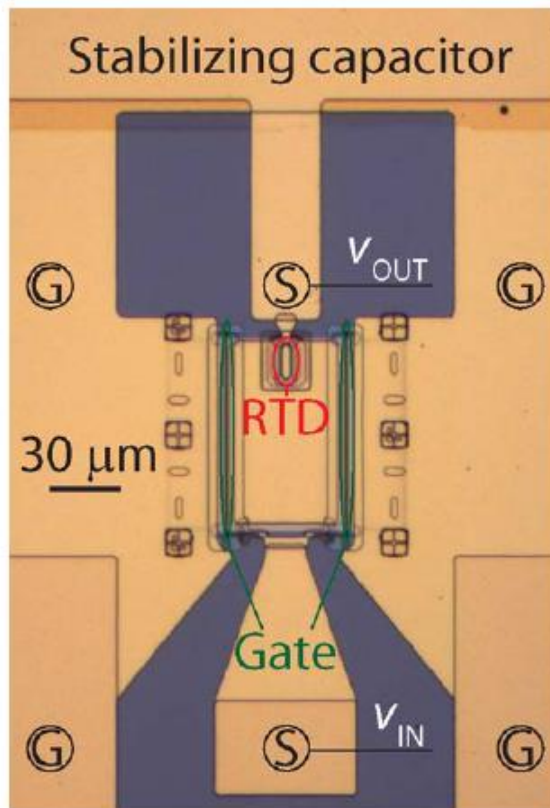
High g_m=1.9mS/µm

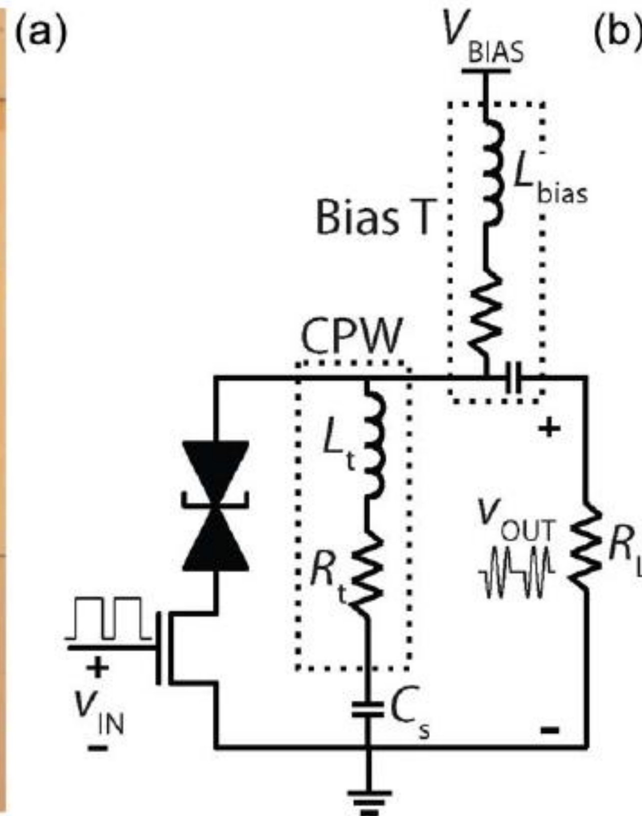
2nd Generation Wavelet Generator



The MOSFET is used to switch the oscillator current

The inductance is given by a coplanar waveguide (CPW) stub





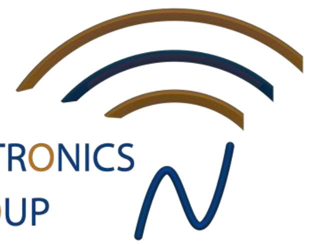
L_t=22 pH

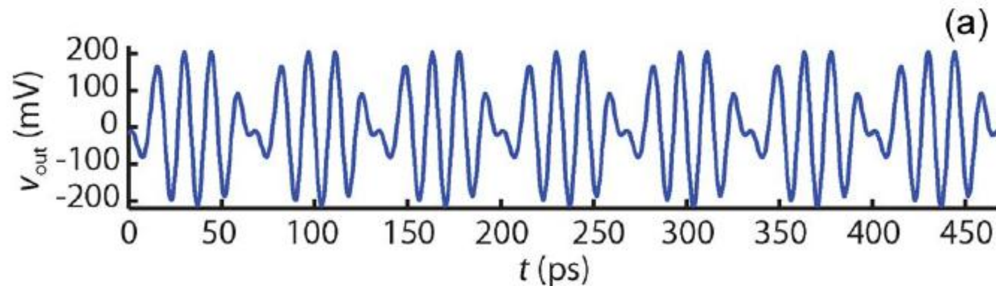
C=4.5 fF/µm^2

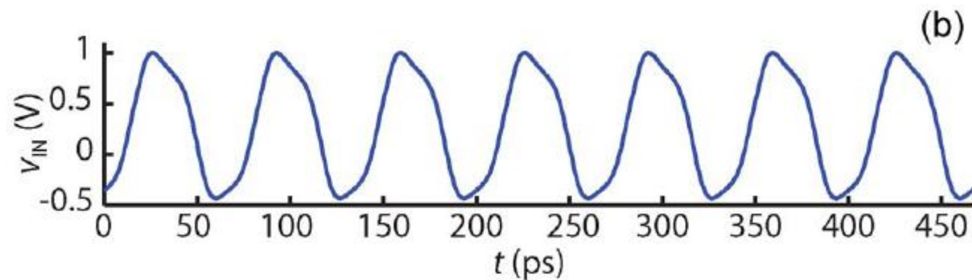
A=2.2x22 µm^2

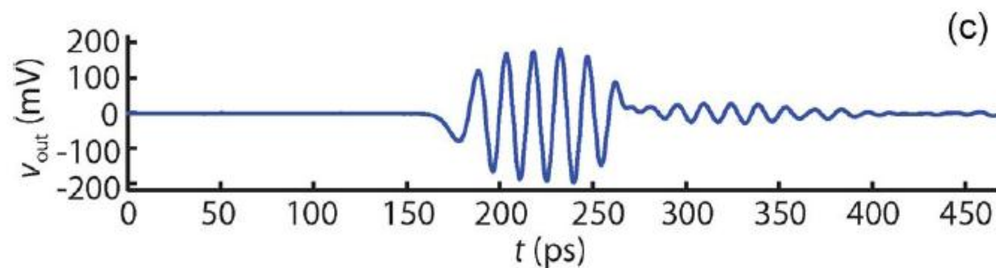
g_{min}=-120 mS

2nd Generation Wavelet Generator









f_0=70 GHz

t_p=41 ps

PRF=15 Gpulses/s

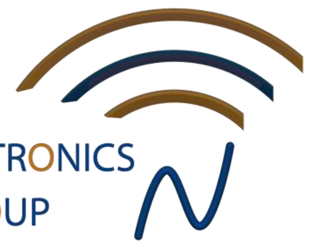
P_{out}=7 dBm

P_{dc}=29 mW

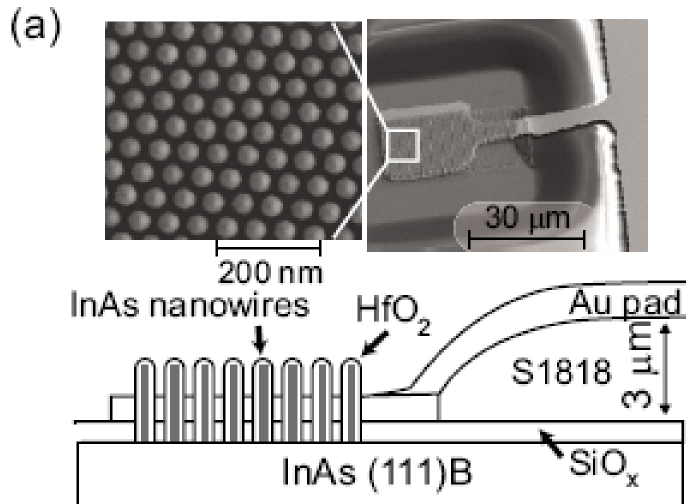
E_p=1.9 pJ/pulse

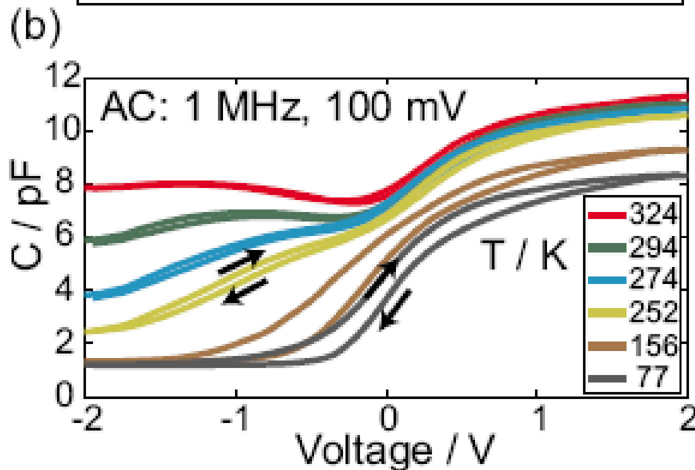
10-dBc bandwidth 20.5 GHz

Surfaces of InAs Nanowires

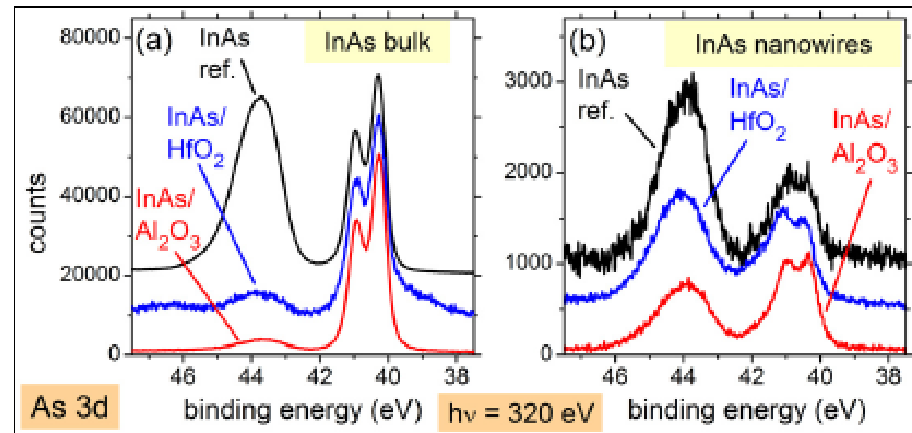


InAs/HfO2 nanowire capacitors





XPS on InAs nanowires



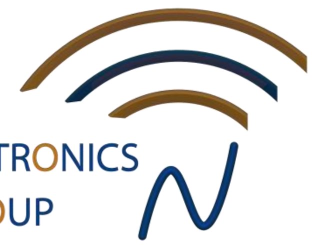
Nanowire capacitors behave like planar InAs capacitors

Temperature and frequency dependence

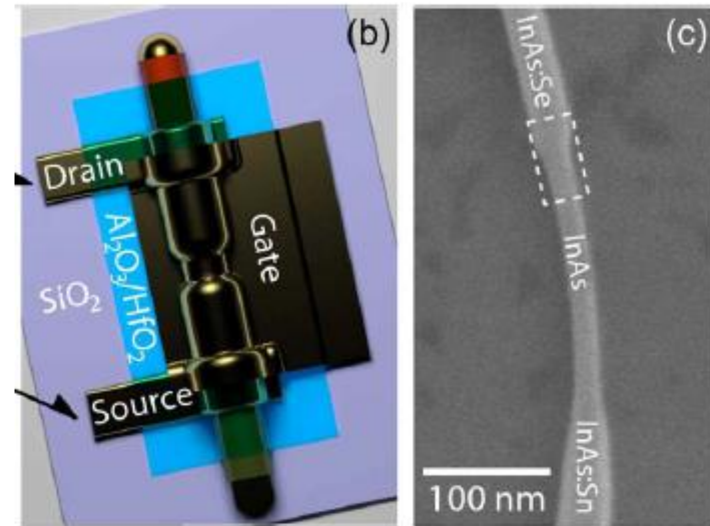
Holes may play a role due to narrow gap

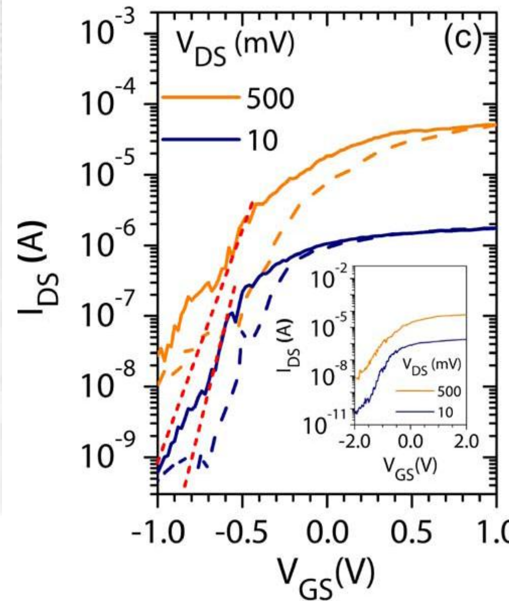
Less effective oxide reduction

Nanowire Transistors



Transport in thin (15 nm) InAs NWs



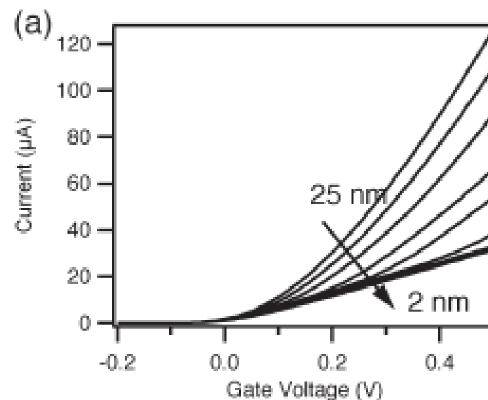


- Lateral transistors
- 100 nm L_g
- Doping reduces access resistance
- R_{on}=260 Ωµm
- Max g_m 1.2 S/mm
- I_d=34 MA/cm^2 or 1.2 A/mm
- Best g_m/g_o=50

Simulated data (tight binding)

I_{on} ~ 80 µA

$I_{on,exp}$ =30 µA



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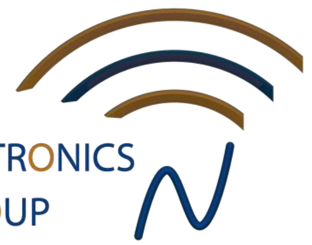
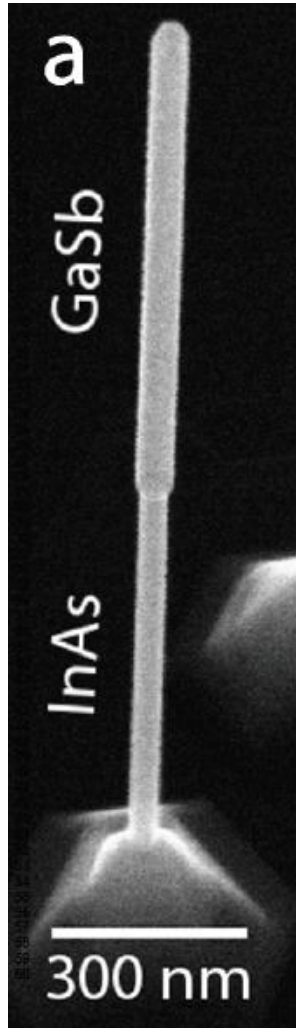
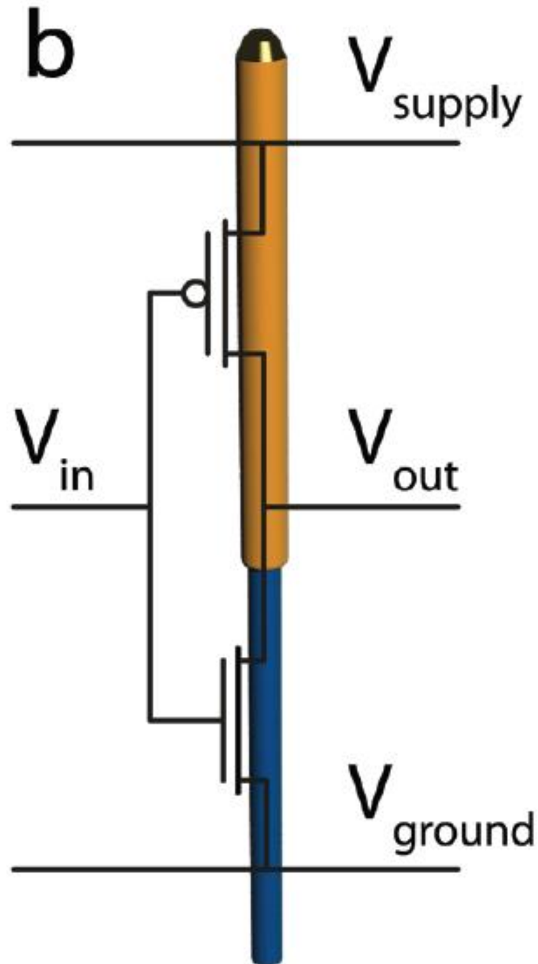
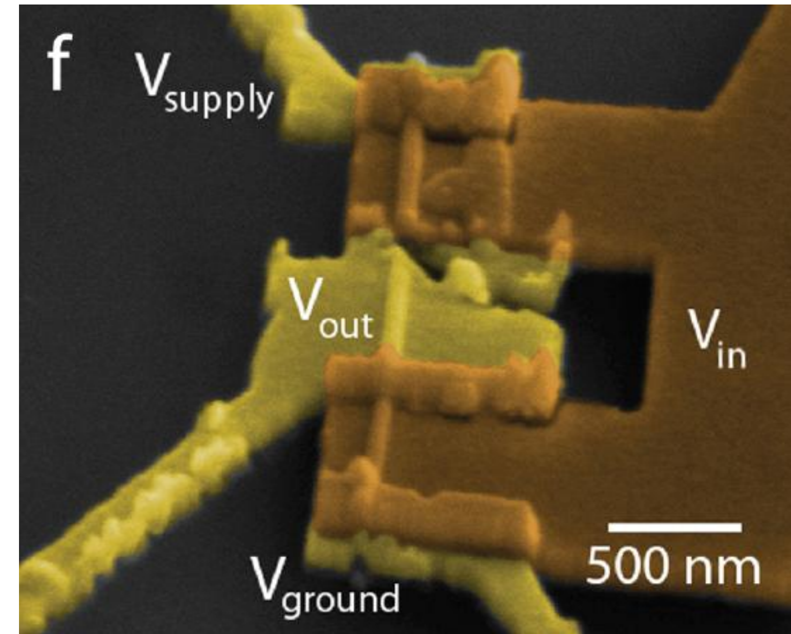
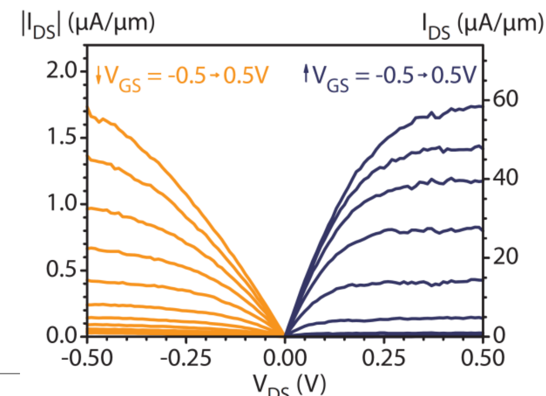
Nanowire Inverters



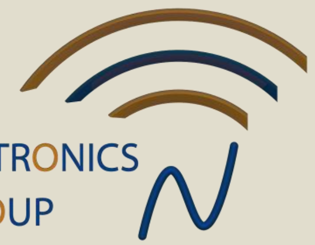


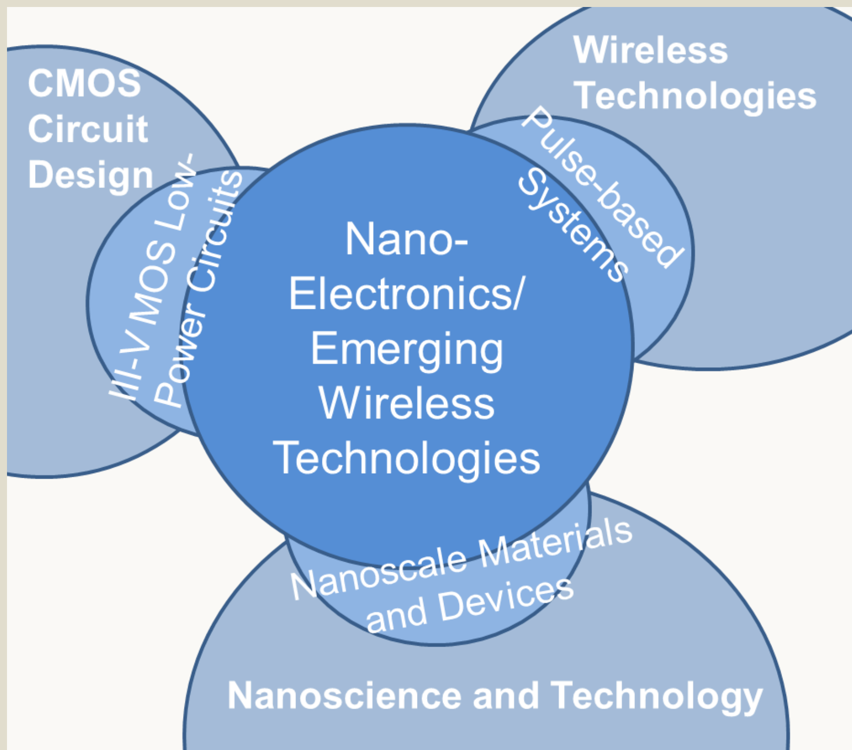






The Nanoelectronics Group





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