Low Power Design
- Jointly towards 28FD-SOI

JOACHIM RODRIGUES, LUND UNIVERSITY

Overview

All PhD projects will be presented at the poster session tomorrow

- 65 nm
  - Custom Full-adder for 300 mV- Cristoph Müller
  - Energy efficient decoders- Reza Meraji
  - ULV DC-DC Converter – Babak Mohamadi
  - Digital baseband for a wake-up receiver- Nafiseh Mazloum
  - Master Thesis projects
- 28 FD-SOI
  - 16 kB low power memory– Babak Mohamadi
  - Synthesizable latch based memory- Oskar Andersson

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300mV Full-adder with fast Carry propagation

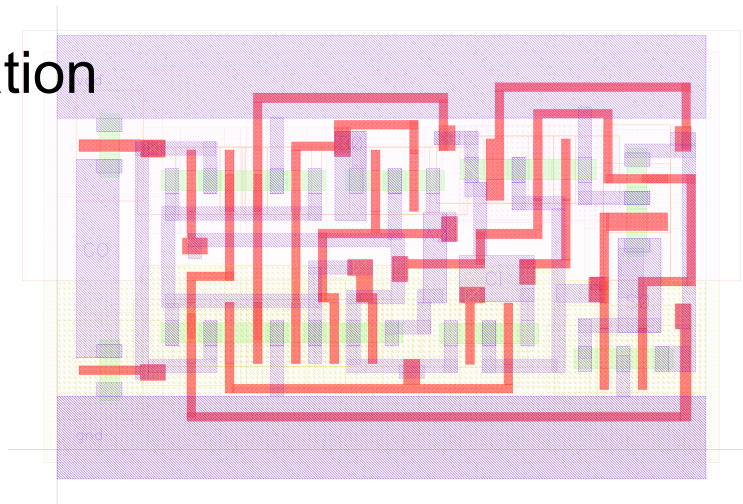
CHRISTOPH MÜLLER

Custom Full Adder Cell for Sub-V_t

Goal: FA for Ripple Carry Adder at 300 mV

- Simplest Adder design, no carry propagation circuitry leaking
- Throughput limited by carry propagation

➔ Optimized for a fast Ci to Co path



Survey over 36 Architectures

- Optimization, characterization and seamless PDK integration of winning design
- 23 T, Mixed Pass-Transistor/CMOS implementation, dual-V_t balancing

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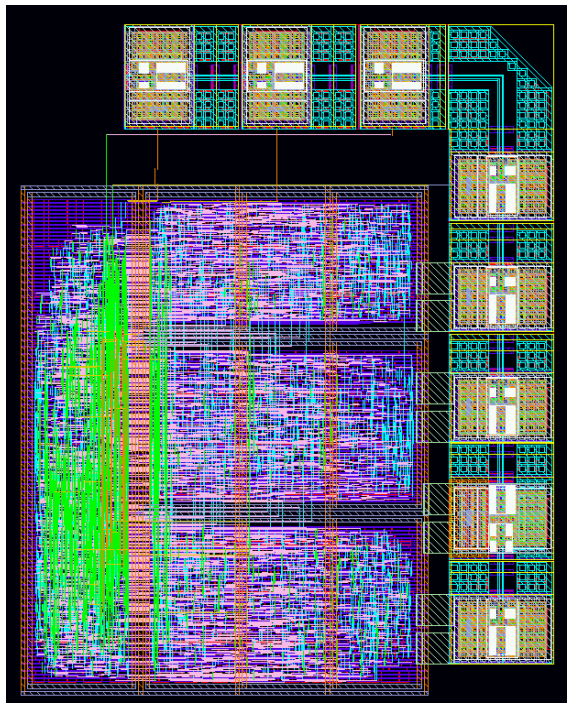
Test Designs

Testbed

- Three 24x24 ripple carry array multipliers, realized by
  - custom FAs
  - PDK FAs (different constraints)
- Separate power domains for measurement
- BIST to reduce pad count



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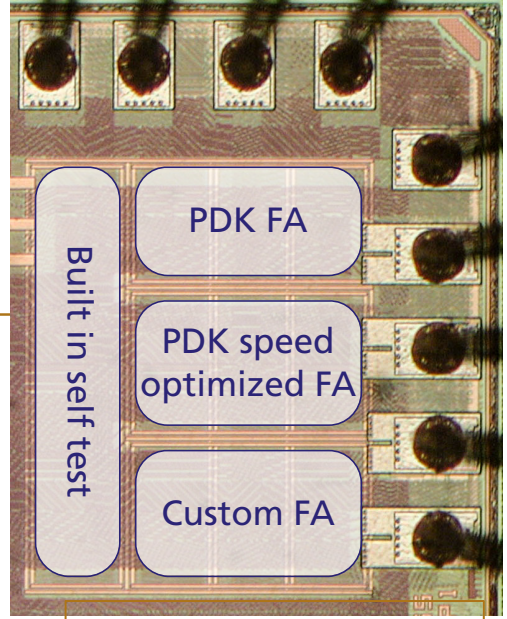
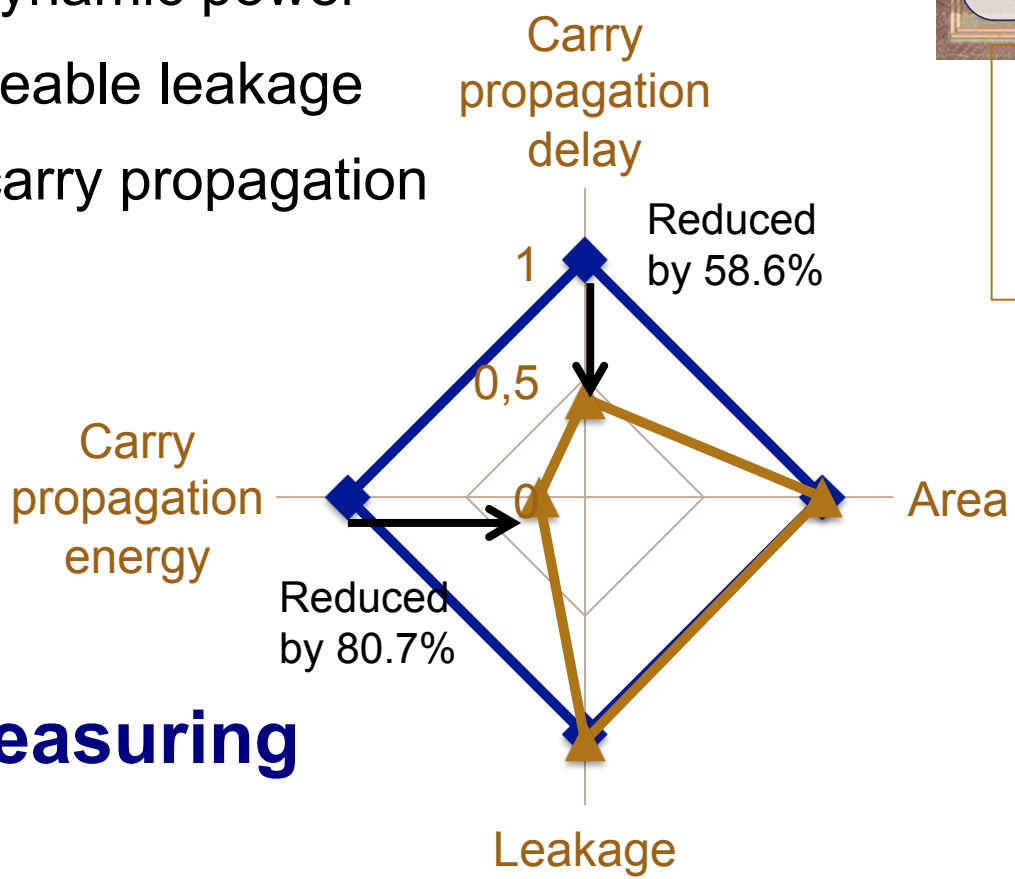
Expected Results

- Simulation results in comparison to FA from PDK:
  - Lower dynamic power
  - Compareable leakage
  - Faster carry propagation





Status: Measuring

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Energy Efficient Decoders for an Ultra Low Power Radio

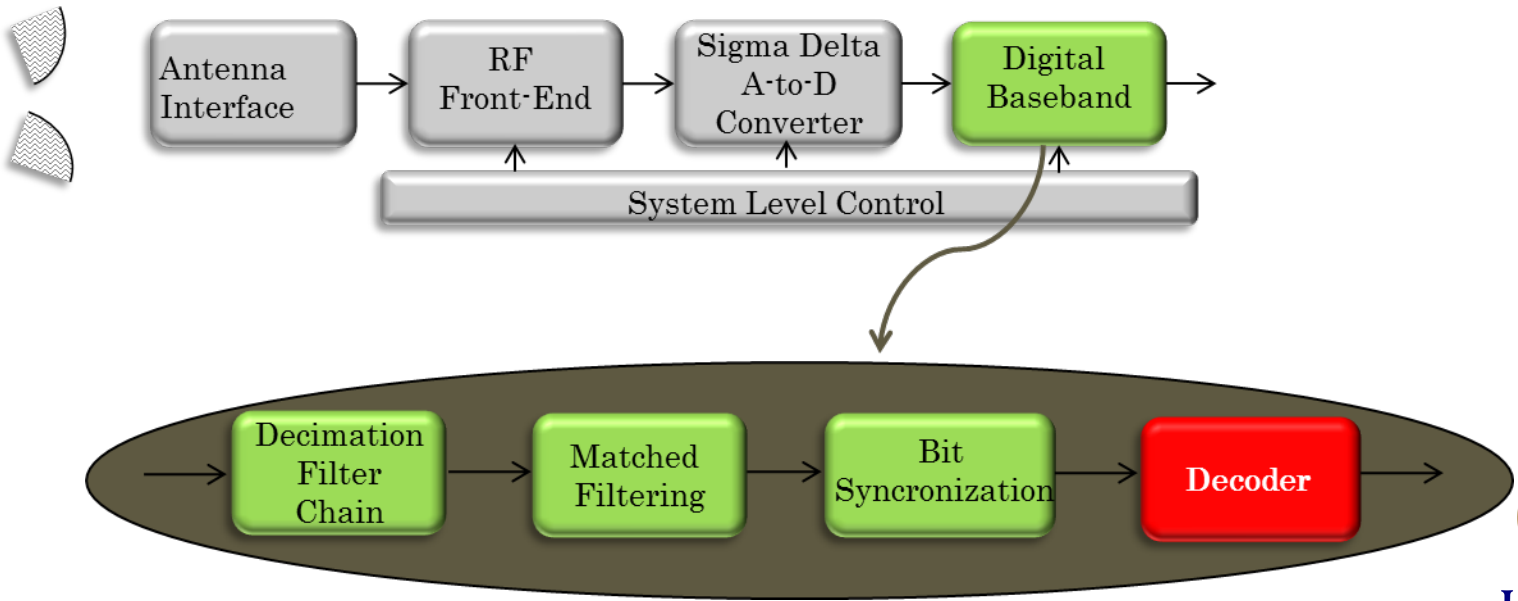
REZA MERAJI

Graduation is planned for October 17th

An Ultra Low Power Receiver Chain

Project Goal: A complete low power receiver chain from antenna to decoder

- 1mW active, 1uW standby, 1mm^2 in 65nm
- 125 kbit/s or above for coded transmission



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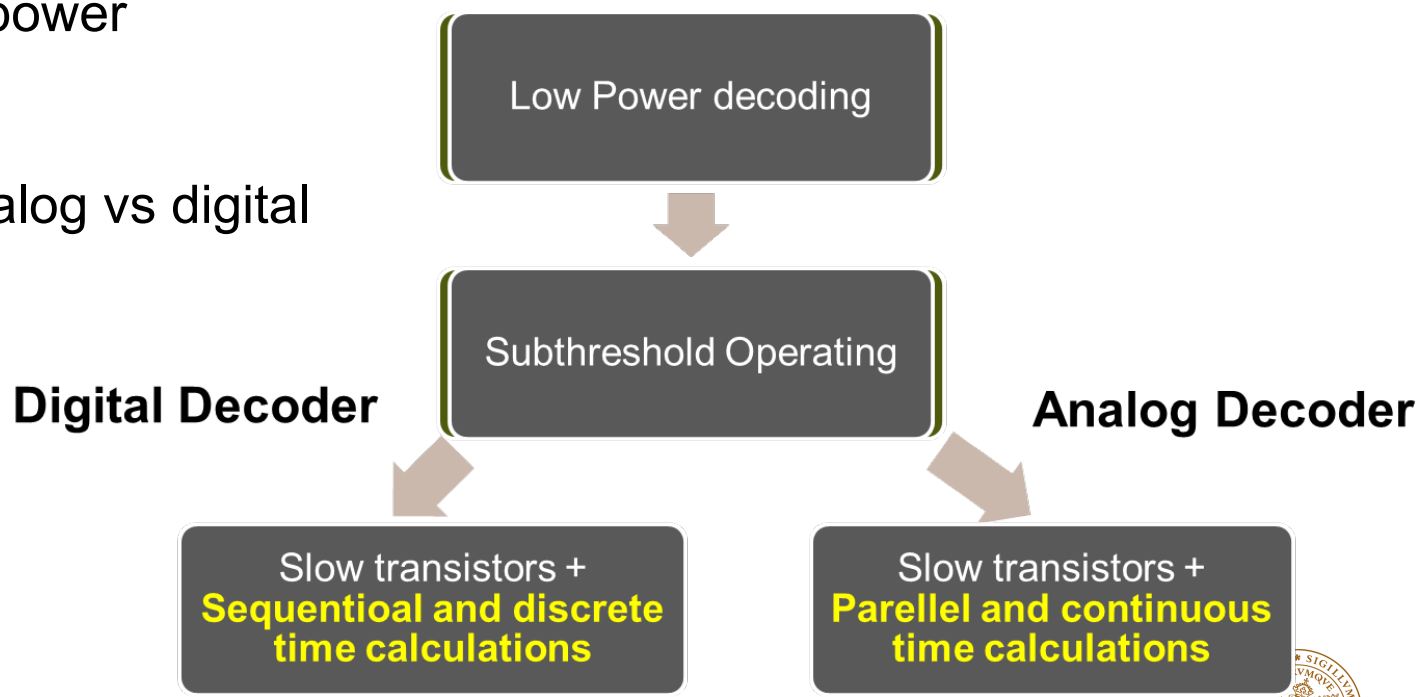
Hardware Implementation Approaches

Goal:

- Below 30 uW power consumption

- Comparing analog vs digital



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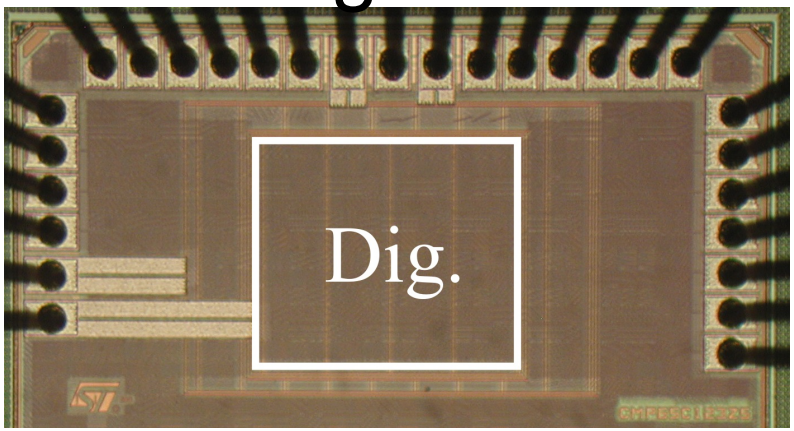
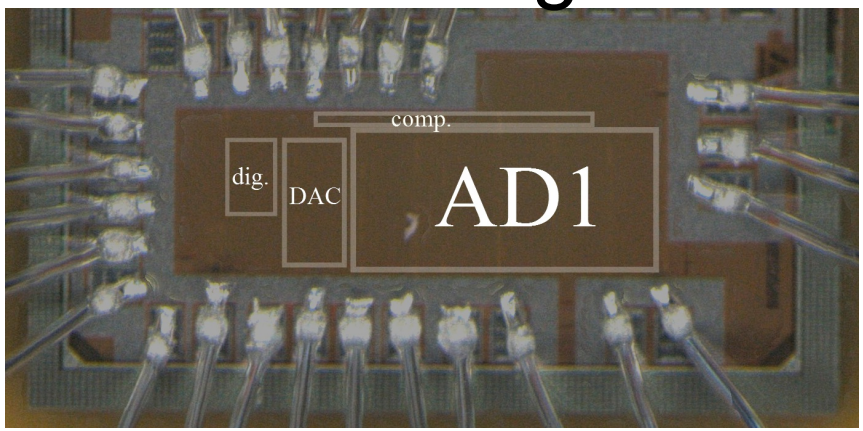
Fabricated ICs

Digital



Analog



- **Analog Decoder has superior energy efficiency at higher throughputs,**
  42 % more efficient @ 2 Mb/s.
  min V_{DD} = 0.8 V, 21 uW @ 2 Mb/s

Similar Area : 0.1mm^2

- **Digital decoder shows better energy efficiency at low V_{DD} / throughputs**
  33 % better @ 125 kb/s
  min V_{DD} = 0.32 V, 2 uW @ 125 kb/s

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Single Clock High efficiency ULV DC-DC Converter with Automatic Power Controller

BABAK MOHAMMADI

High efficiency Charge-Pump

Goal

- Charge-Pump operational in Ultra low voltages
- Low area cost, fast, high gain
- Low Power

Our idea

Concept

- Improving switching quality by control logic
- Body biasing dynamically adjusted for increased efficiency
- Employing a voltage sensor to shutdown the switching activity

Conventional

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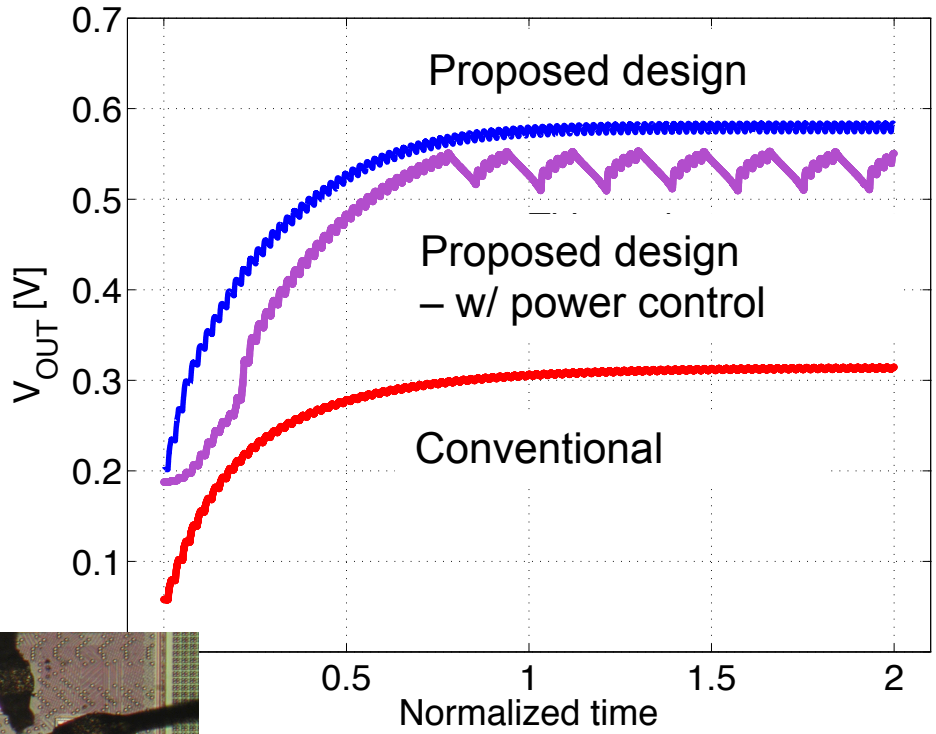
Results

W.r.t to conventional Charge-Pump with same area cost:

- More than 10x speed up
- More than 85% higher gain in ULV

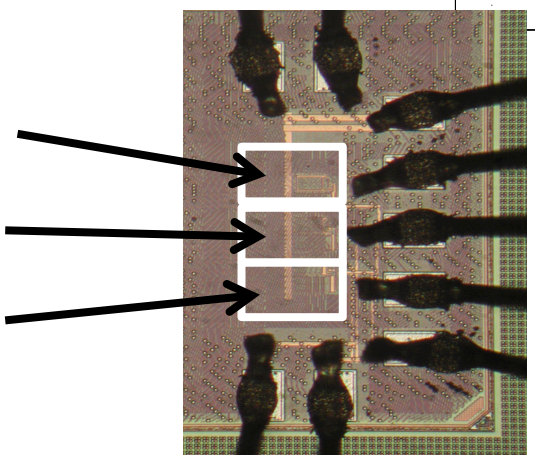
Functionality in 300mV verified by initial measurements



Conventional

Proposed design

Proposed design
- w/ power control



VDDL=250mV
Clk=500KHz
Load=2pF, 10MΩ

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A 1µW wake-up receiver digital base-band with large address-space scalability

NAFISEH S. MAZLOUM

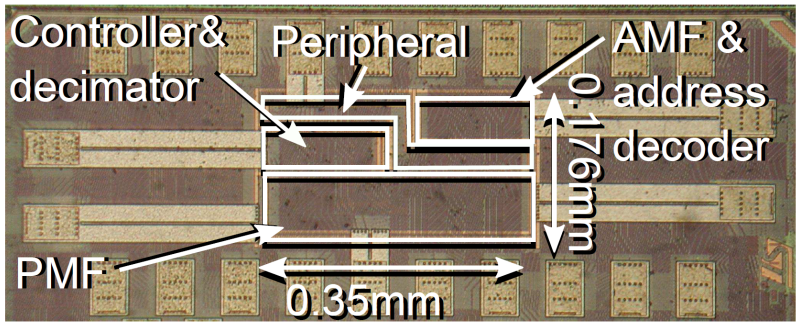
A Sub-V_t digital base-band

Goal:

An ultra-low power digital base-band for a certain wake-up beacon structure.

Measurements:

1µW operating with 1MHz at V_{DD} = 0.37V



V_{DDmin} = 0.27V (at 5kHz)

The properties of the architecture enable scalability for massive networks with large address-spaces.

Nafiseh will give a more detailed presentation after my talk

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Master Thesis

Sub-V_t Variation Aware Clock Network

Yuqi Liu, Babak Mohammadi, Oskar Andersson

- Reduced relability due to increased PVT variations, thus larger variations in skew and slew rate
- Quality of clock network improved by full-custom sub-V_t clock buffers

Expected Results

- 6x improvement in skew
- Lower area cost
- Less dynamic energy in clock tree

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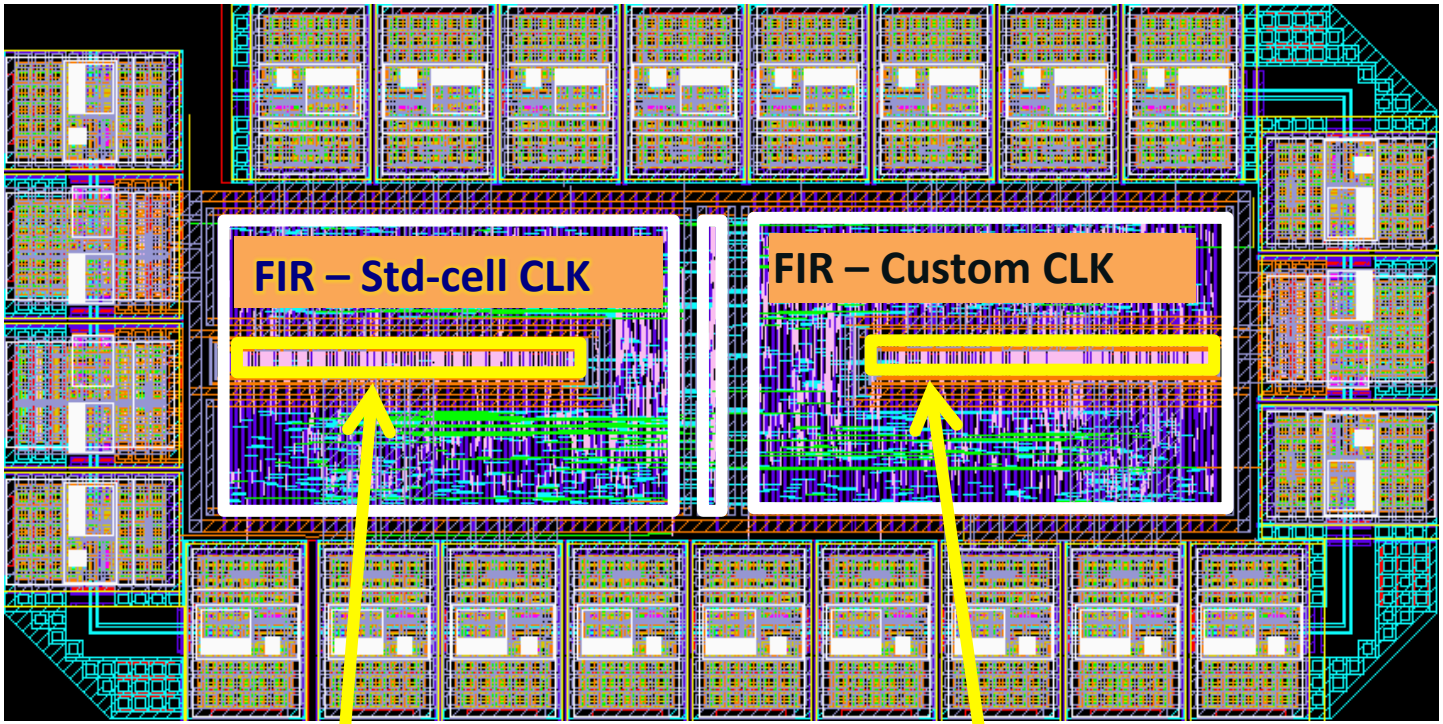
Master Thesis

Sub-V_t Variation Aware Clock Network



Standard-cell clock buffers

Custom Clock buffers

Clock buffers in separate power domains

Status: Measuring queue

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Low Energy Data Compression for Brain Implant

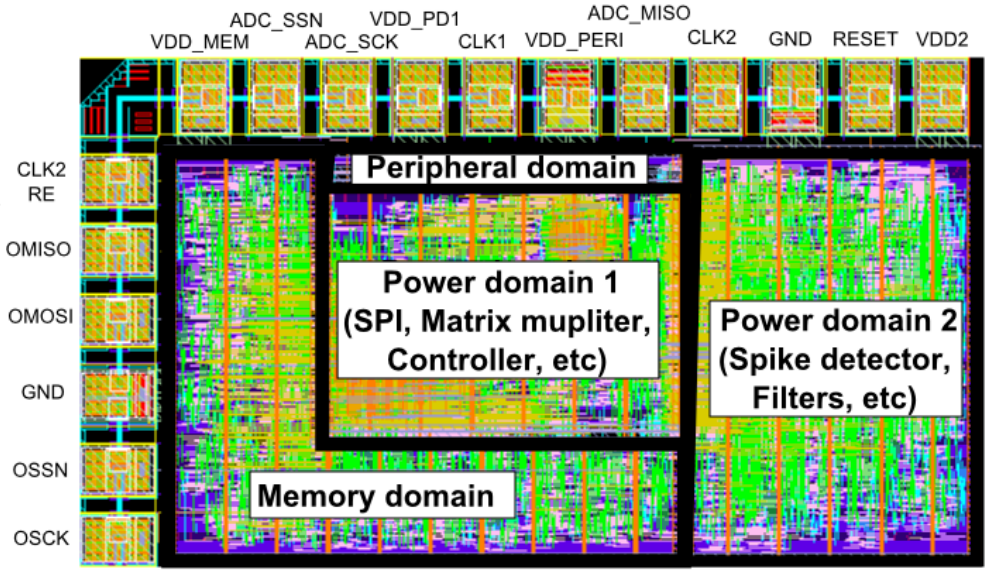
Master Thesis

- Compression ratio

  Up to 125X @ 100 spikes/s
- Architectural Optimizations

  Area optimized
- Energy savings

  30X from sub-V_t operation



Longyang Lin is a Phd student in Massimo Alioto group in Singapore now

Status: Measuring queue

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Memories

BABAK MOHAMMADI

OSKAR ANDERSSON

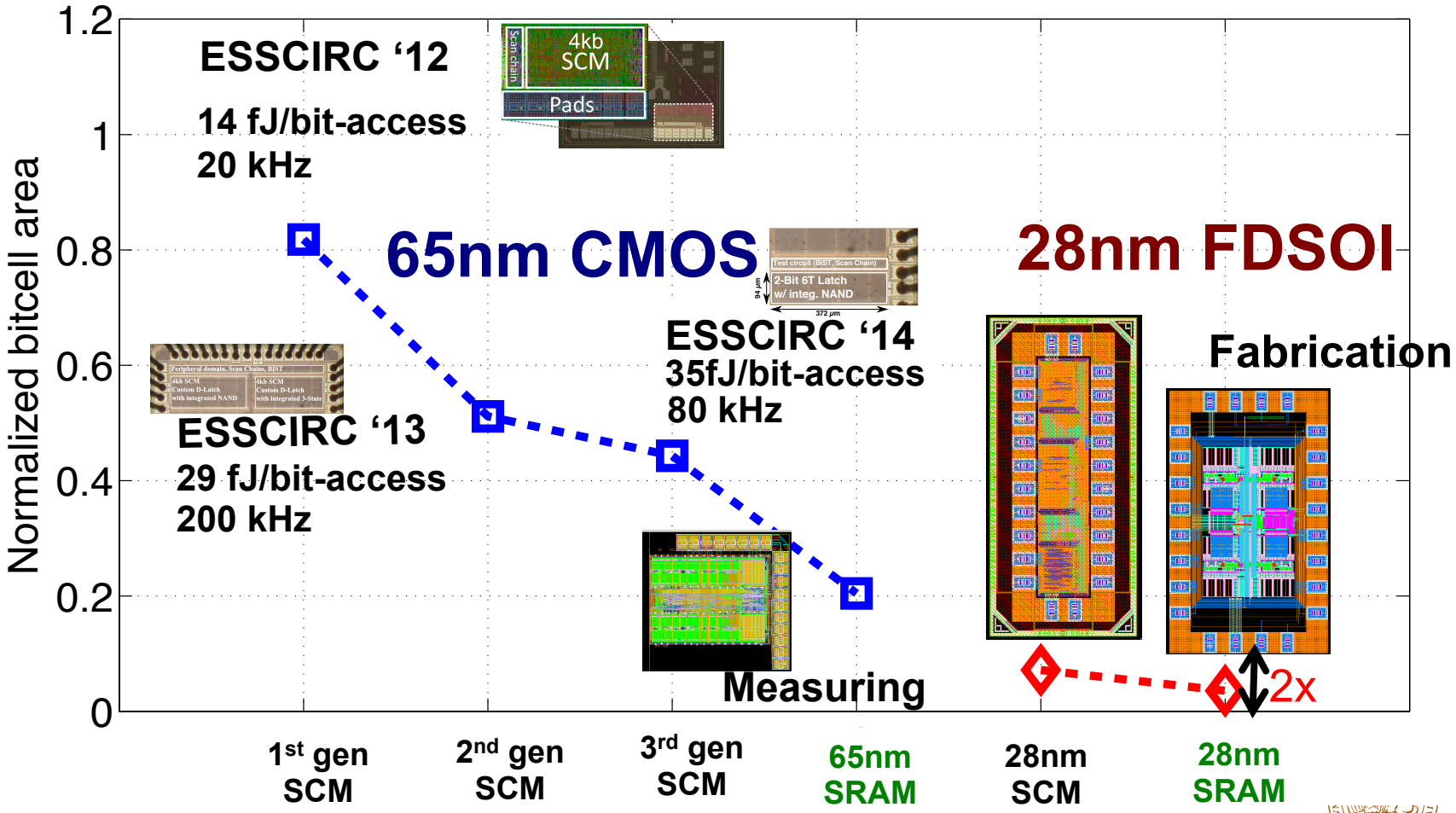
PASCAL MEINERZHAGEN (EPFL, NOW AT INTEL LABS)

ANDREAS BURG (EPFL)

LORENZO CIAMPOLINI, ST CROLLES, FRANCE

JOSEPH NGUYEN, ST CROLLES, FRANCE

OUR ULV memories



– Area normalized to 65nm standard cell

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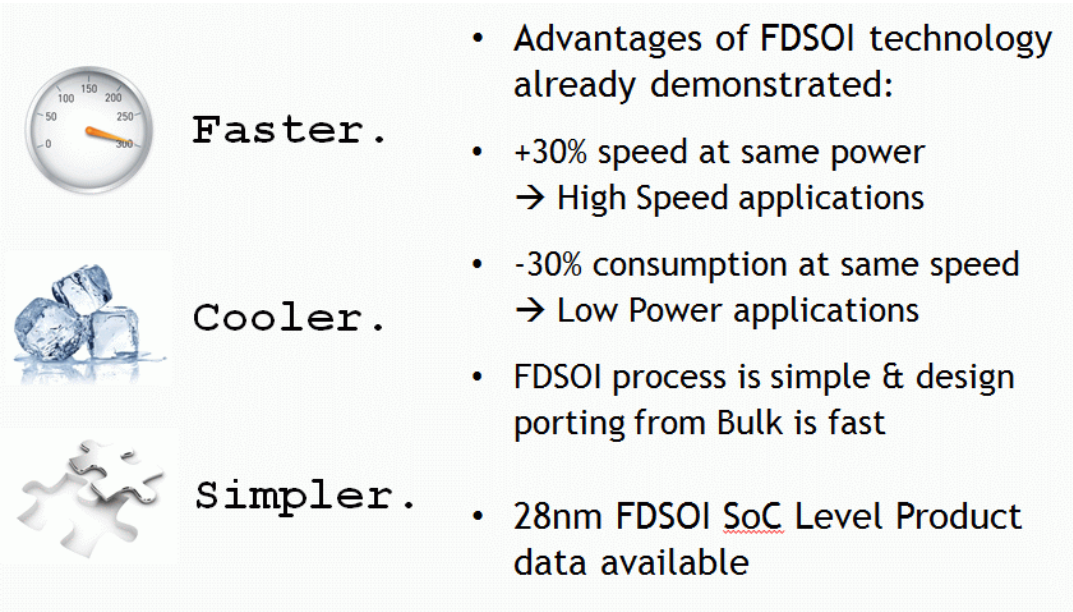
Low Power Memory in 28 nm FDSOI

BABAK MOHAMMADI, EIT

LORENZO CIAMPOLINI AND JOSEPH NGUYEN, ST CROLLES, FRANCE

Lund/ST Collaboration Framework

- STMicroelectronics grants fabrication and supports the design on the newly developed FD28SOI technology



- Development done by Babak Mohammadi at Lund University

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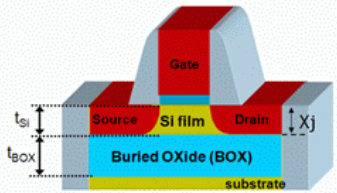
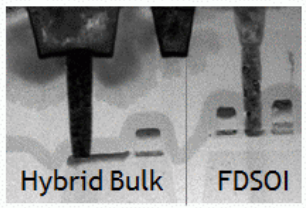
Lund/ST Collaboration Framework

- 2 months internship in STMicroelectronics Crolles (France), the fab where the FD28SOI process has been developed

- Device architecture gate-first HKMG
- *Tsi 7nm, thin BOX 25nm*



- BOX opened with NOSOI mask for co-integration with Bulk devices and well ties



- *Thin Tsi* → excellent electrostatic control
- *Undoped channel* → low variability
- *Thin BOX* → efficient and extended body biasing
  → well type used to define Vt

- 15% less process steps in 28nm FDSOI vs LP

- Possible future joint developments currently being discussed

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Memory specifications and Features

- 16 kB Memory Macro operating at 20 MHz at 300 mV with a single power supply
- Custom Ultra Low-Leakage bit-cell (PIPR) with modified Bit-Line write
- Low-power Boost Unit based on custom charge-pump (PIPR) dramatically improves write & read operations
- Novel Hybrid Decoding method (PIPR) allows to fully exploit the Boost Unit
- New read operation mechanism (PIPR) allows ULV operation
- Internal scan-chain and BIST will be used to test the Macro on silicon

PIPR= Planned IPR

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Custom ULL Bit-cell

- Single-well architecture (stronger PMOS available)
- DRC-clean design using **no pushed DRC** rules;
- **Negligible area** overhead compared to industrial 8T bitcell (ST), area might improve with increased fab support.
- Bit-cell Spice characterization ongoing at ST
- Highly optimized for low leakage, lower leakage compared to existing 8T bit-cell
- Faster than existing 8T bit-cell
- Getting Closer to industrial design environment

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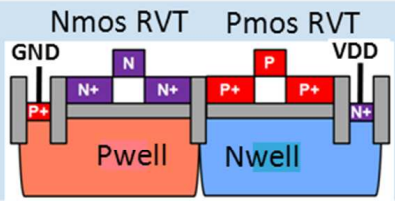
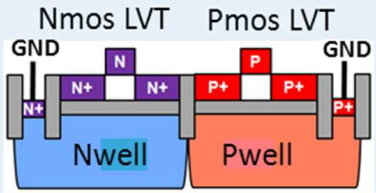
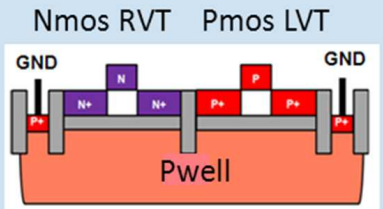
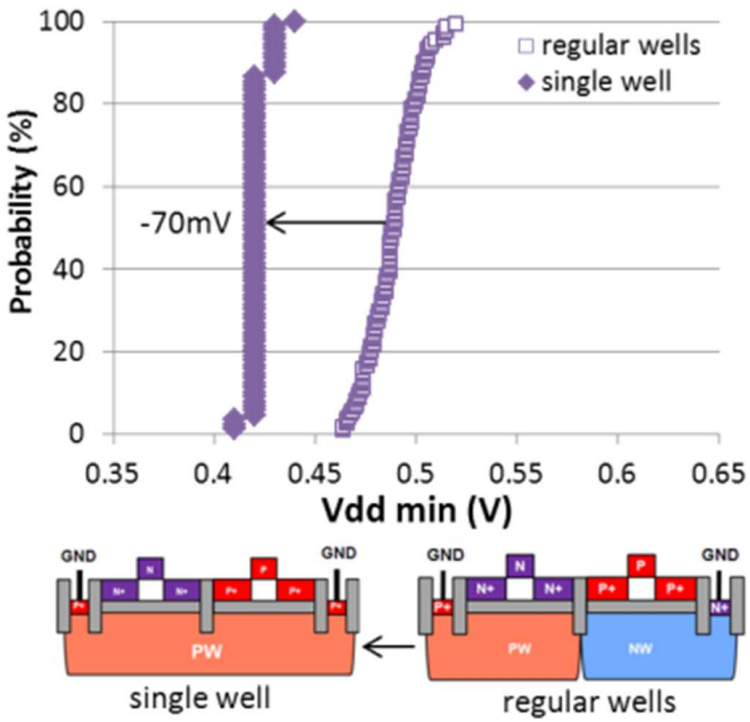
Single P-WELL Macros

- Dynamic bias bitcell centering with single-well architecture

SRAM architecture	Features
	Regular architecture Bulk design portability Full RBB → ultra low leakage FBB VDD/2
	Flip-well architecture Full FBB → High Speed cell
	Single well architecture High SNM, Low Voltage Full RBB/FBB for bitcell recentering



Source for images: FDSOI Process/Design full solutions for Ultra Low Leakage, High Speed and Low Voltage SRAMs , R.Ranica (STMicroelectronics, Crolles, France) et al, VLSI 2013

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Current Status

- Design sent for fabrication, wafers expected beg 2015

Layout view of the chip sent for fabrication Total Area 730x1100 μm^2 = 0.803 mm^2

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Synthesizable latched based memory in 28nm FDSOI

OSKAR ANDERSSON

SCM in 28FDSOI with Full-Custom 4-Bit Latches

Goal:

- Provide an alternative to SRAM for medium throughput system with energy awareness.
- Comparison with standard cell:
  - Decreased area
  - Reduced leakage
- Comparison with SRAM:
  - Reduced energy dissipation
  - Area penalty (?) & Delay

Status: Fabrication confirmed for October run

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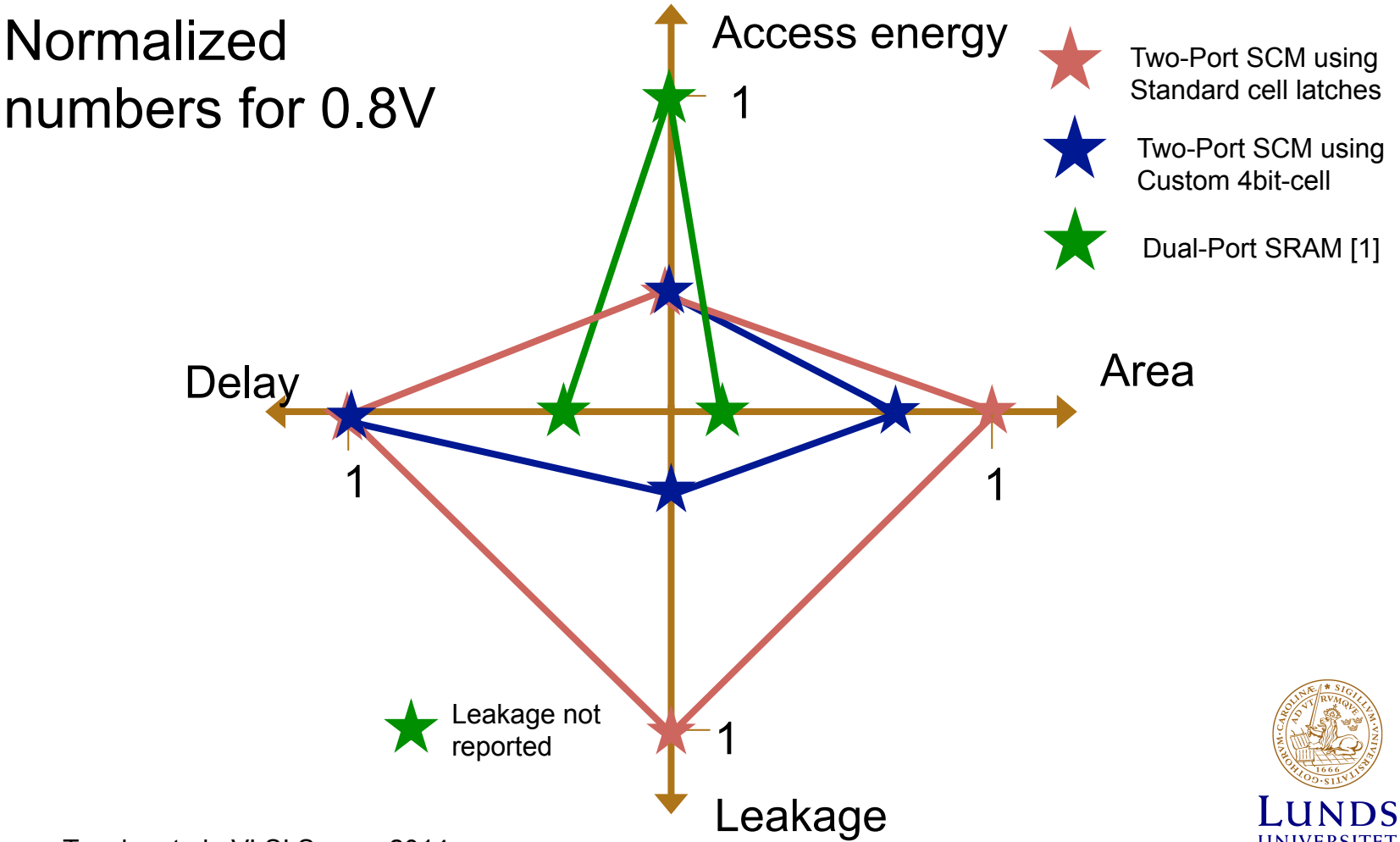
SCM in 28FDSOI with Full-Custom 4-Bit Latches



[1] **Renesas**:Tanaka et al., VLSI Symp., 2014

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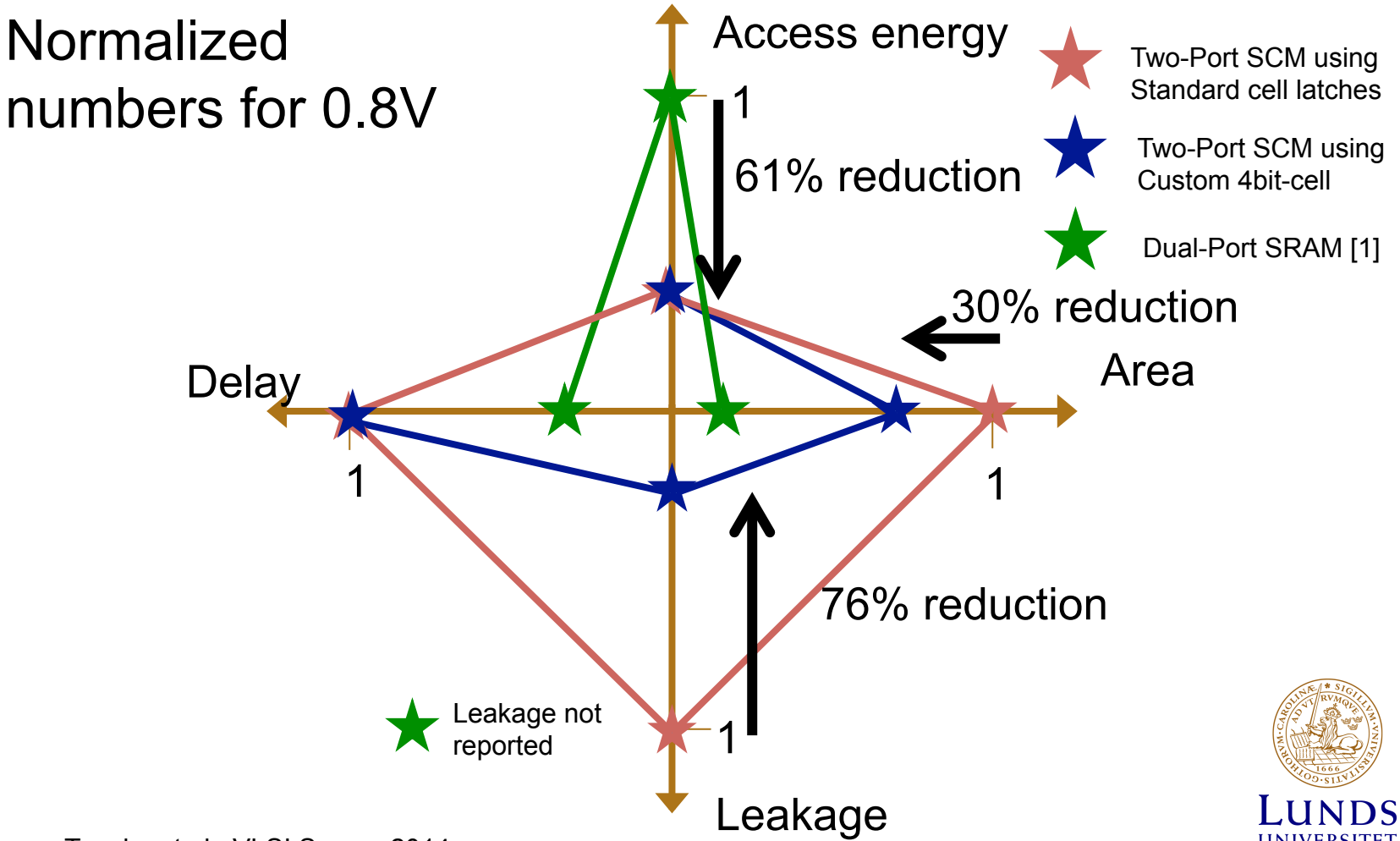
SCM in 28FDSOI with Full-Custom 4-Bit Latches



[1] **Renesas**:Tanaka et al., VLSI Symp., 2014

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A 1µW wake-up receiver digital base-band with large address-space scalability

NAFISEH S. MAZLOUM

Questions?