

A Noise Cancelling Resistive Feedback Receiver Front-End

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Outline

- Introduction
- Implementation
- Results
- Conclusions

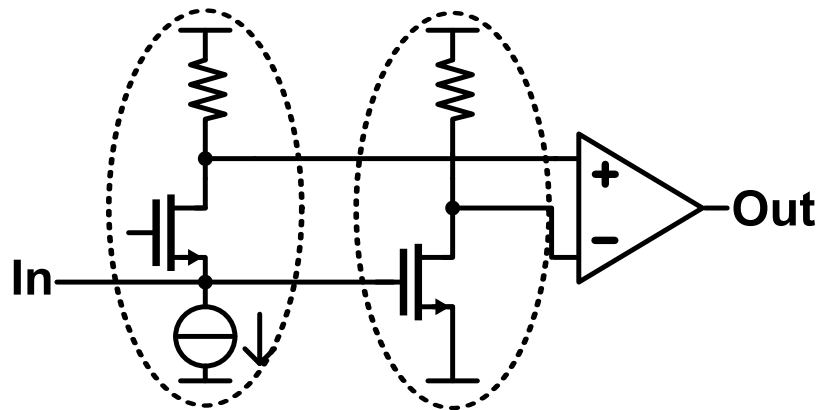
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Motivation

- Past years, many techniques using the bi-directional frequency translational properties of passive mixer have been demonstrated
- Low noise critical for cellular applications
- Noise cancellation translational techniques

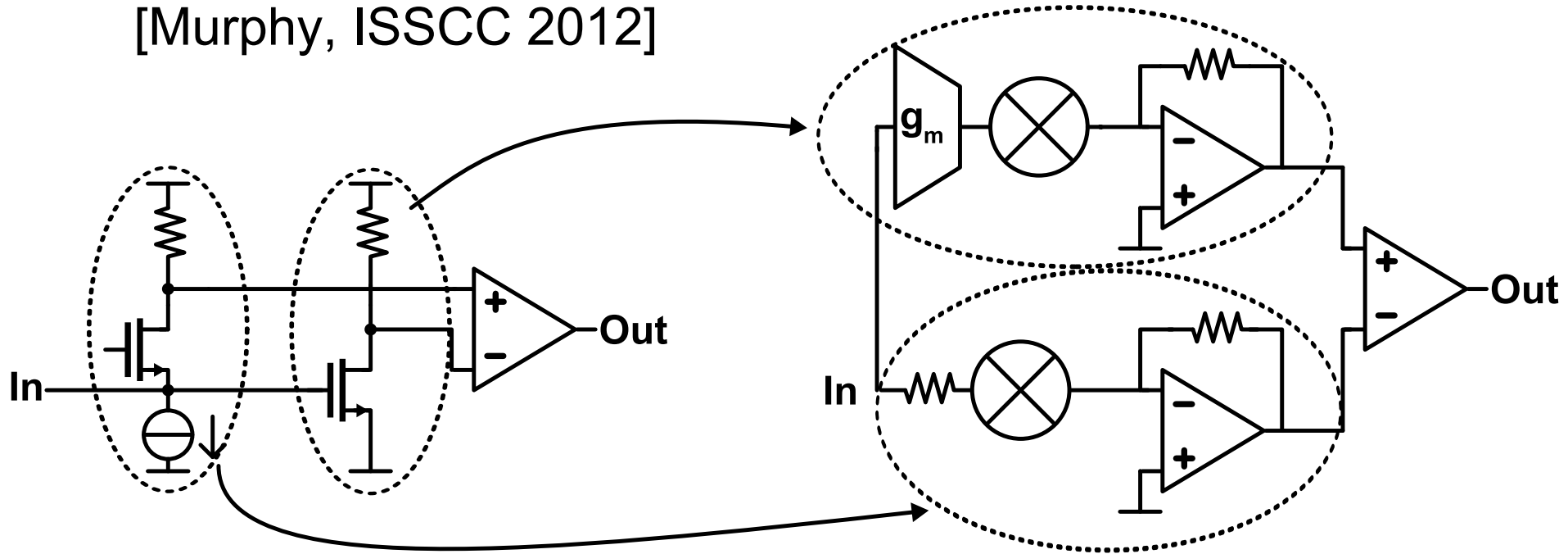
Previous art



- CG-CS Noise-Cancelling LNA

Previous art

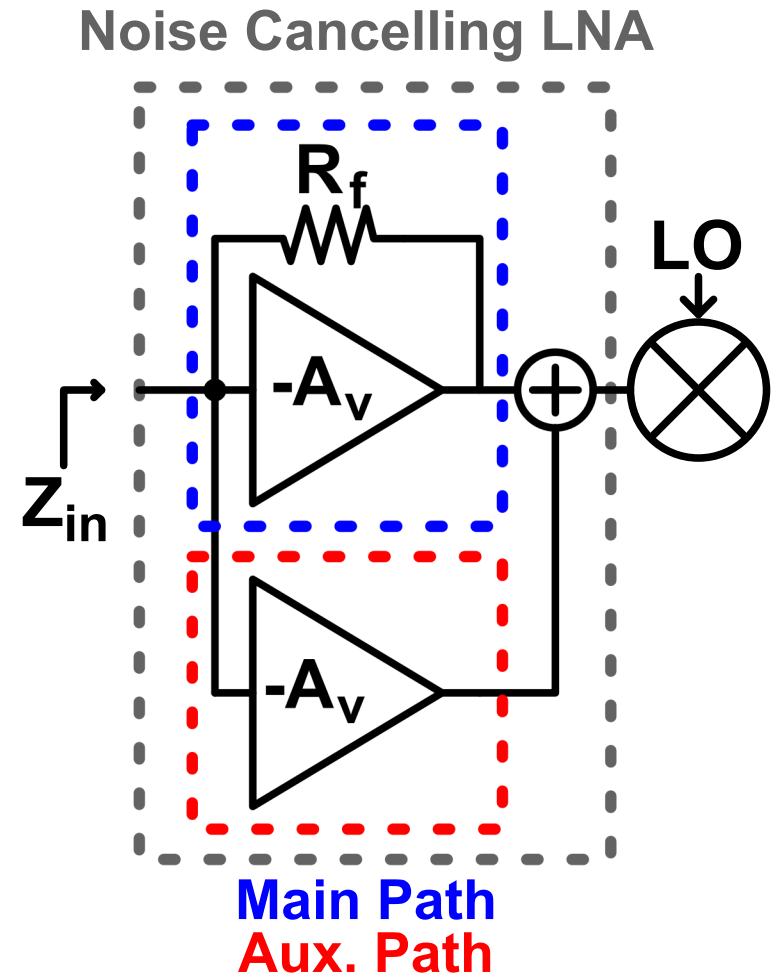
[Murphy, ISSCC 2012]



- CG-CS Noise-Cancelling technique used in Receiver Front-End

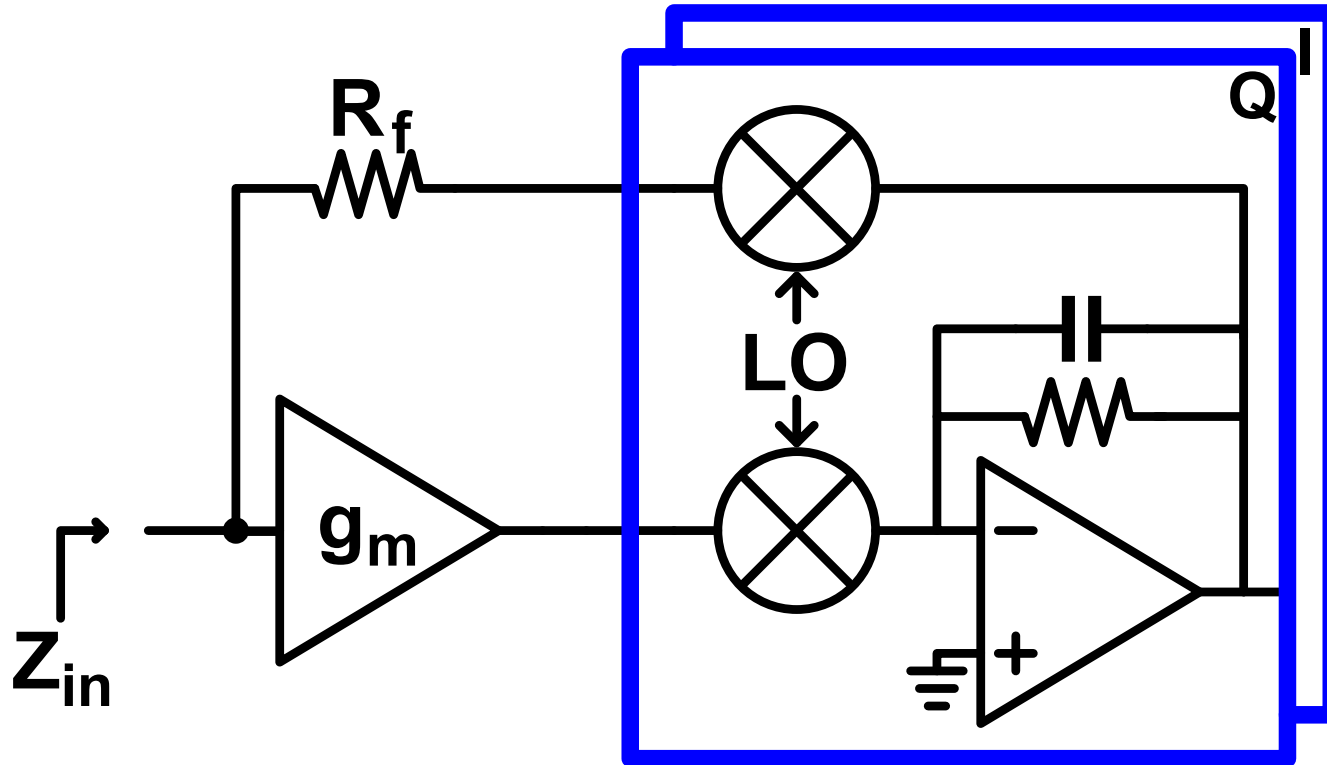
Noise cancelling feedback LNA

- Wideband input match
 - By **Main path**
- Noise cancellation
 - By **Aux. Path**
- All processing at RF
- More processing in BB



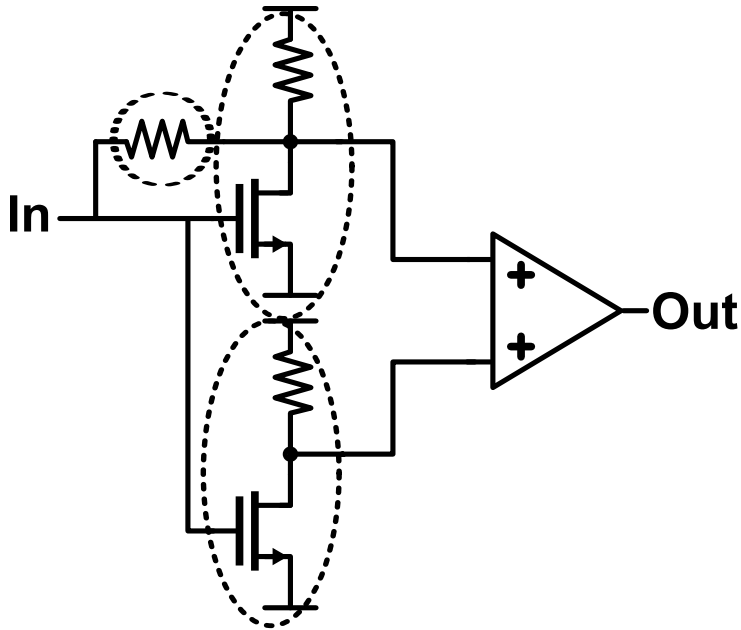
Shunt Fb Receiver Front-End

- No voltage gain at RF [He, ISSCC 2011]



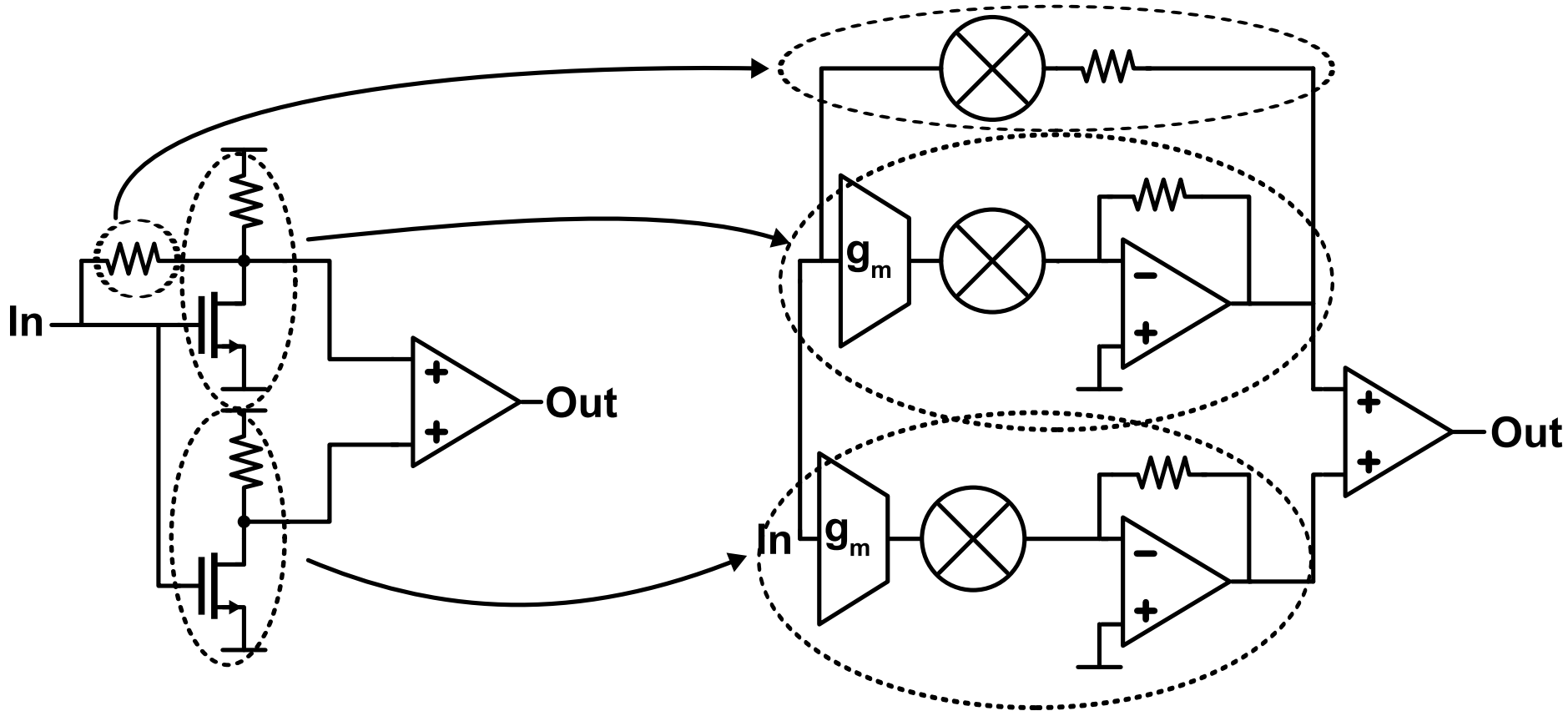
- Frequency selective input match at f_{LO}

Noise Cancelling Principle



- Amplifiers implemented with CS-stages

Noise Cancelling Principle



- Is Z_S not resistive, feedback phase can be tuned

Noise cancelling FB Front-End (I)

- Input match

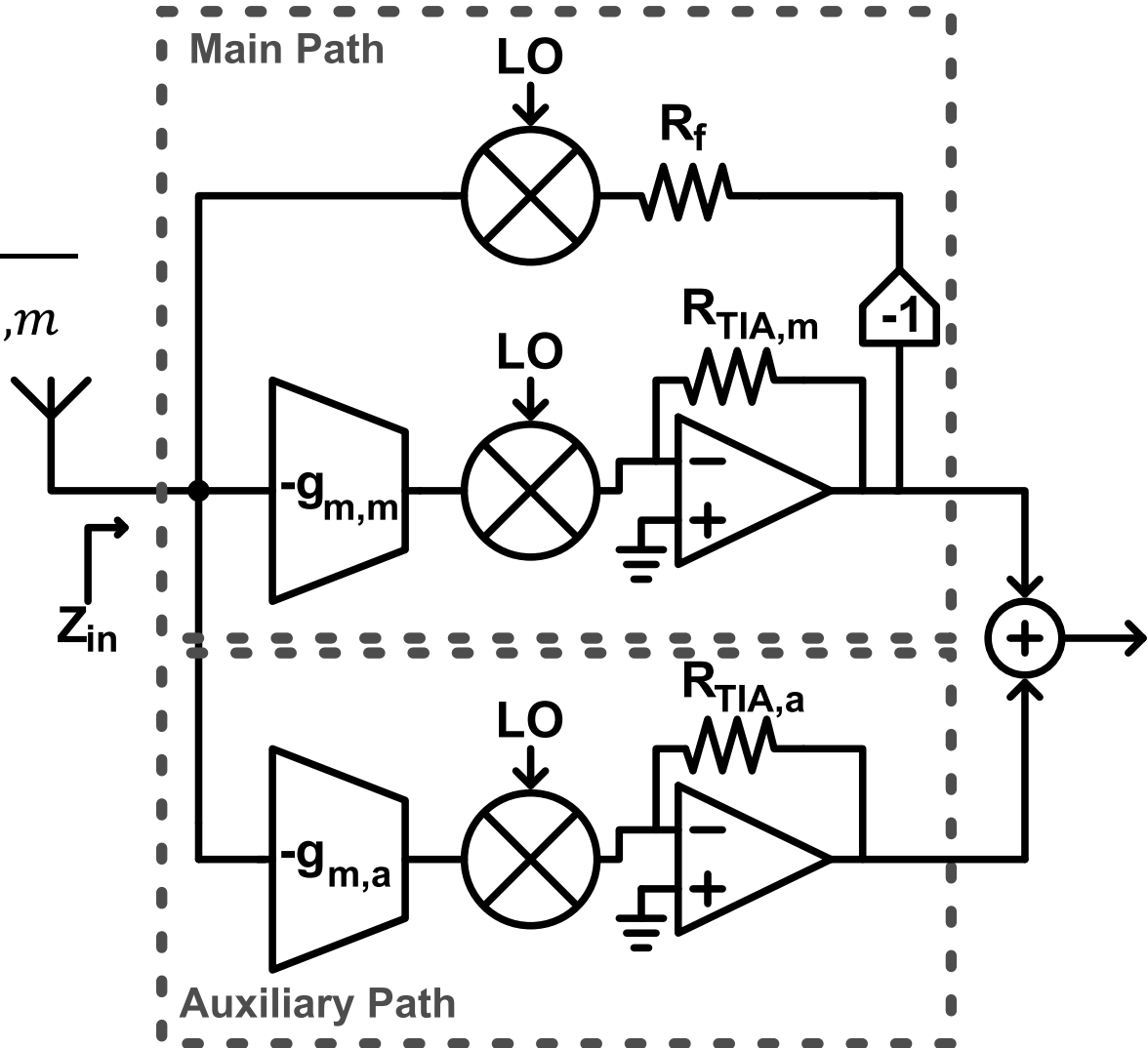
$$Z_{in} \approx \frac{R_f}{1 + g_{m,m}R_{TIA,m}}$$

- Gain main path

$$A_v \approx 1 - \frac{R_f}{R_s}$$

- Gain aux. path

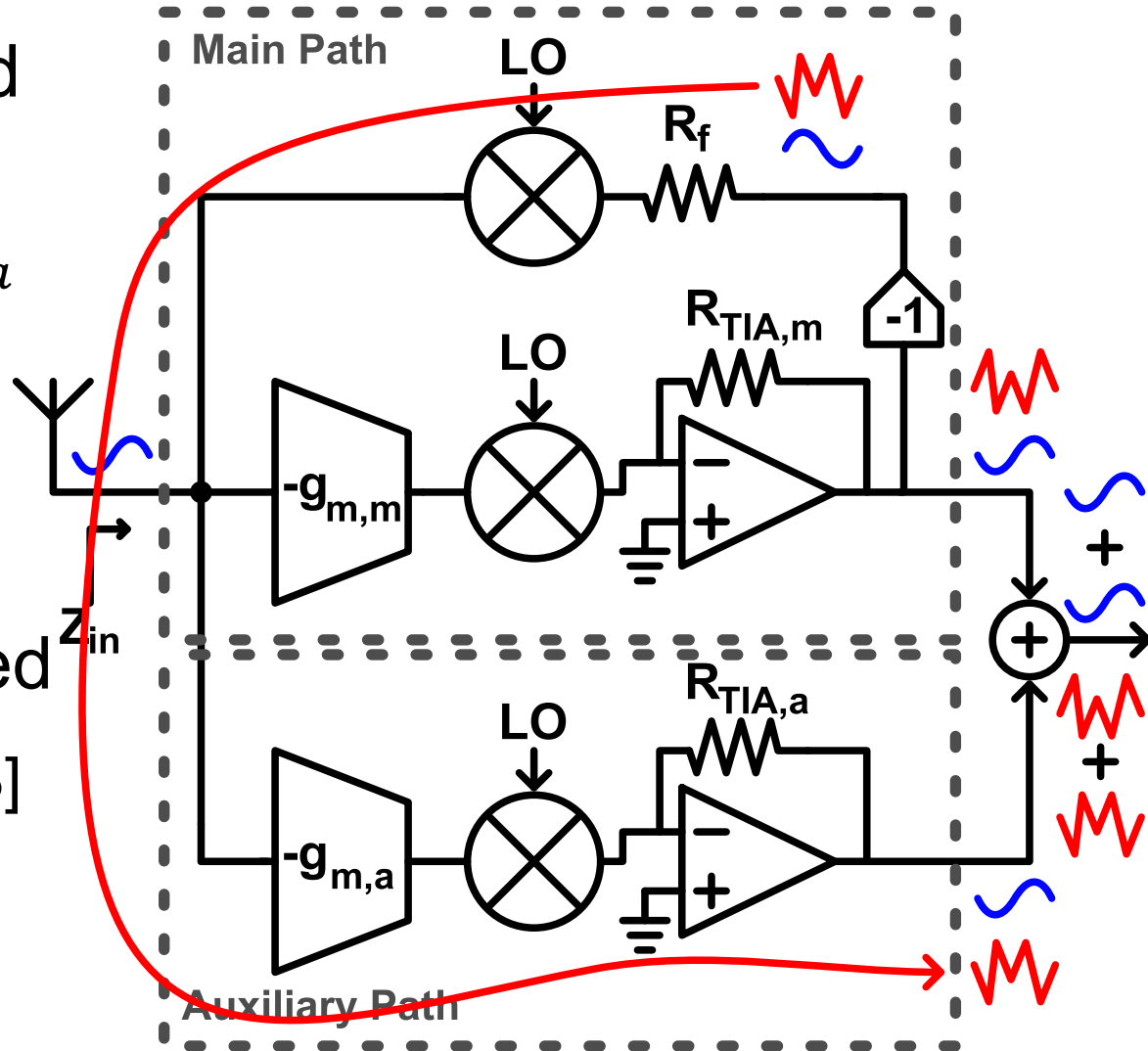
$$A_v \approx g_{m,a}R_{TIA,a}$$



Noise cancelling FB Front-End (II)

- Noise cancelled
 - If resistive Z_s
 - Aux phase tuned
- [Murphy, CICC 2013]

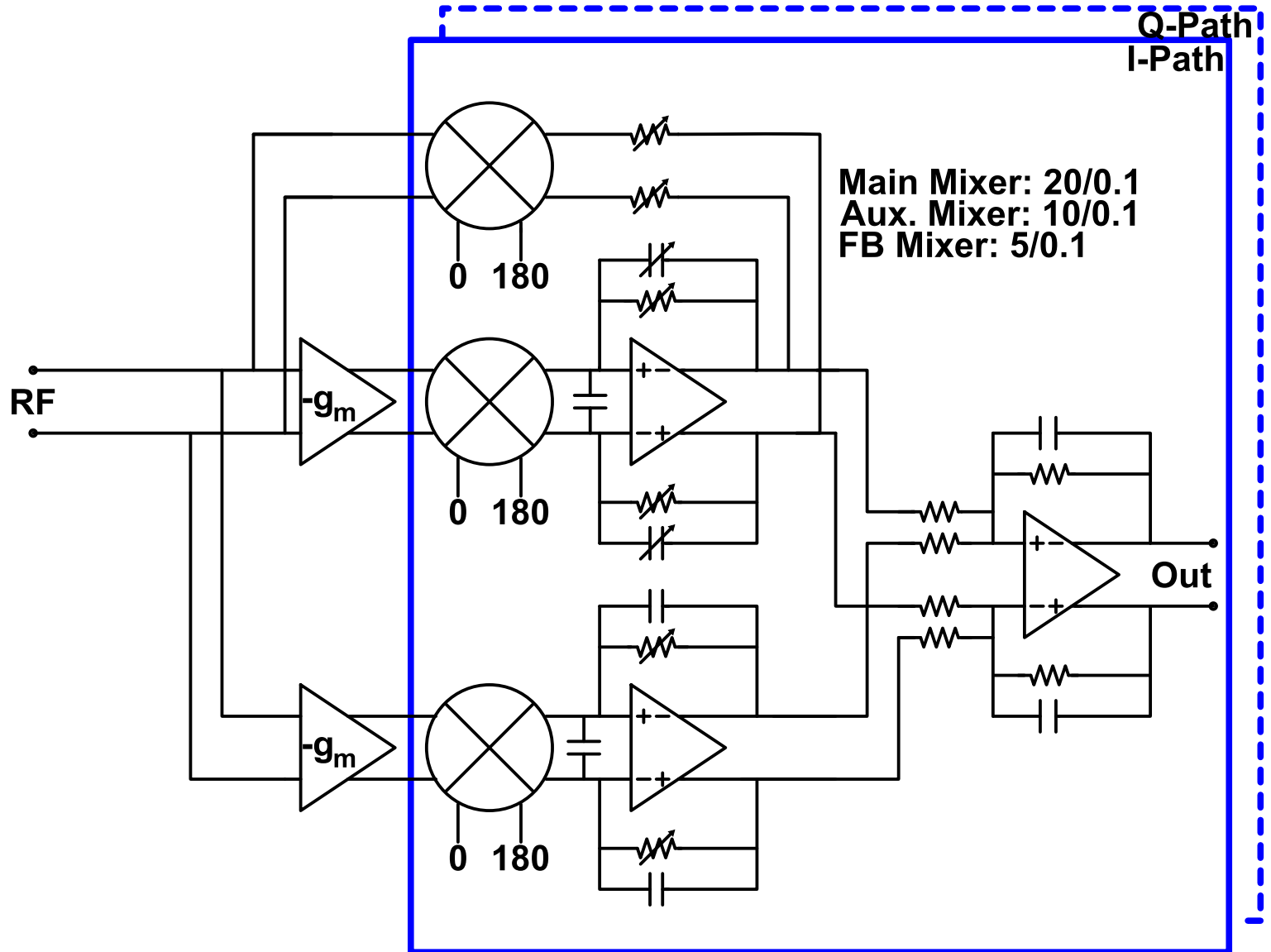
$$1 + \frac{R_f}{R_s} = g_{m,a} R_{TIA,a}$$



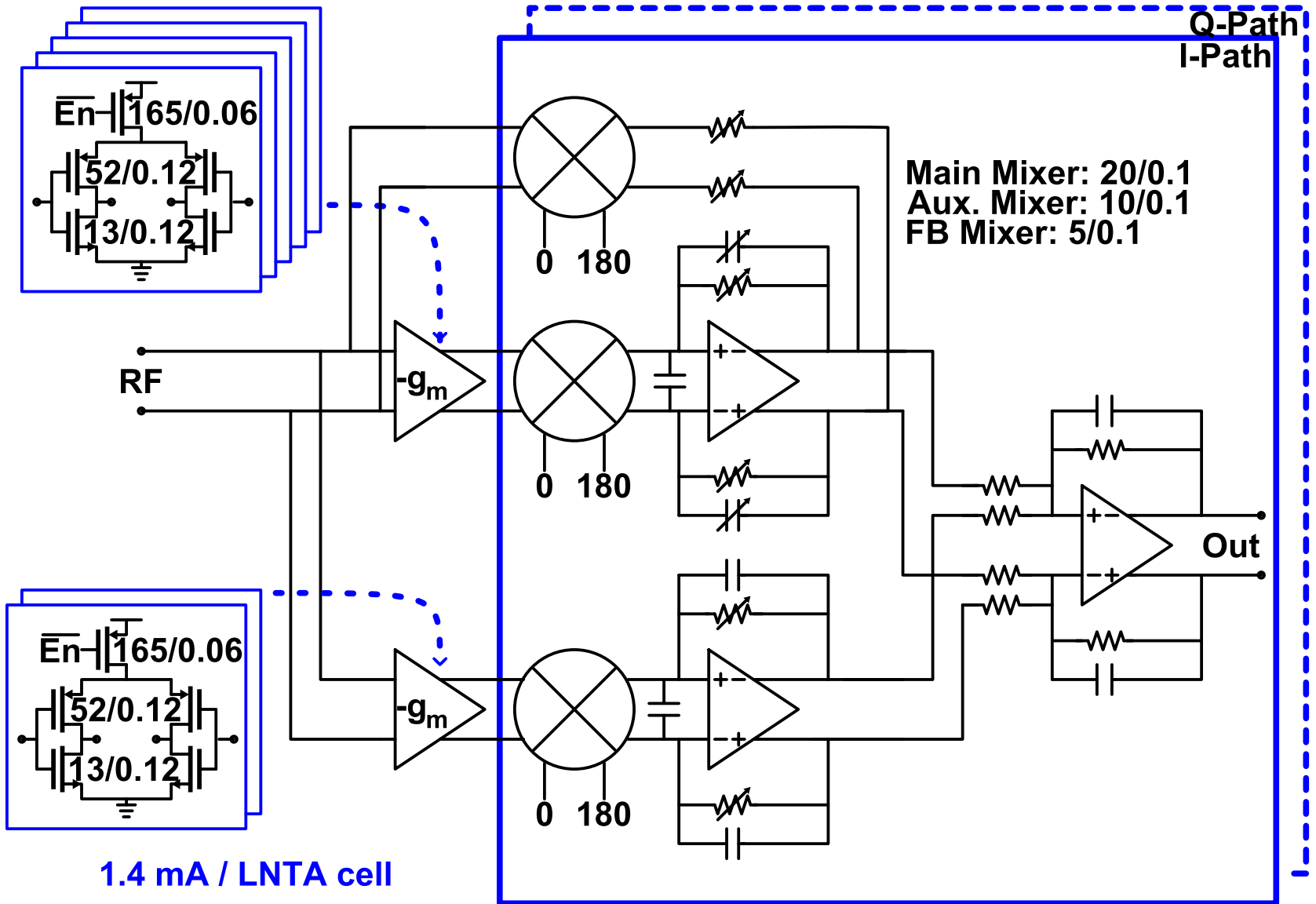
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Implementation



Implementation

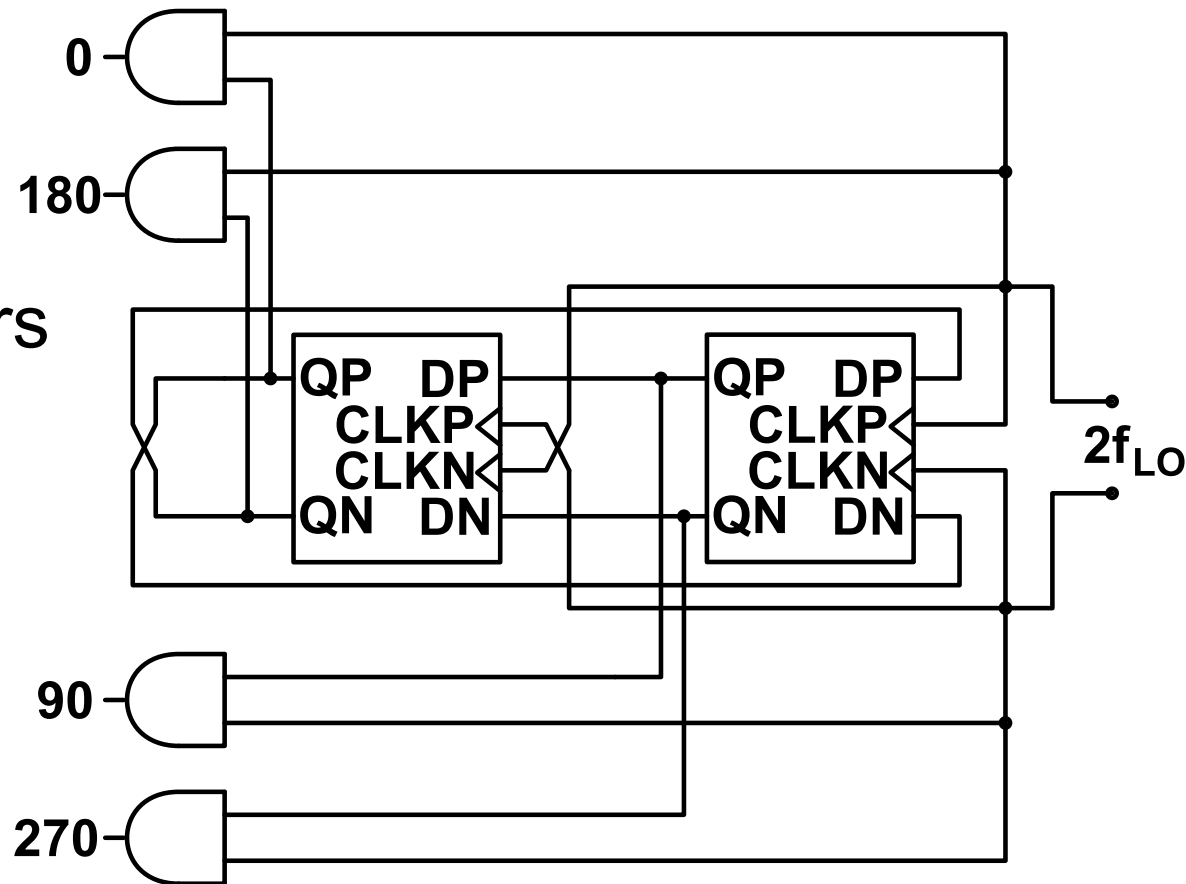


1.4 mA / LNTA cell

LO generation, CML

- CML Div-by-2 core + NAND with inputs

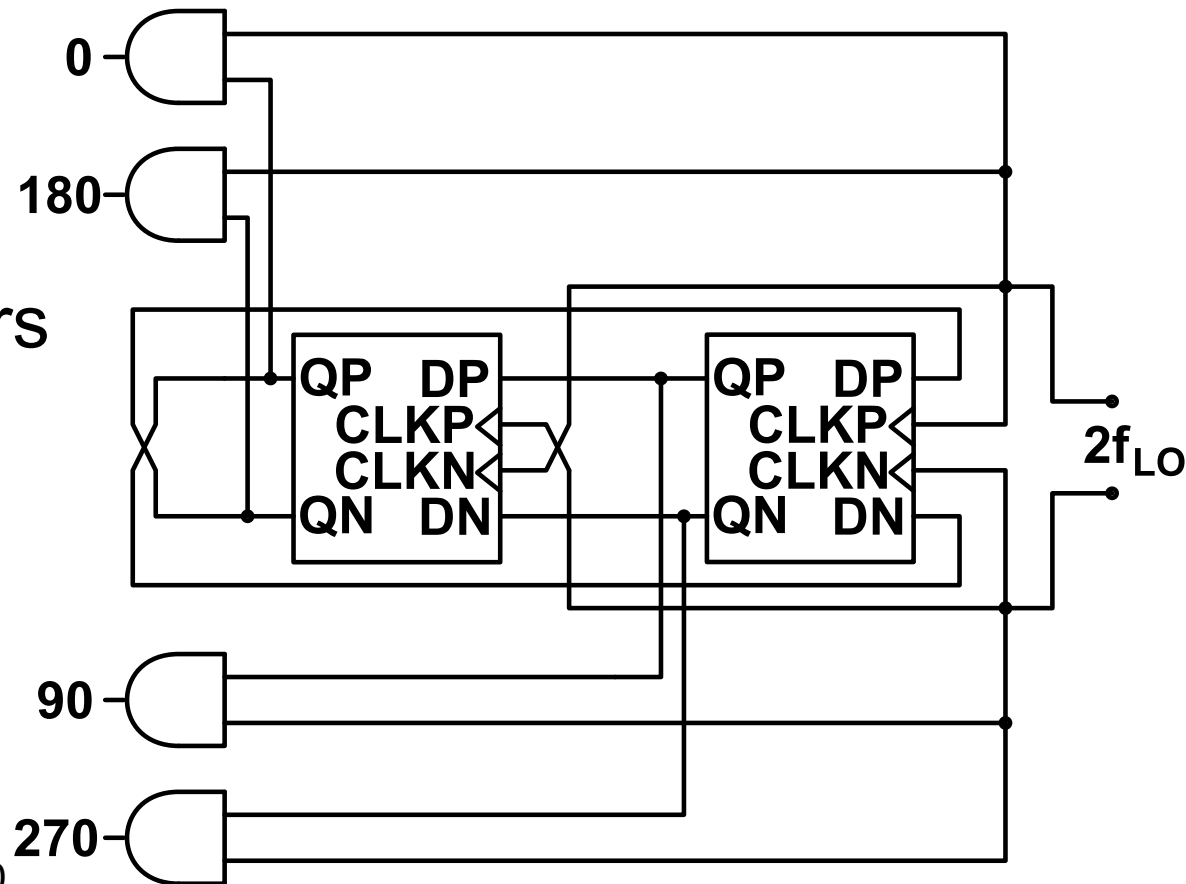
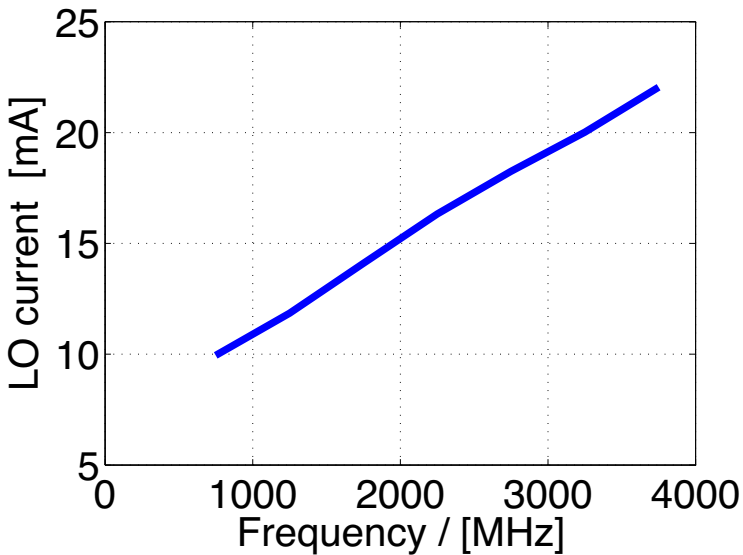
- Fed to all mixers



LO generation, CML

- CML Div-by-2 core + NAND with inputs

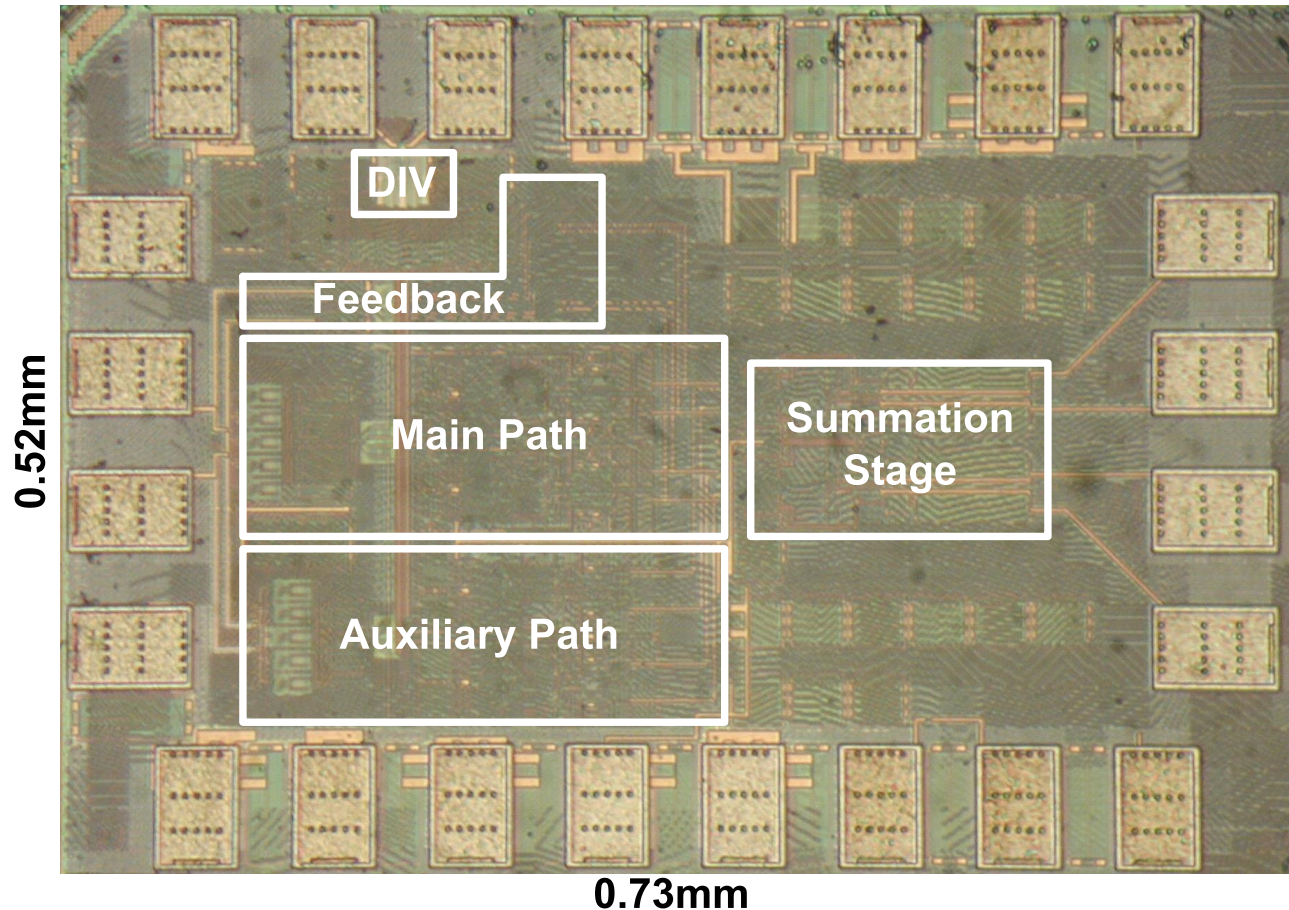
- Fed to all mixers



Outline

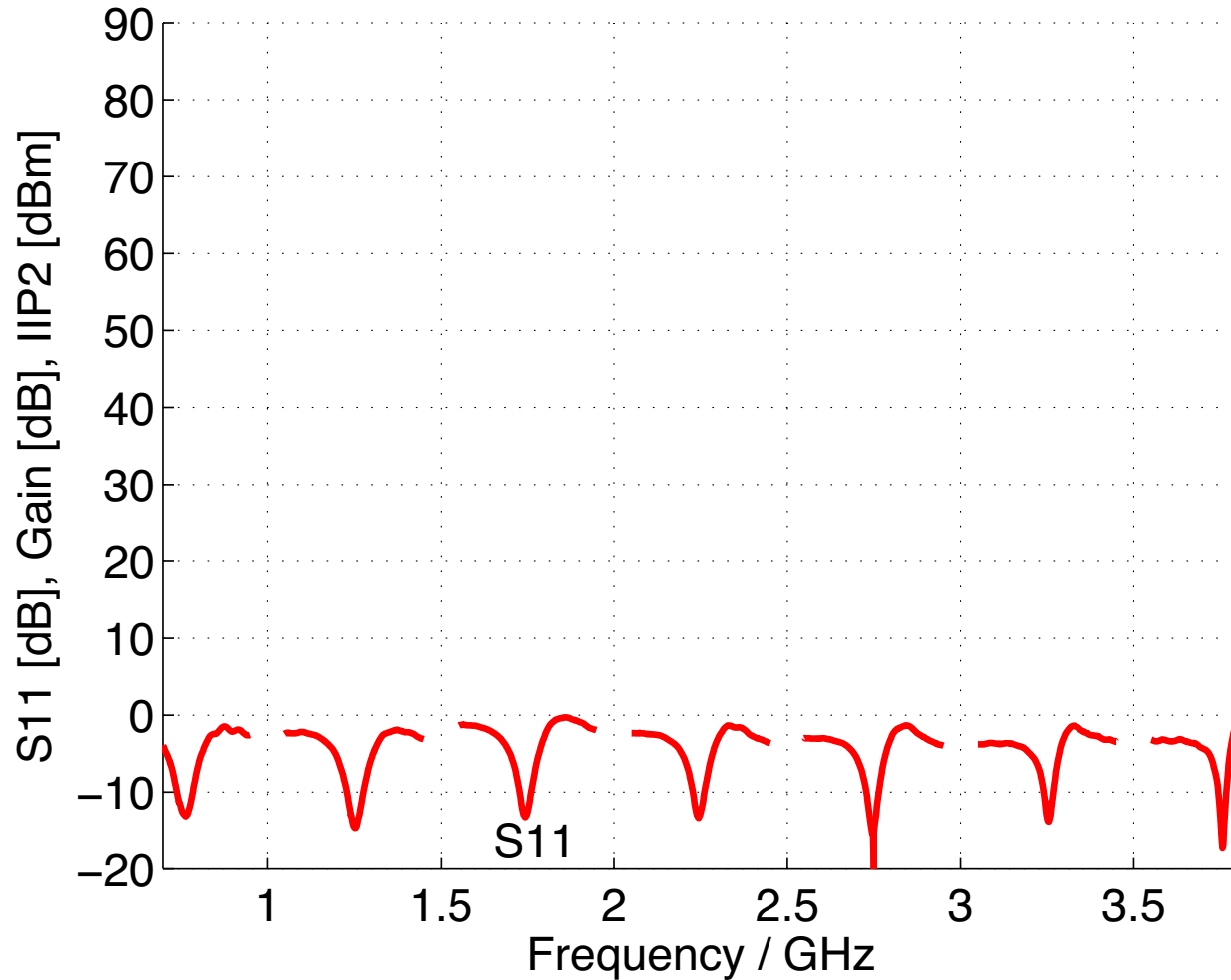
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Results

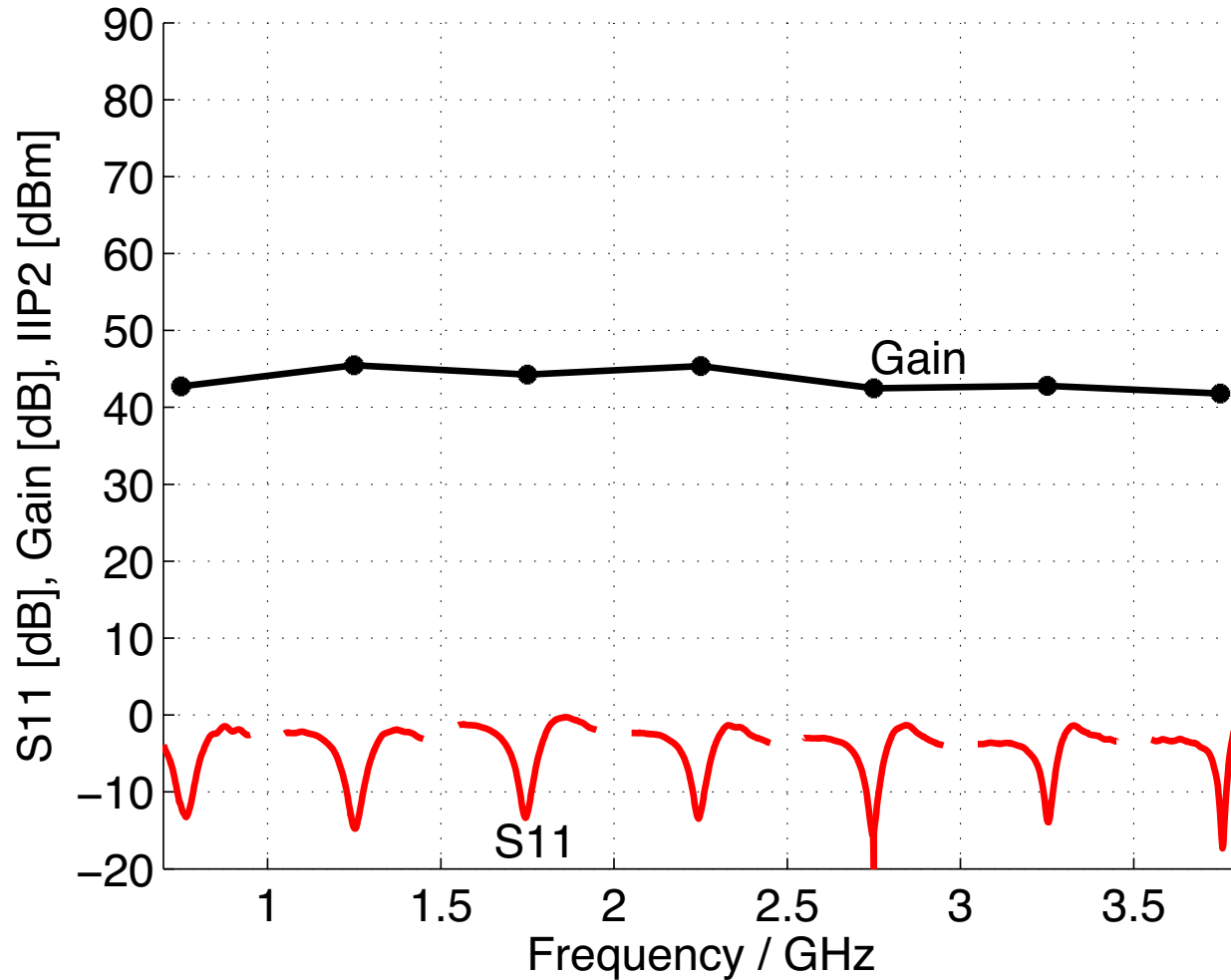


- STMicroelectronics 65nm process
- Total active area: 0.15mm²

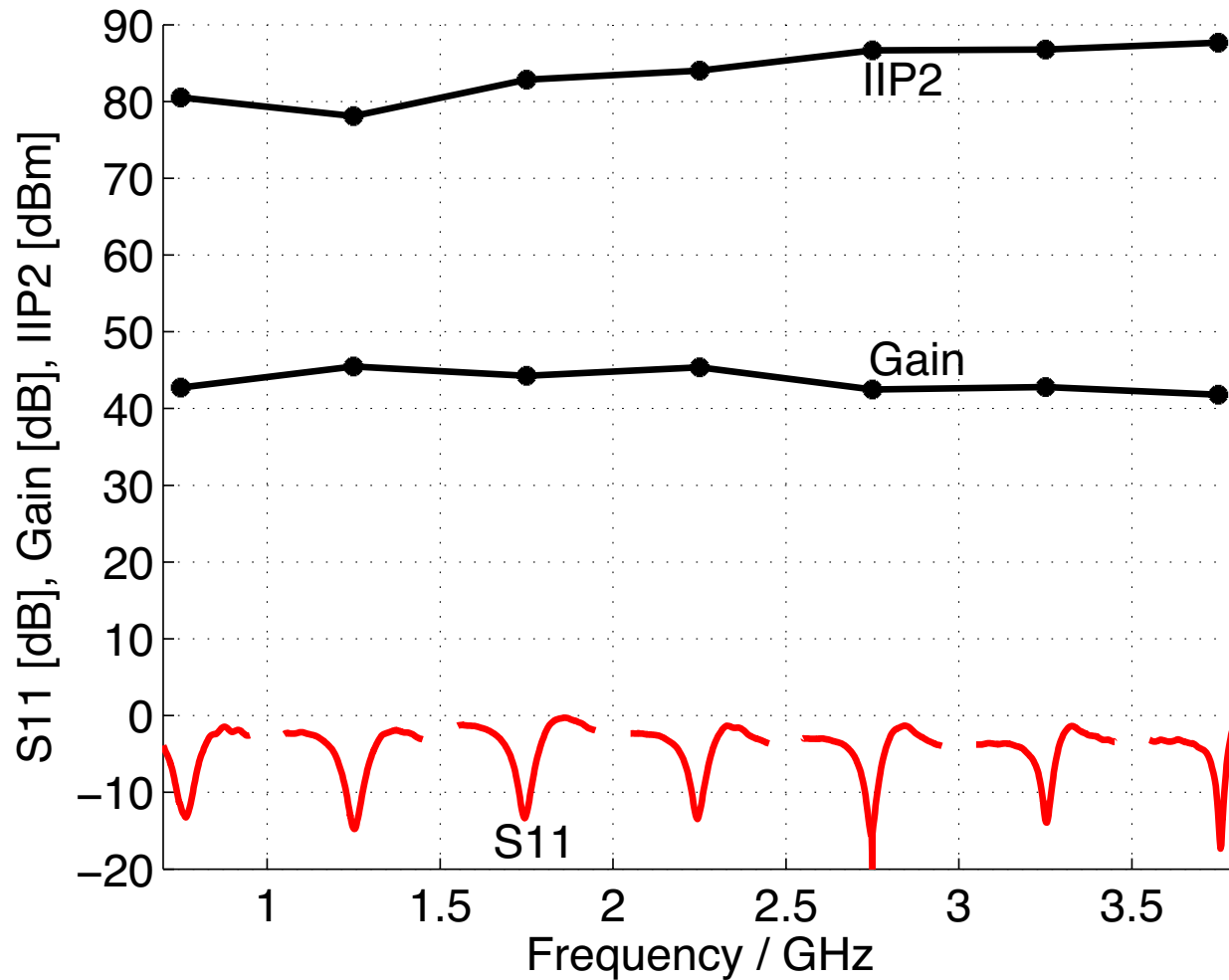
Input Matching, Gain, IIP2



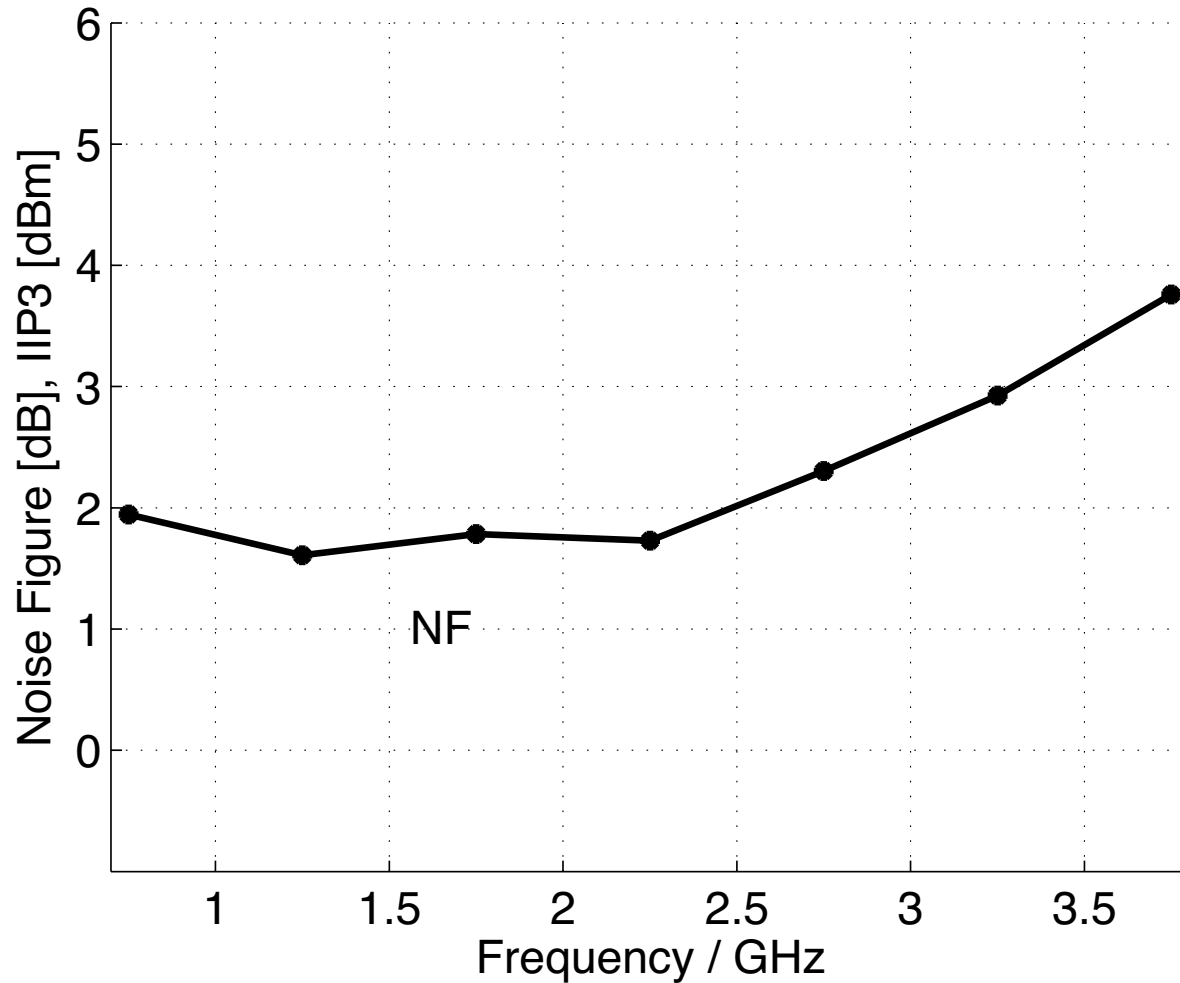
Input Matching, Gain, IIP2



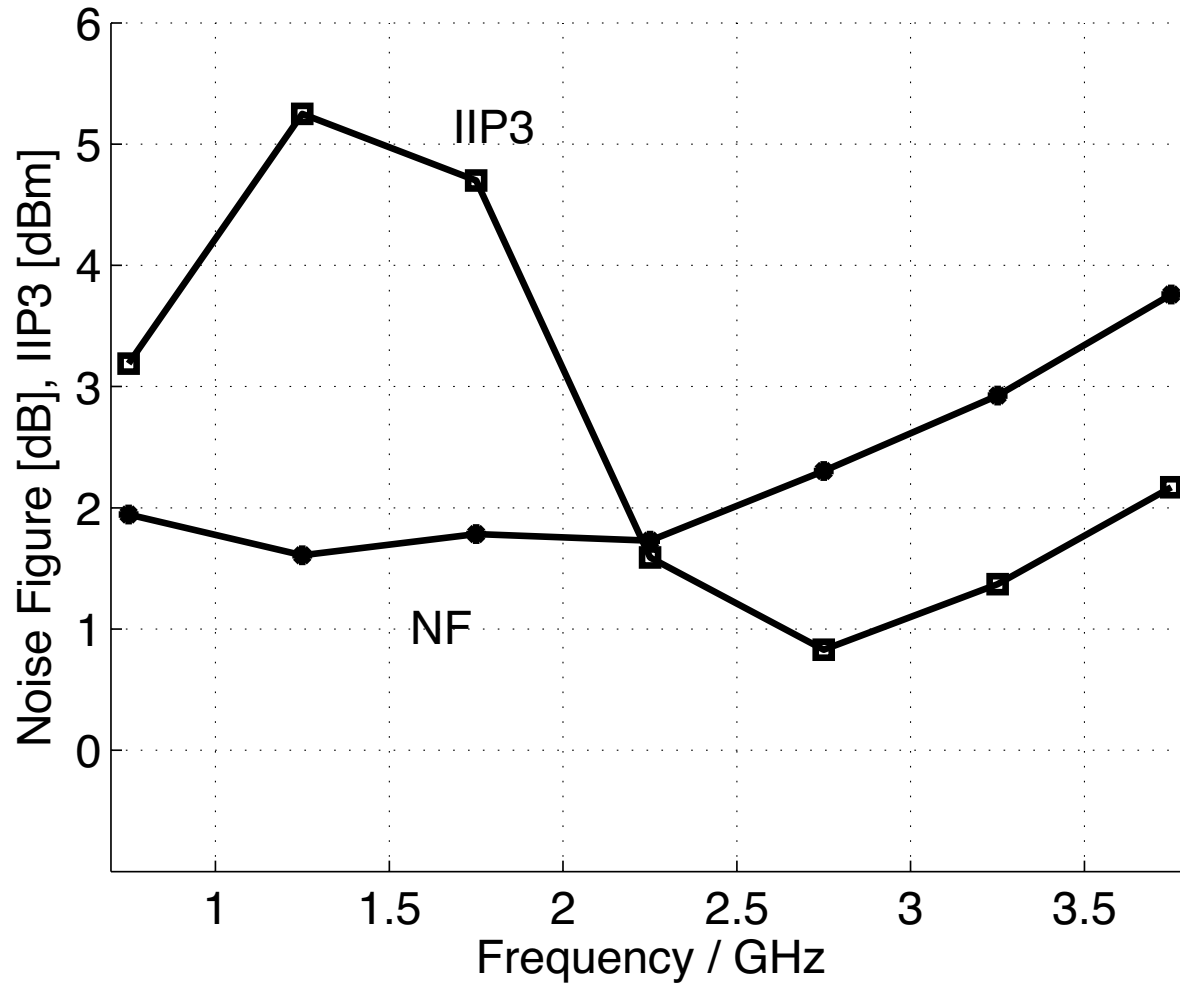
Input Matching, Gain, IIP2



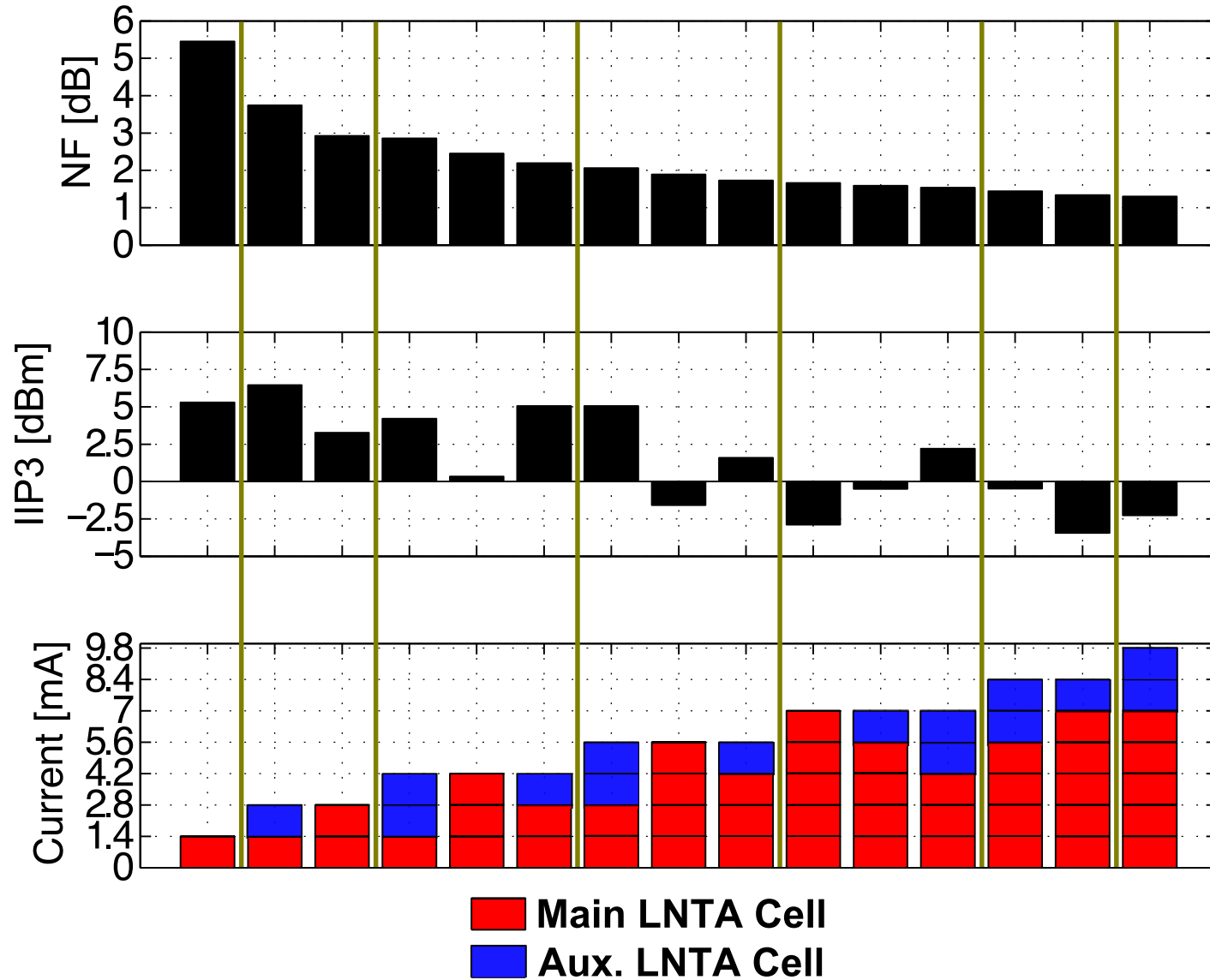
Noise Figure, IIP3



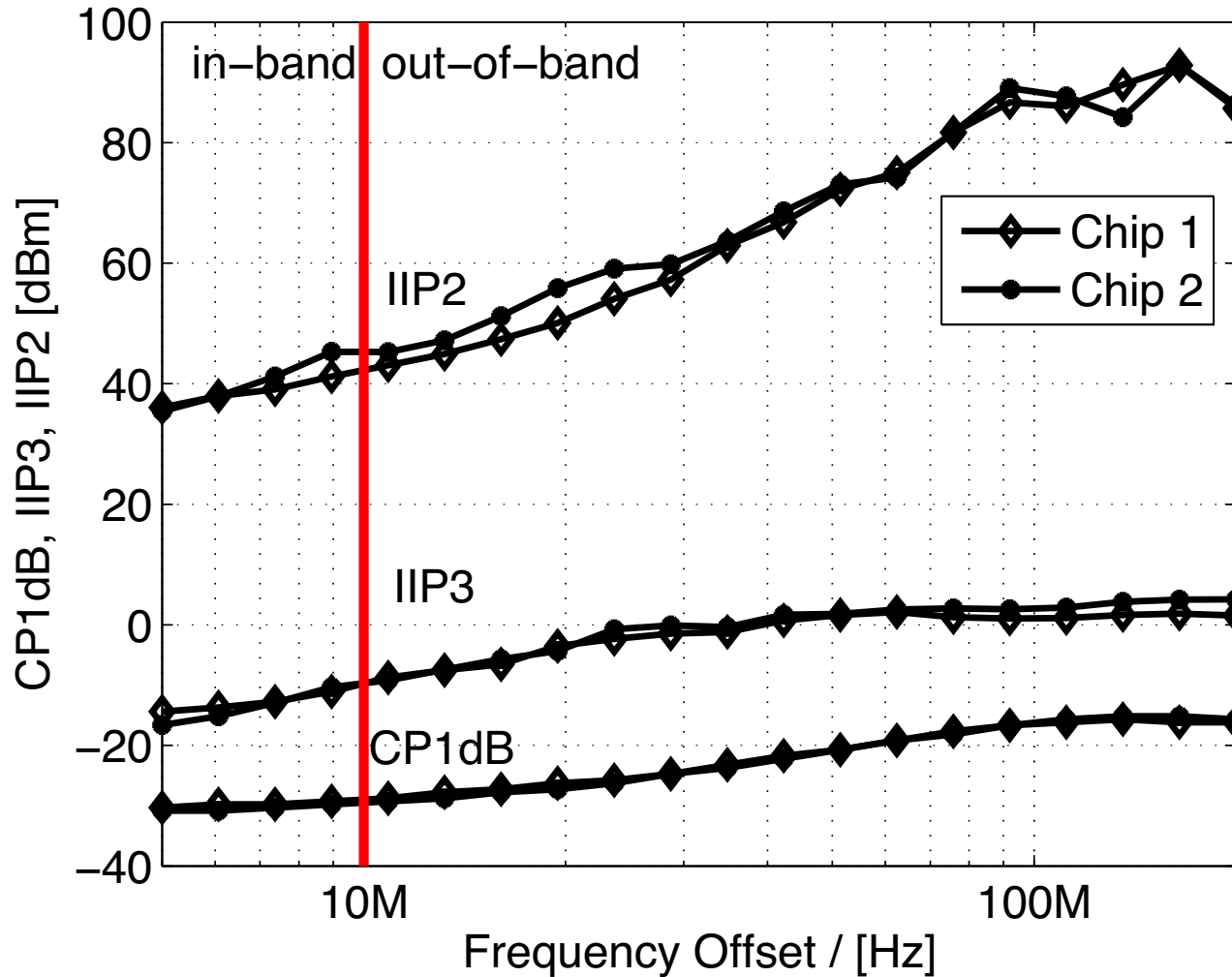
Noise Figure, IIP3



Noise Figure, IIP3 vs. Current



CP1dB, IIP3, IIP2



Performance summary

	ISSCC 2012	ISSCC 2011	RFIC 2013	This Work
Type	Noise Cancelling	Resistive Feedback	Sampling	Noise Cancelling
Frequency / [GHz]	0.01-2.7	0.7-2.1	0.5-3	0.7-3.8
NF / dB	1.9	2.2-2.7	6.8-13.2	1.6-3.8
Gain / dB	70	37	35	45
Current / mA	27-60*	7.3**	208-500*	22.8-34.9
Supply / V	1.3	1.3	1.2	1.2
IIP3 / dBm	+13.5	-3.5	+11.7	+1
IIP2 / dBm	>54	>40	>58	>75
Area / mm ²	1.2	0.2	5.9	0.15
Process / nm	40	45	65	65

*Incl. Harmonic Rejection, **Excl. LO drivers

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Conclusions

- Feedback receiver front-end with frequency selective input match has been demonstrated
- By introducing auxiliary path, noise from main path can be cancelled, and the linearity is better compared to using more current in the main path
- Low noise figure, high linearity, small area

Acknowledgement

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