

LuMaMi - Lund University Massive MIMO testbed

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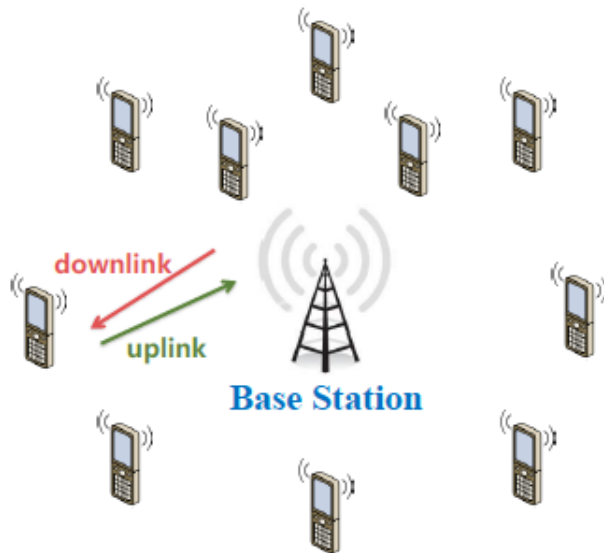
Testbed Challenges

- Large amount of baseband data
 - 100 Ant. * 4 byte for I/Q * 30.72 MS/s ~ 100Gbps
- Synchronization of RF front ends
 - Octoclock
- Processing latency
 - Find suitable frame structure
- Reciprocity calibration
 - RF chains not reciprocal
 - Calibration scheme required
- First testbed of this size worldwide



Testbed used for ...

1) High speed data streaming for multiple users

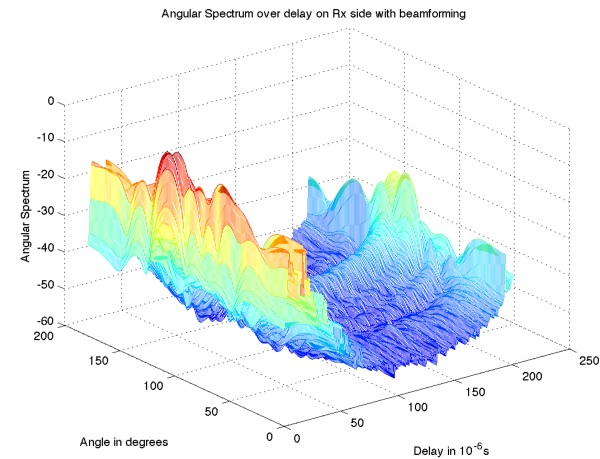
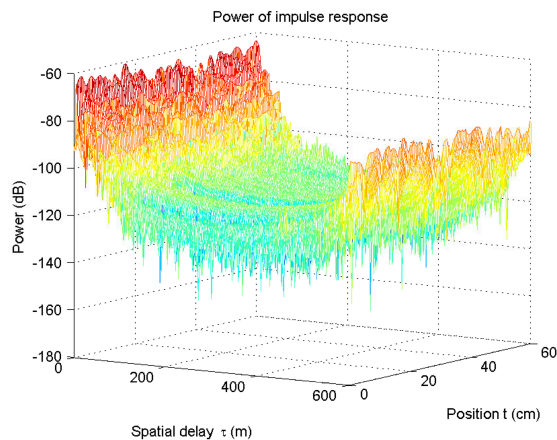


- 10 mobile users stream HD video on uplink to basestation
- Basestation streams 10 HD videos on downlink to users.



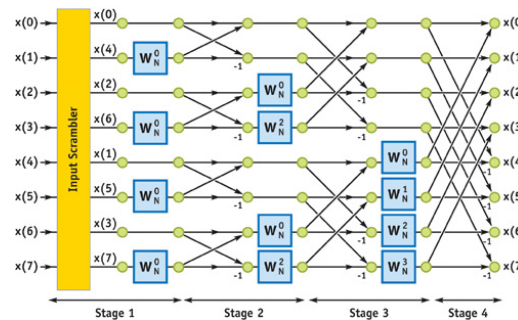
Testbed used for ...

- 1) High speed data streaming for multiple users
- 2) Channel sounding



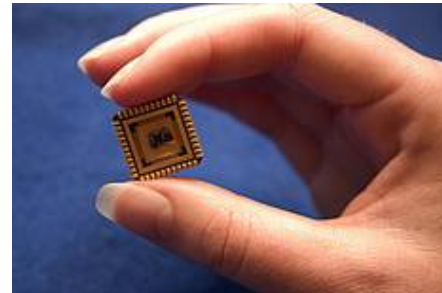
Testbed used for ...

- 1) High speed data streaming for multiple users
- 2) Channel sounding
- 3) Evaluation of baseband solutions (algorithms and architectures)

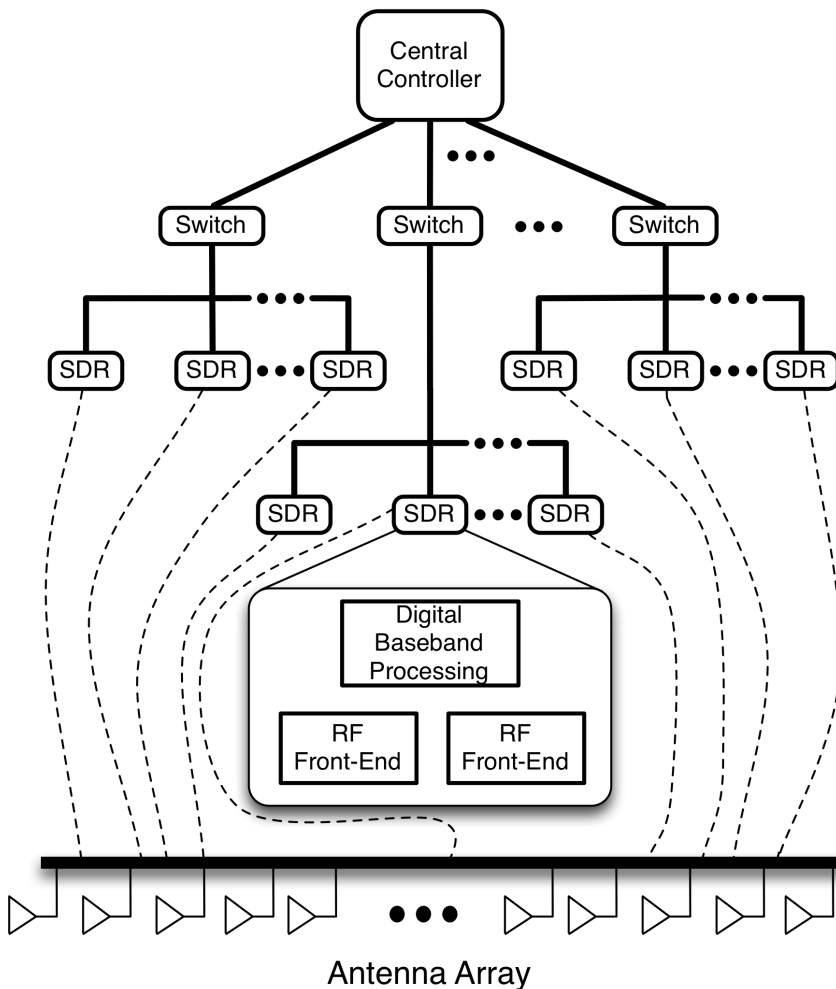


Testbed used for ...

- 1) High speed data streaming for multiple users
- 2) Channel sounding
- 3) Evaluation of baseband solutions (algorithms and architectures)
- 4) Assisting circuit design



General Overview



- Based on Star-Architecture
- Central Controlling Unit
 - Link Evaluation
 - Upper layer protocols
 - Logging data
 - Baseband Proc.
- Switches
 - Routing data
- SDR
 - Baseband Proc.
 - RF-Front End



System components - Overview

SDR



Chassis



Central Controller



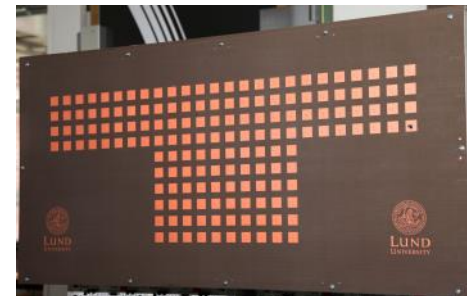
FPGA coprocessor



OctoClock



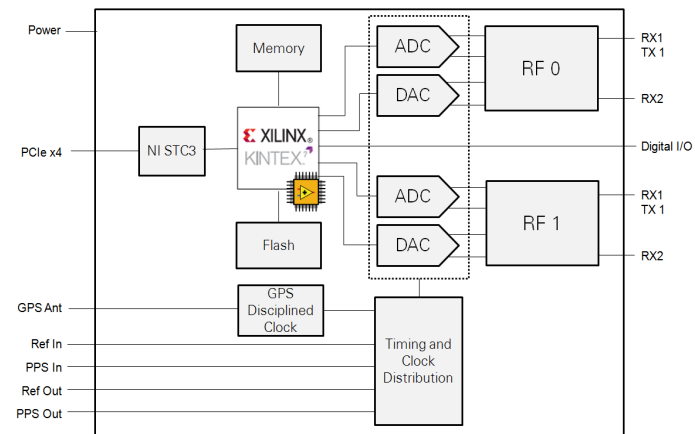
Printed antenna array



System components - SDR

USRP RIO 2953R (Universal Software Radio Peripheral)

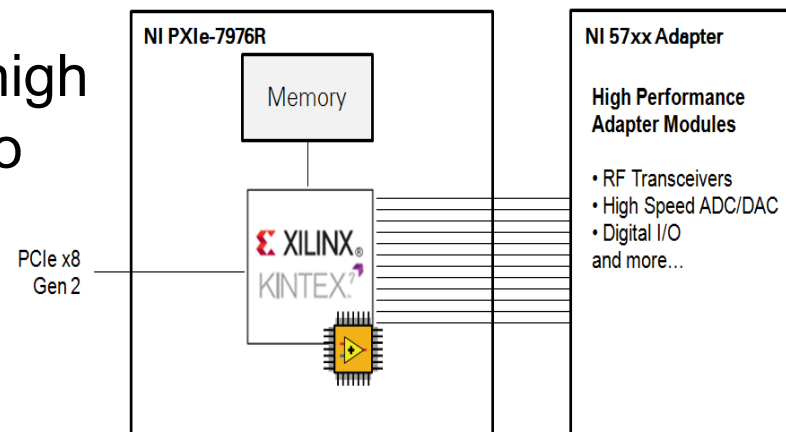
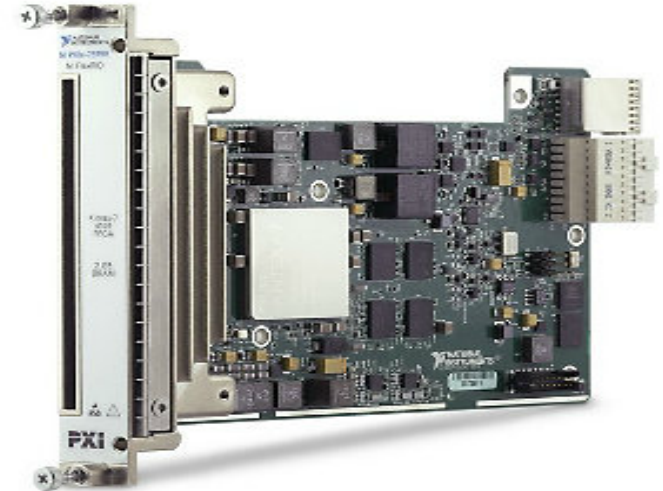
- 2 RF chains
- Xilinx Kintex-7 FPGA
- ~800 MBps bidirectional data streaming
- ~135 MBps baseband data
- Center frequency from 1.2 to 6 GHz



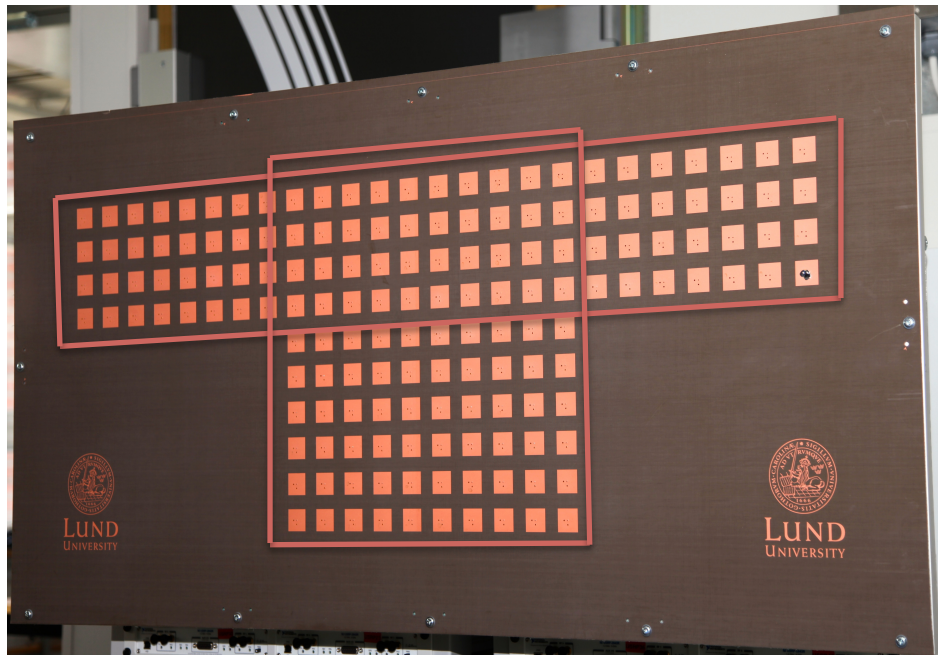
System components – FPGA coprocessor

FlexRIO 7976R (Flexible Reconfigurable Input Output)

- Xilinx Kintex-7 FPGA
- Up to 3.2 GBps data streaming
- Customizable I/O
- Up to 32 simultaneous high throughput connection to other FPGAs
- Used for centralized co-processing



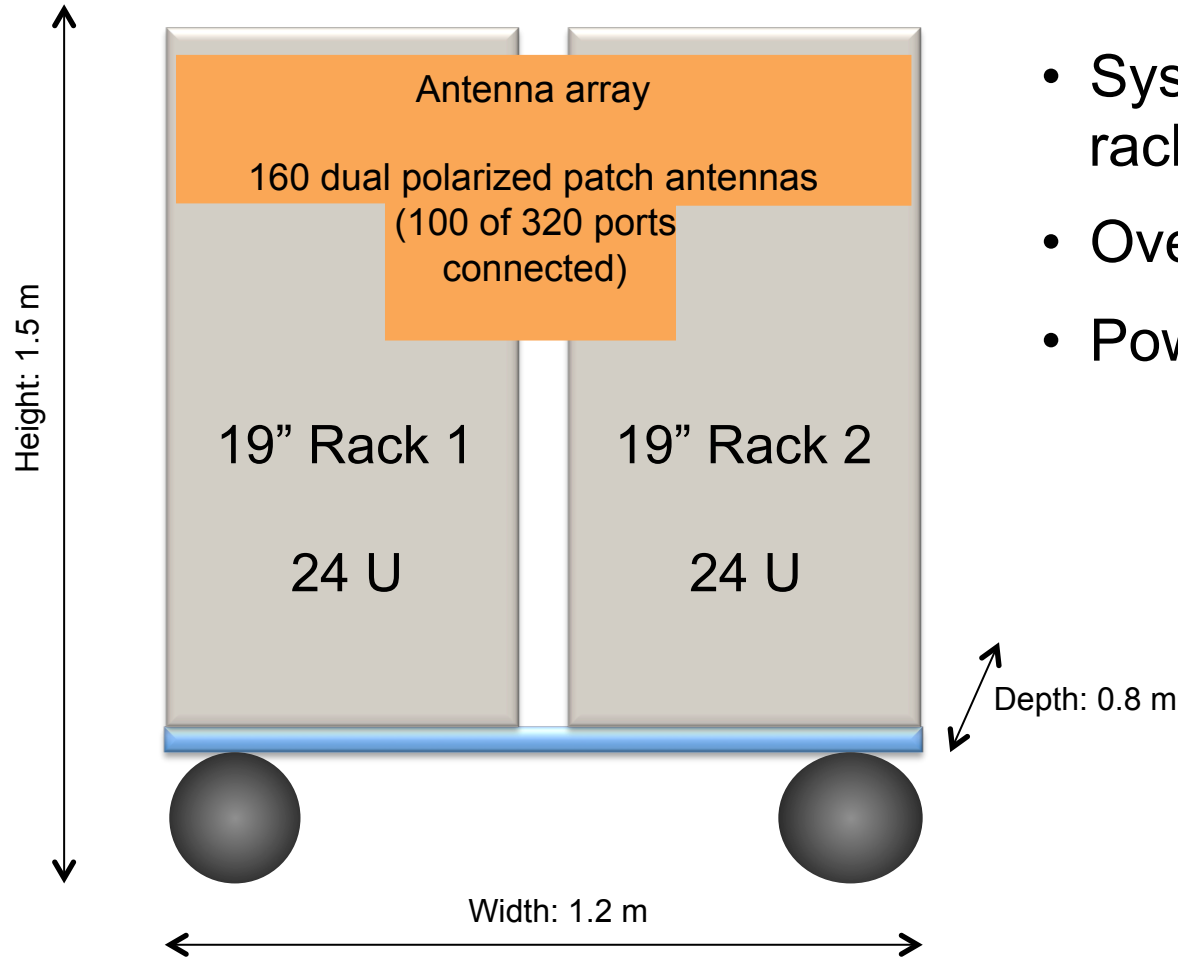
System components – Antenna Array



- Designed at the department for $f_c = 3.7$ GHz
- 10dB bandwidth of 183MHz
- Average antenna match -28dB.
- 160 dual polarized patch antenna array elements
- Allows different configurations
 - 4 x 25
 - 10 x 10
 - etc ...



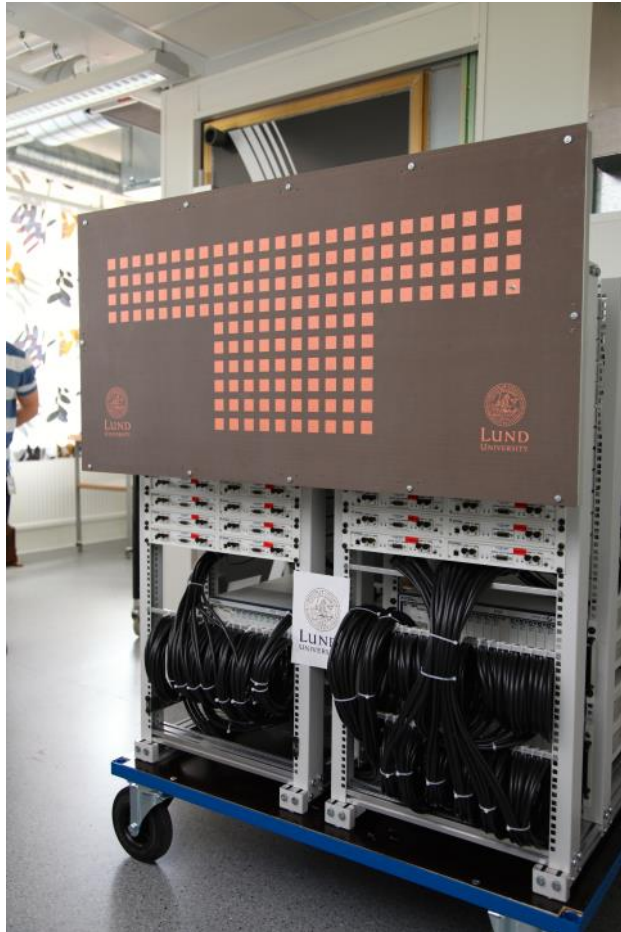
Assembly of "mobile" base station



- System mounted on rollable rack
- Overall weight: 300 kg
- Power consumption: 2.5 kW



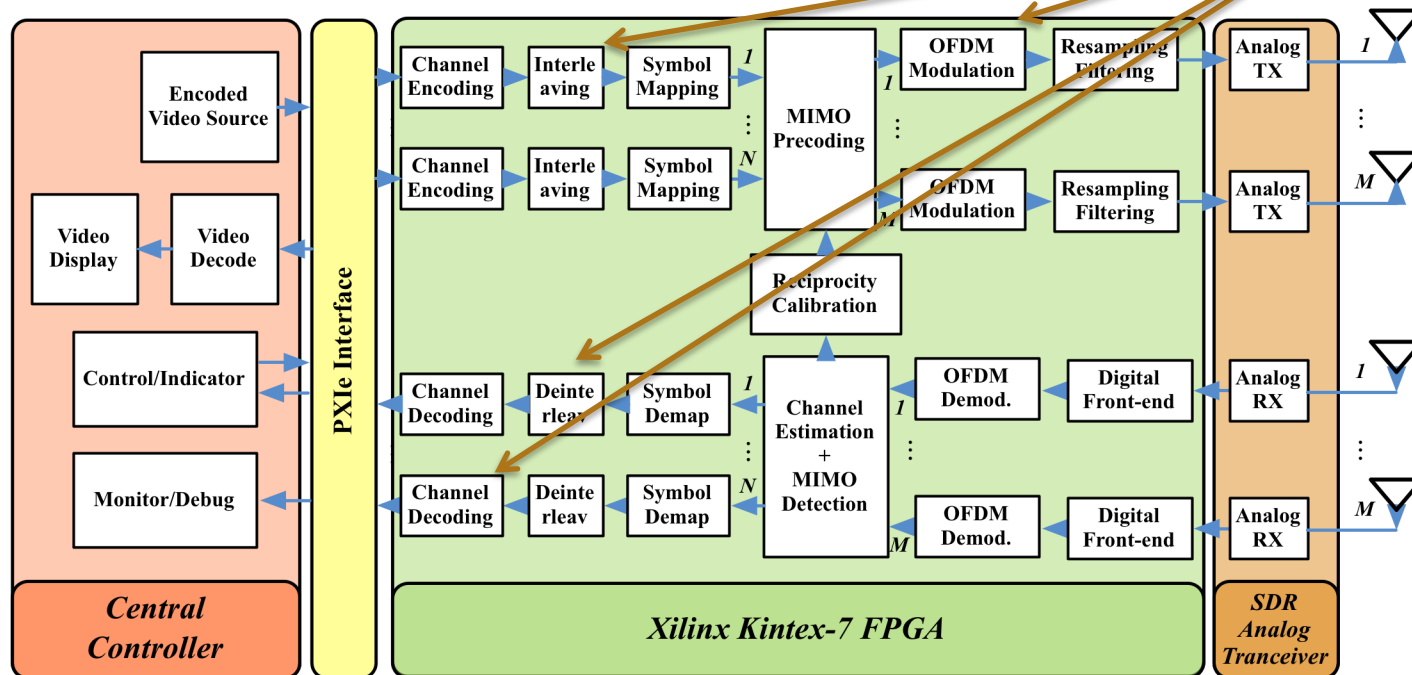
1st Version Assembly



1st version LTE-like OFDM-based massive MIMO transmission

Parameter	Variable	Value
Bandwidth	W	20 MHz
Carrier frequency	f_c	3.7 GHz
Sampling Rate	F_s	30.72 MS/s
FFT Size	N_{FFT}	2048
# Used subcarriers	N_{used}	1200
Slot time	T_S	0.5 ms
Sub-Frame time	T_{sf}	1 ms
Frame time	T_f	10 ms
# UEs	K	10
# BS antennas	M	100

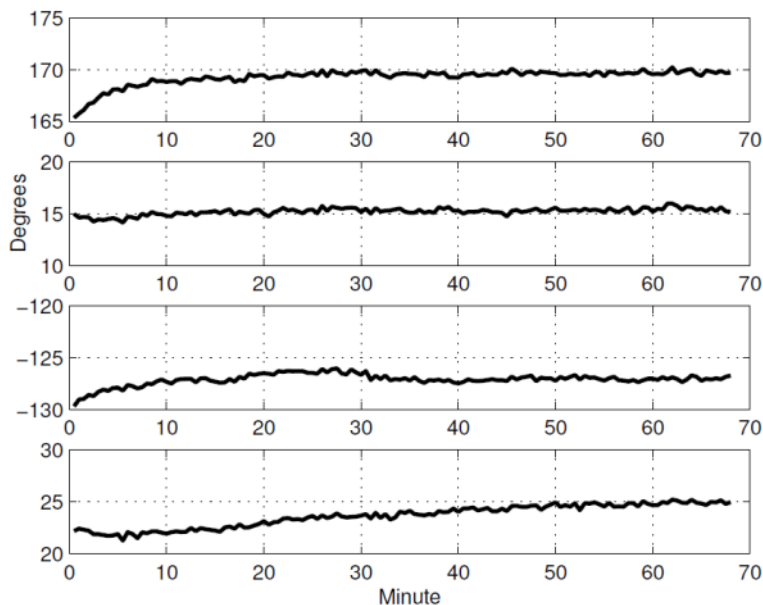
Thank you Xilinx for donating IP blocks



Initial results I

Capabilities of the RF front ends:

Phase coherence

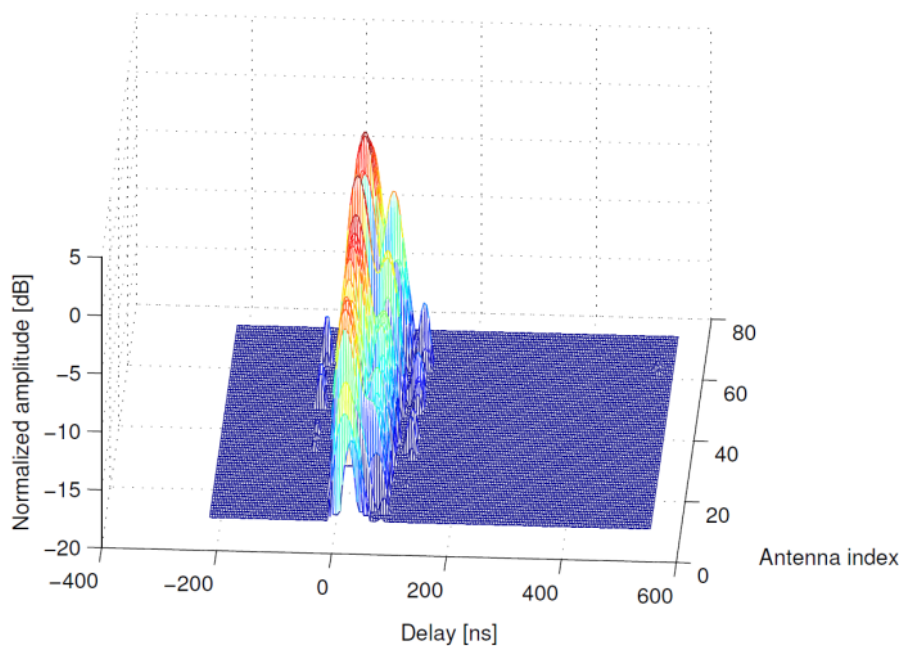


- Requirement: stable frequency response of RF-chains to achieve reciprocity calibration
- Transmit signal by one SDR and split into 4 other signals
- Fig. shows the phases of the received signals
- 5 degree drift during 1 hour of measurements

Initial results II

Capabilities of the RF front ends:

Time synchronization



- 40 MHz Gaussian PN sequence transmitted by single antenna
- 16 x 4 Rx antenna subset with roughly same distance to Tx
- Strong LOS channel to verify sampling synchronization capabilities;
- Distinctive planar wavefront with a small delay spread;
- The received samples are time aligned within one 40 MHz sample

Ongoing Work

- **Short term goal:**
 - A demonstration of massive MIMO at the uplink using MR and ZF combiners
- **Long term goals:**
 - Implementation of uplink/downlink frame structure, reciprocity calibration, etc, for uplink/downlink transmission
 - Reduced/no PAR, precoders
 - Establish performance boundaries for practical Massive MIMO systems