E-band SiGe Beamsteering Transmitter Building Blocks

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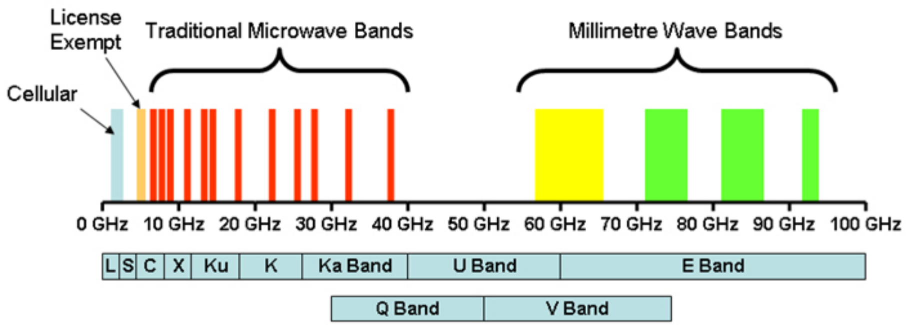
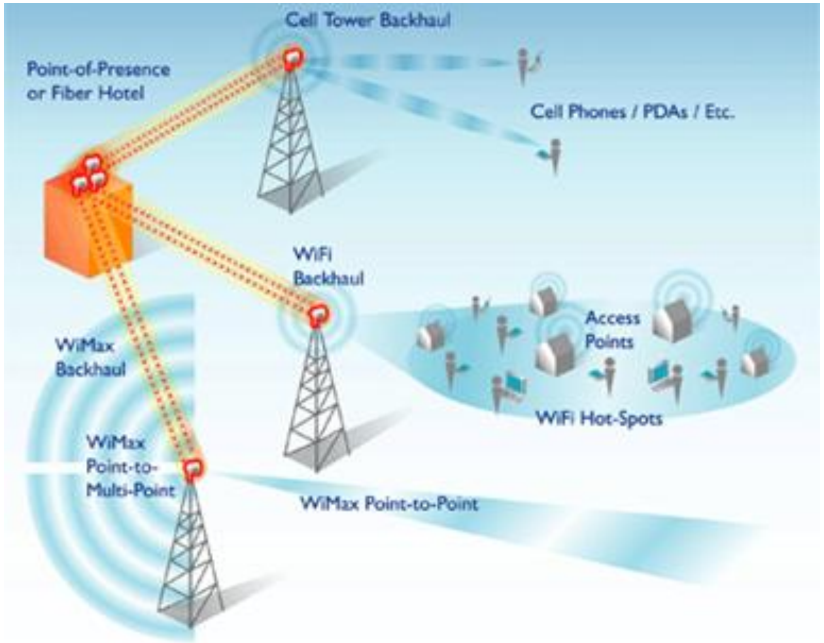
Presentation outline

- **E-band wireless backhaul**
- **Beam forming concept**
  - Linear timed and phased arrays
- **Transmitter architecture**
- **Designed building blocks**
  - 28 GHz QVCO with I/Q phase error tuning and detector
  - 28 GHz to 1.75 GHz Divider
  - PA version 1
  - PA version 2
  - PA version 3: diploma thesis
- **Conclusions**

E-band wireless backhaul

- **The E-band at 71-76 GHz and 81-86 GHz: wireless point-to-point communication**
- 5 GHz of spectrum $\Rightarrow$ data rates of Gb/s



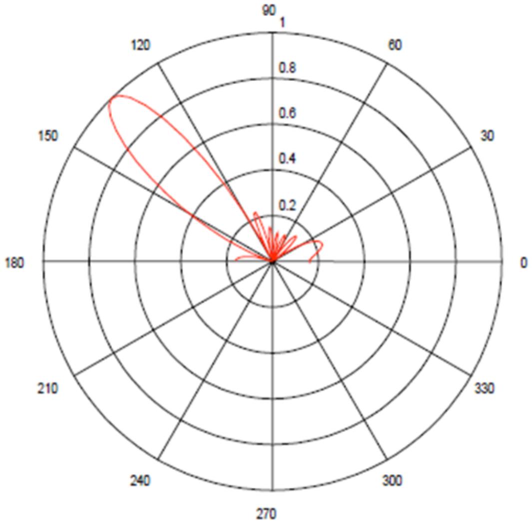


- costly optical fiber backhaul $\Rightarrow$ wireless data link
- Heterogeneous networks: macro, pico and femto cells $\Rightarrow$ **large number of base stations**

A wireless backhaul is highly advantageous

Beamsteering concept

- Beamsteering ⇒ equal to spatial filtering of radio signals
- Array of antennas ⇒ steered to block transmission to certain directions and to provide antenna gain to a desired direction

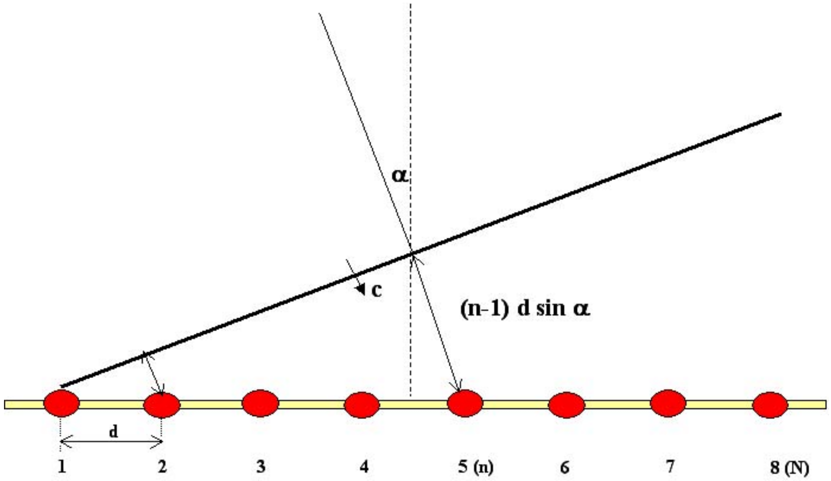


- Applications:

  - Radio communication
  - Surveillance
  - Radar
  - Sonar
  - Audio

Linear timed arrays

- Linear equally spaced array with 8 TX antenna elements
- Wave plane at transmit angle α



- Different time of departure Δt

$$\Delta t = \frac{(n-1)d\sin\alpha}{c}$$

c= light speed, d = element spacing

- Beamforming transmitter: aligns the signals to the antenna elements in time

$\Rightarrow$ **Coherent combination to one direction and suppression to other directions**

Use a small fractional BW $\Rightarrow$ Realization of time delay with **fixed phase shift** $\Rightarrow$ **Linear phased array**

E-band transmitter architecture

Unpublished material

28 GHz QVCO plus phase error detector and tuner

Unpublished material

QVCO phase error detector

Unpublished material

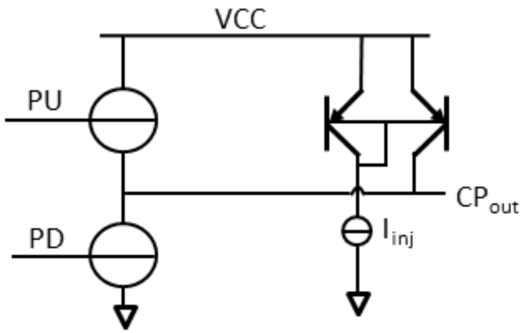
28 GHz QVCO with phase error detector and tuner

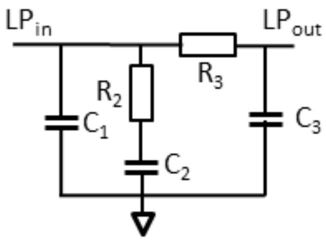
Unpublished material

Divide by 16

Unpublished material

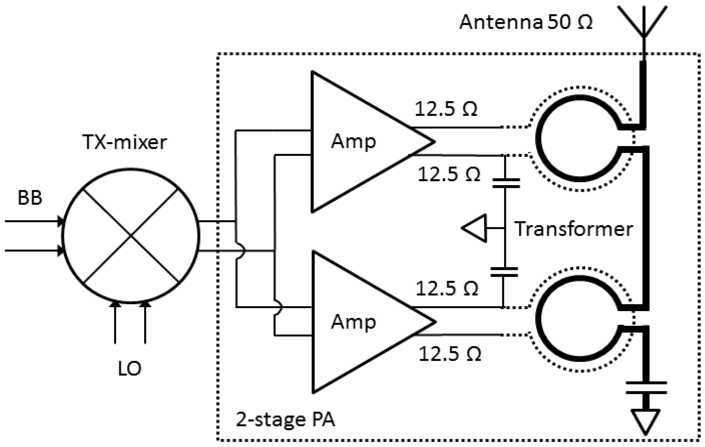
Beam steering implementation with PLL



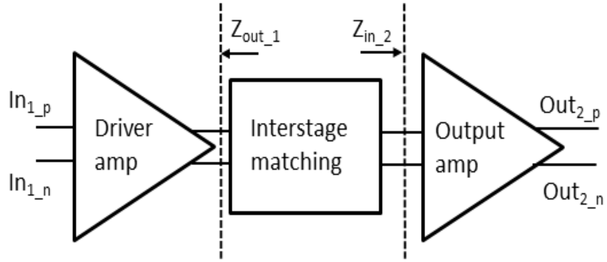


Unpublished material

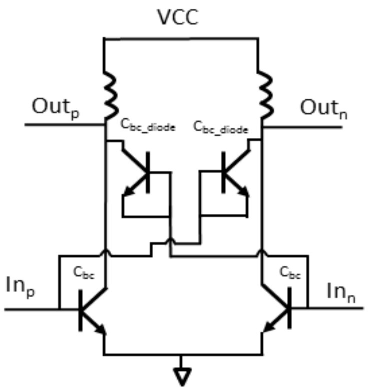
Power amplifier architecture



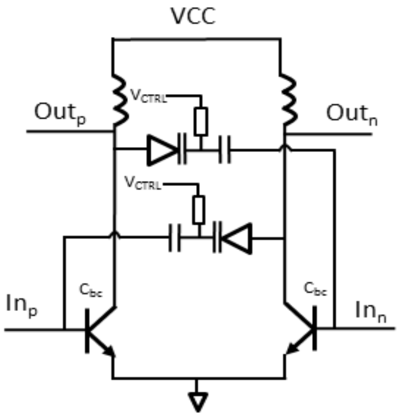
50 Ω antenna impedance transformed to 12.5 Ω ⇒ lower VCC



Stage 1 and 2 Version 1

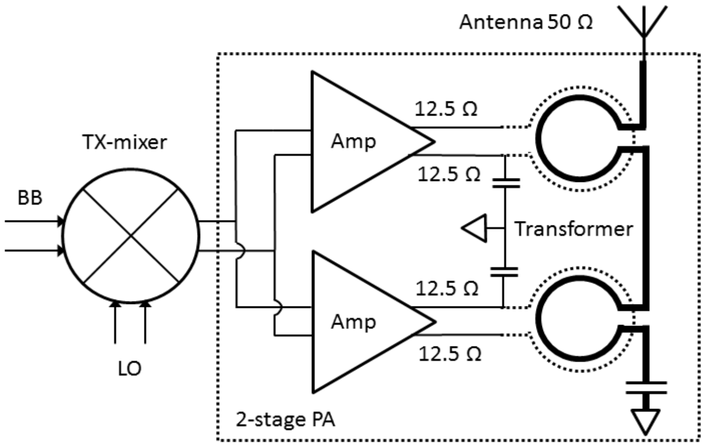


Stage 1 Version 2

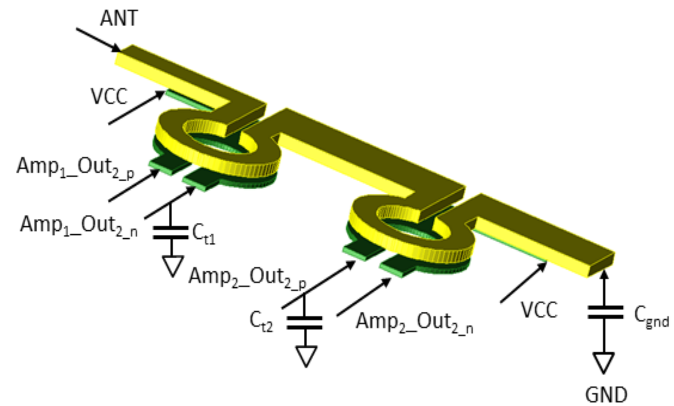


Capacitive cross coupling with diode connected devices to neutralize base collector capacitance

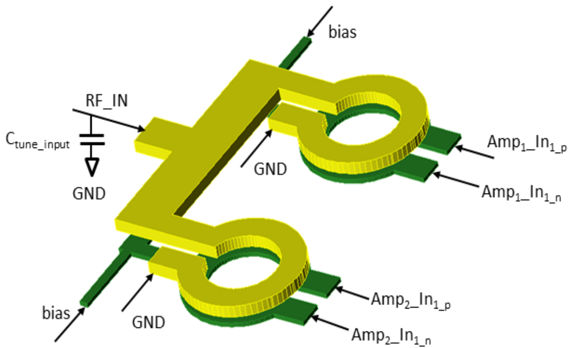
Power amplifier transformers



Output transformer

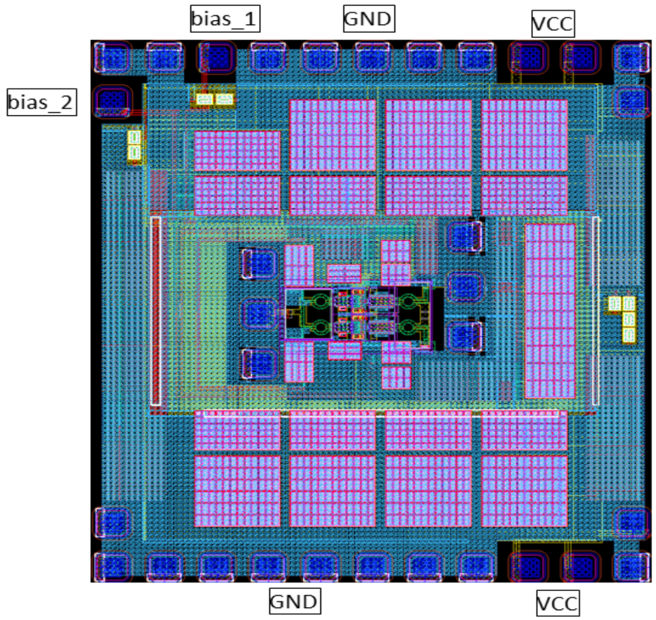


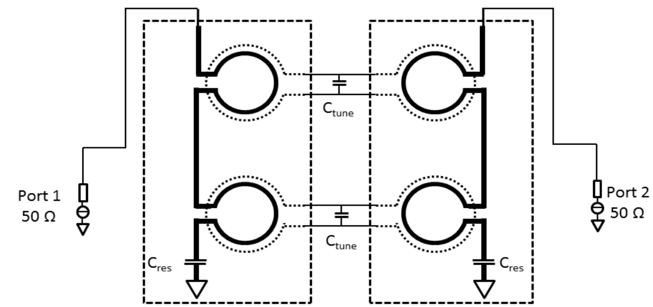
Input transformer

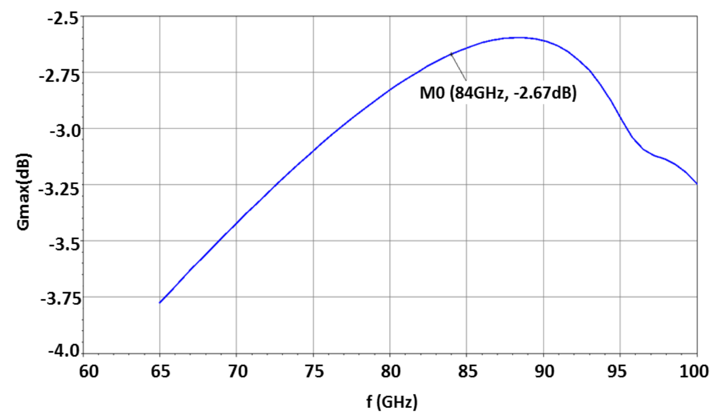


- 50 Ω antenna impedance transformed to 12.5 Ω single ended ⇒ lower VCC for same CP_{1dB}
- Tuning capacitors: reduce imbalance for improved power combination
- Input transformer: 50 Ω antenna impedance to 100 Ω differential for each amplifier

Transformer simulation results and chip layout







- **Chip area: 0.87 mm^2**

- **Output transformer loss: two transformers back to back ⇒ G_{max} = - 2.67 dB ⇒ 1.34 dB loss for one transformer**

Power amplifier simulation results

Version 1

Unpublished material

Power amplifier simulation results

Version 2 – gain versus varactor voltage

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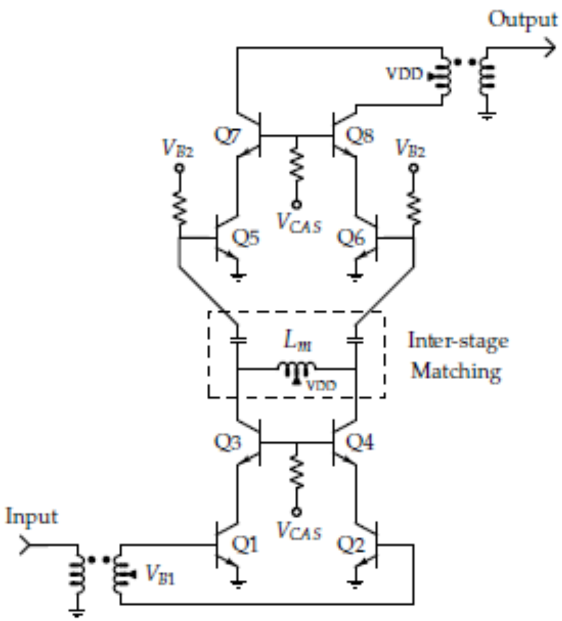
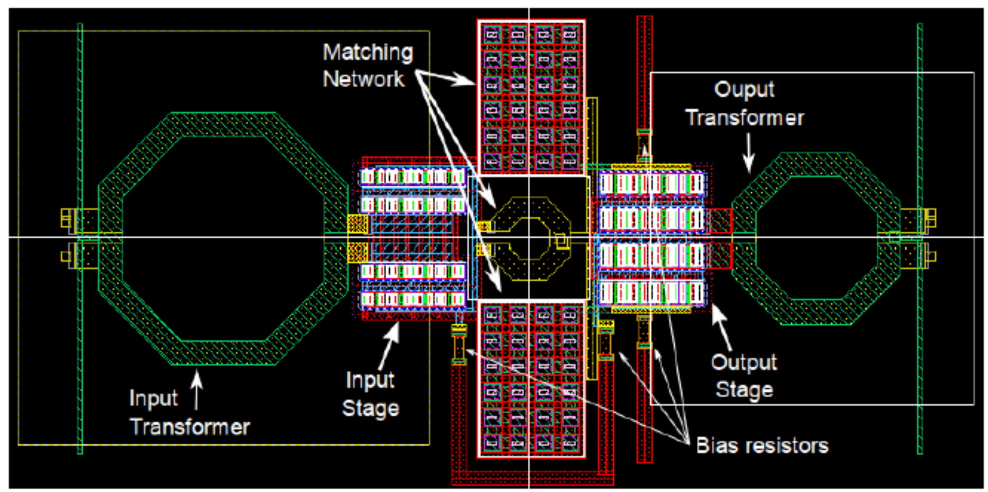
Power amplifier diploma thesis

Version 3 by Manuel Beljano

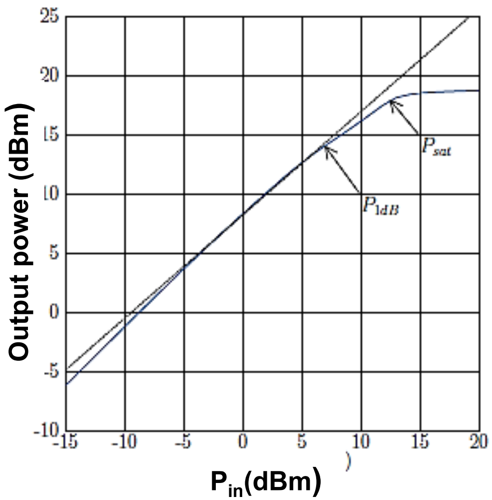




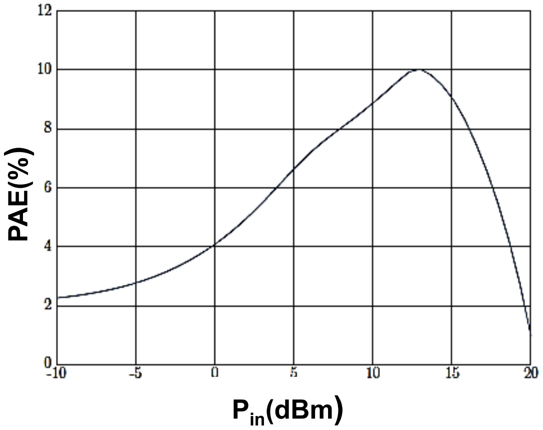
- **Cascode architecture**
- **VCC = 3.5 V**

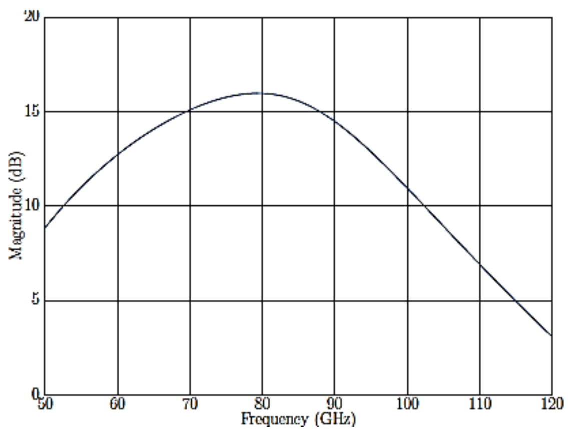
Power amplifier simulation results

Version 3: diploma thesis



VCC = 3.5V
Gain = 16 dB
PAE = 7.5 % at CP_{1dB}
CP_{1dB} = 14.1 dBm
P_{sat} = 18 dBm





Conclusions

- **Project status September 2014**
- **Designed TX blocks: 28 GHz QVCO**
  Three power amplifiers
  Divider
  PLL with phase control
- **Remaining TX blocks:** 28 GHz I/Q mixer
  84 GHz mixer
- **Complete beam steering transmitter to be taped out in December 2014**