CMOS Switched-R-C Techniques for Interference Rejection and Self-Interference Cancellation

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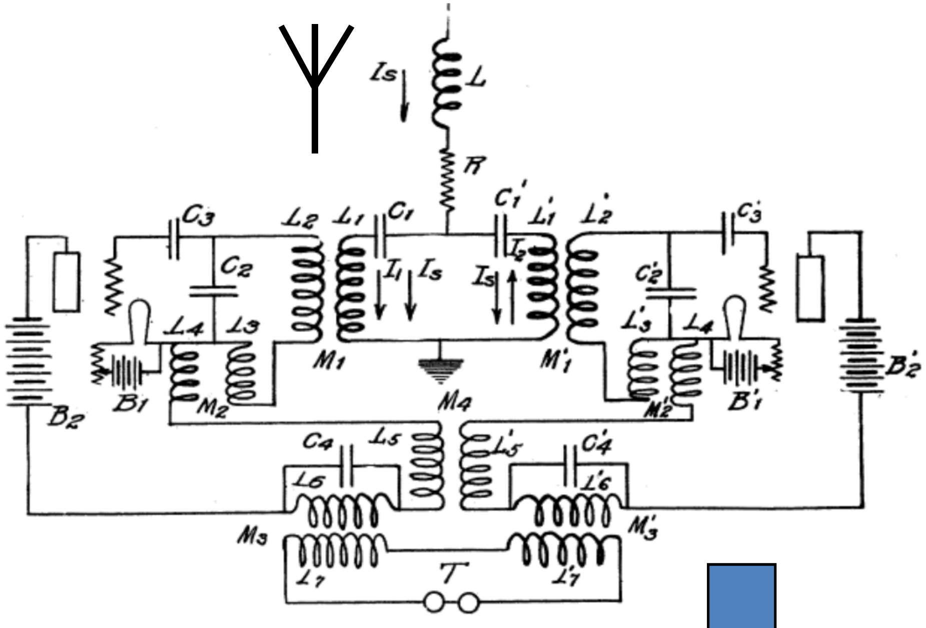
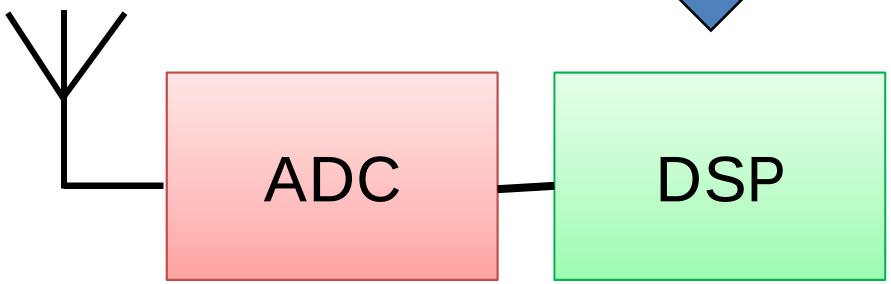
Trend to remove dedicated filtering

- Armstrong 1915



- Dream

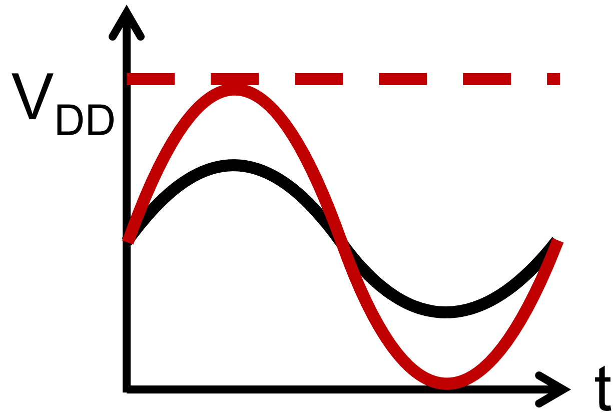


Key Observations:

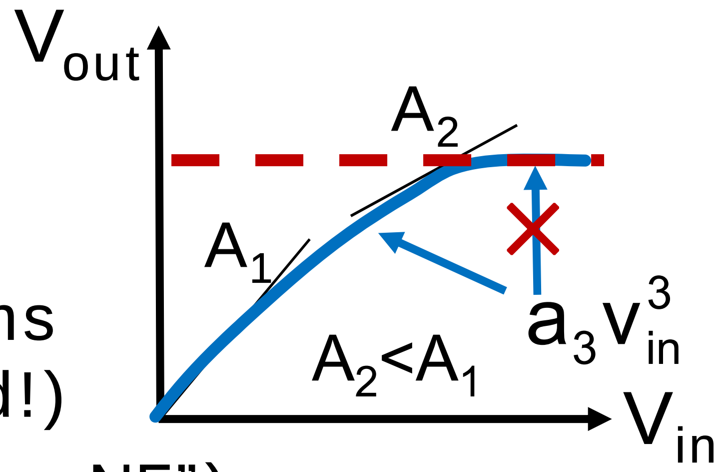
- Trend Analog ⇒ Digital
- Still analog needed for feasibility
- Flexibility ⇔ less RF pre-filtering
- Different names:
  - "SAW-less"
  - "Inductorless", "wideband"
  - Reconfigurable
  - Software Defined Radio (SDR)
  - Cognitive Radio
- Focus on flexible techniques to:
  - Handle blockers ⇔ high CP1dB, IIP3 needed
  - Reject interference flexibly⇔ filter/cancel selectively

Compression Problem

- P_{RF}=0 dBm ⇔ 1mWatt ⇔ .63 $V_{pk\text{-}pk}$ in 50Ω
  - Typical supply: VDD=1.2V
  - 6dB gain ⇔ clip to VDD!

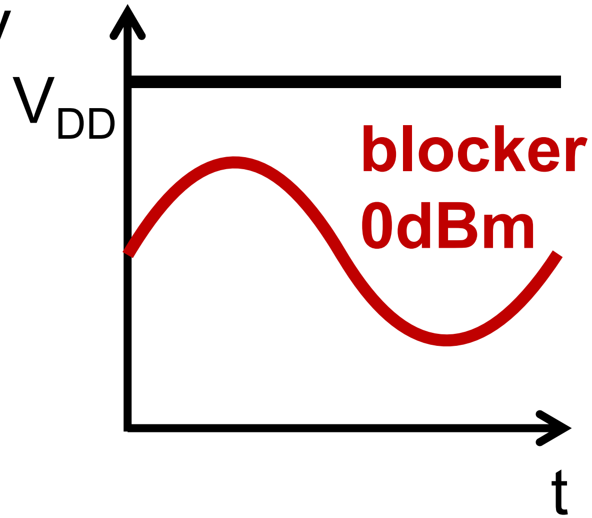


- Compression:
  - reduced gain: A2<A1
  - ...to hard clipping/blocking
  - renders "Cross-modulation"
  - Higher order distortion terms (IIP3/IIP2 model NOT valid!)
  - Higher Noise Figure ("Blocker NF")



How to cancel strong blockers?

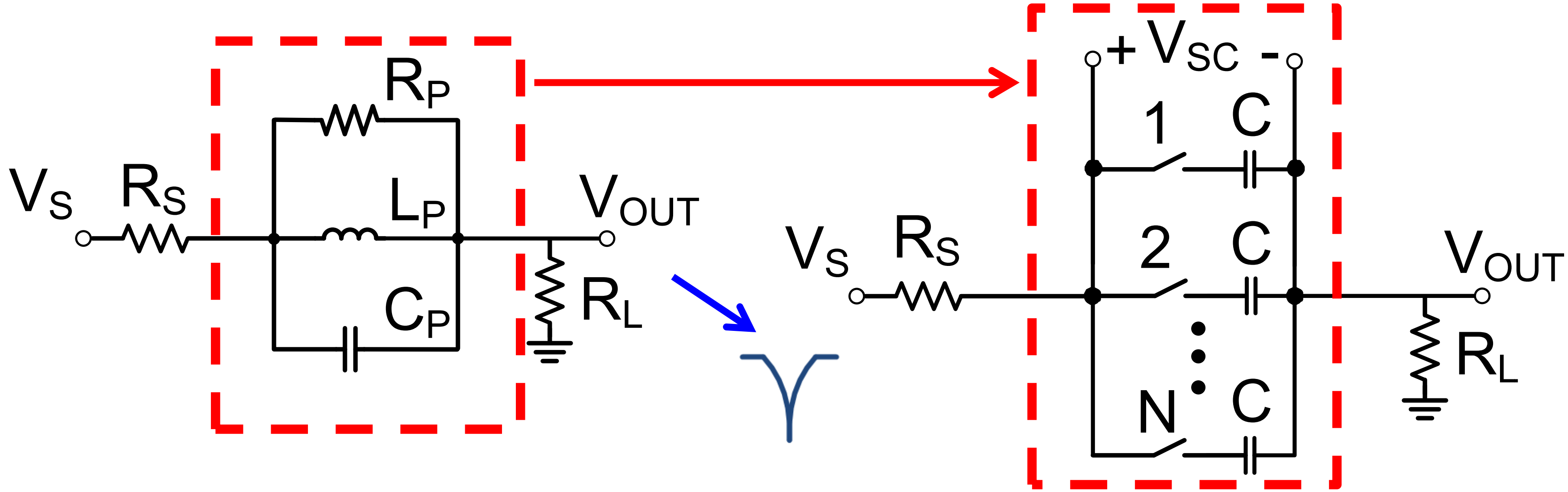
- Gain ⬄ clipping and nonlinearity
- Start Passive, reject "upfront"!!
- Traditionally:
  - SAW-filter: fixed frequency
  - L-C "tracking" filter: $\omega_0 = \frac{1}{\sqrt{LC}}$ (limited tuning-range, limitted Q and big size)

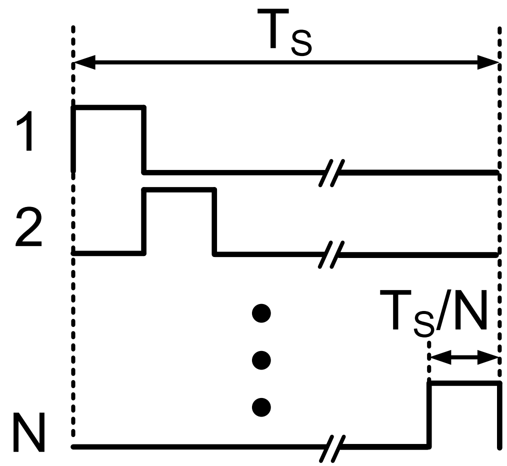


- More flexibility: clocked switches + R + C
  - Interference cancelling high CP1dB Notch filter
  - Self-Interference Cancelling Full-Duplex Rx

Notch Filter via Switched-Cap Network

- RLC model:



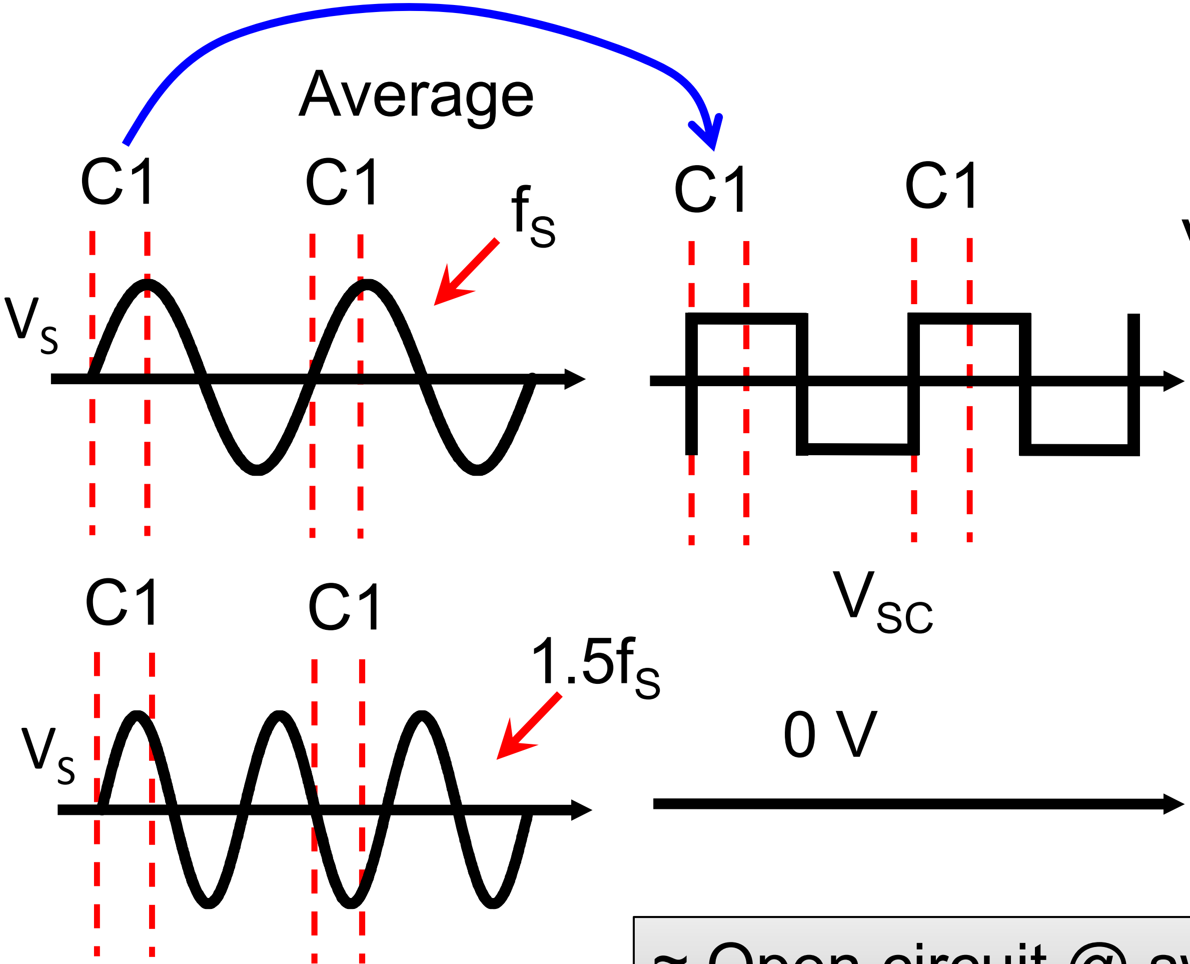


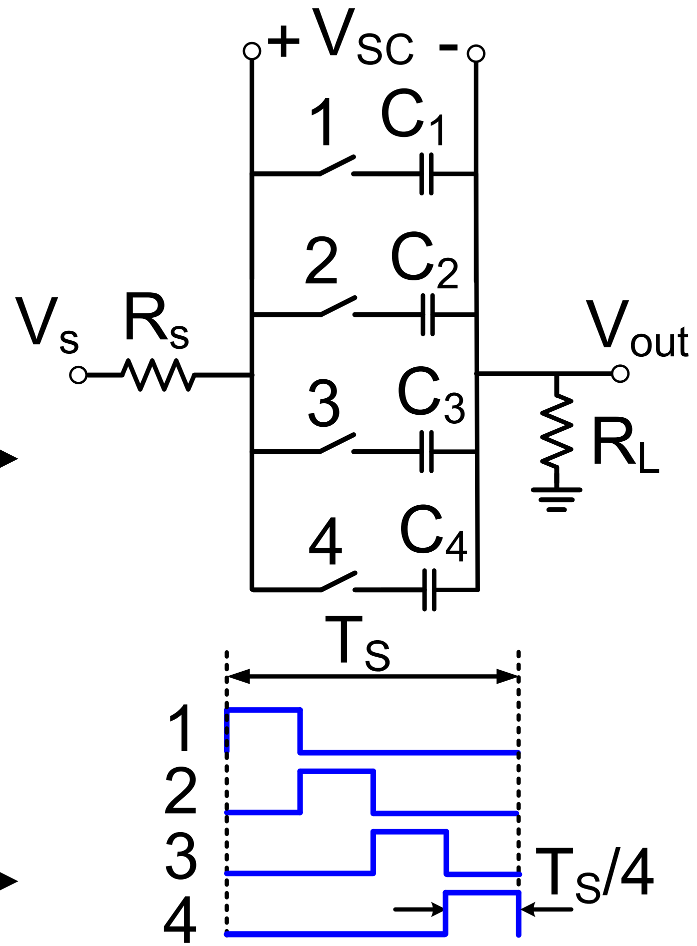
- R_P is preferably high

- Clock frequency
  ⇔ notch frequency

N-Path Notch Filter

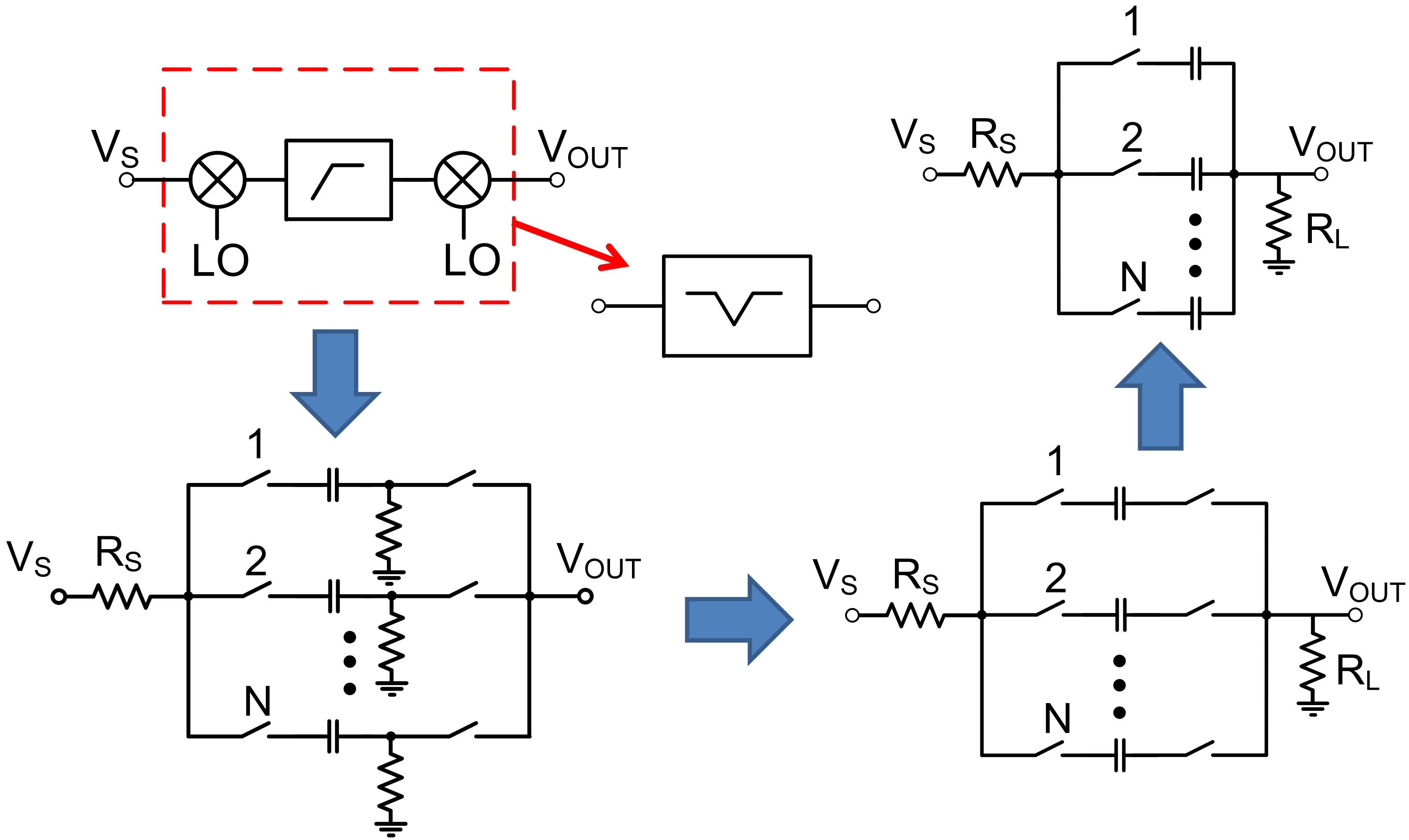
RC>> $T_S/4$



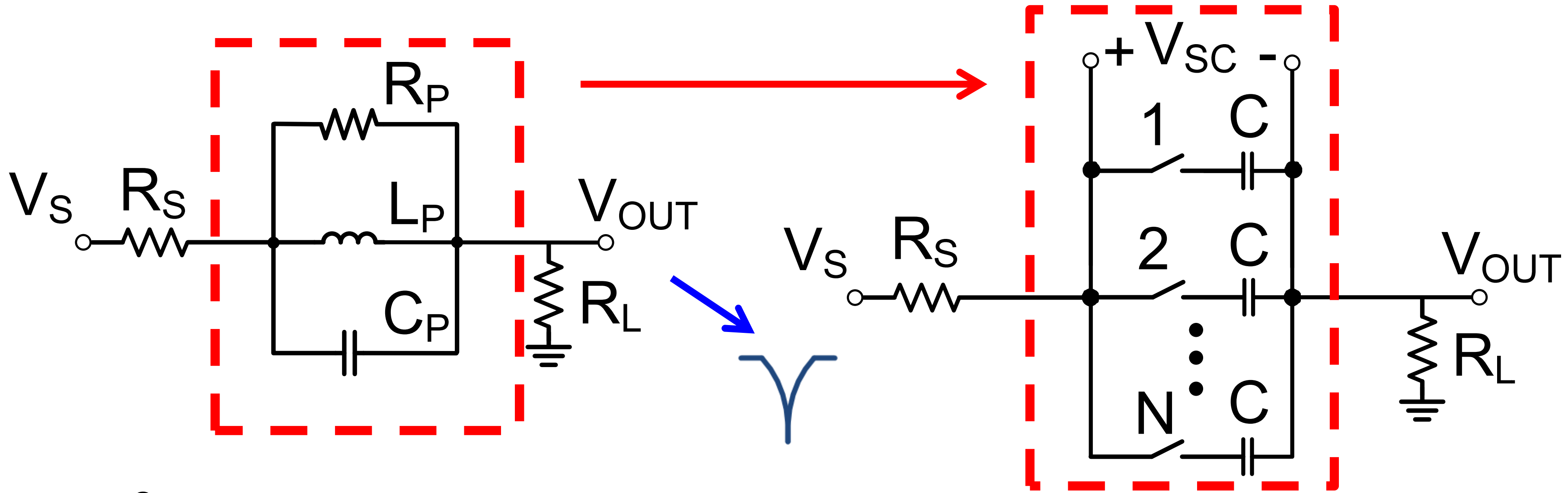


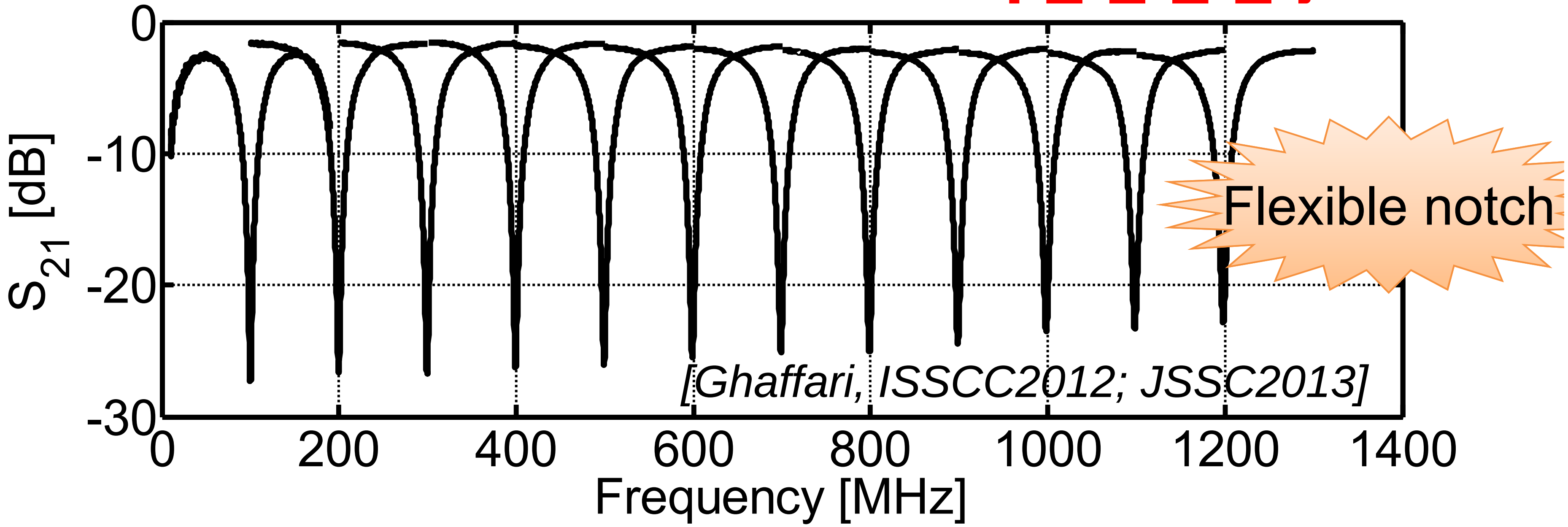
≈ Open circuit @ switching frequency
≈ Short circuit @ other frequencies

Notch= Up-Converted High-Pass Filter



8-path Notch-Filter



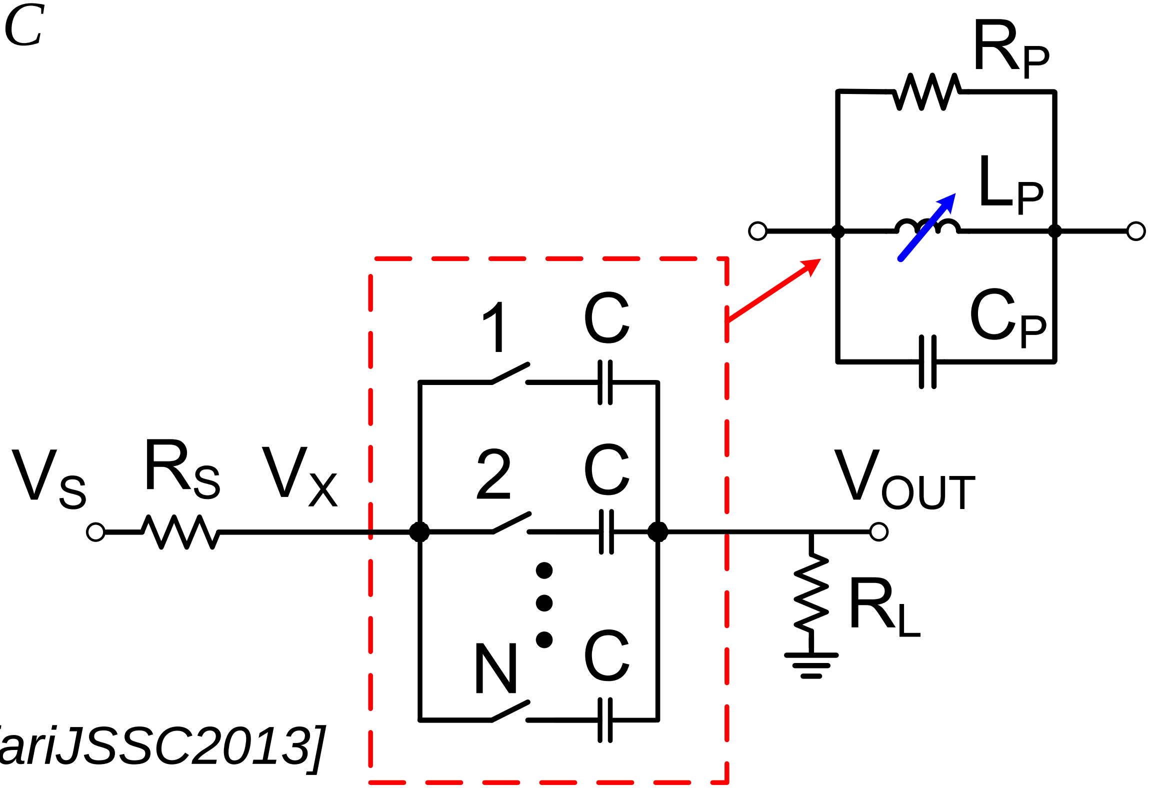


Approximate RLC Model

$$R_P = \frac{N^2(1-\cos(2\pi/N))}{2\pi^2 - N^2(1-\cos(2\pi/N))}(R_S + R_L)$$

$$C_P = \frac{N(R_P + R_S + R_L)}{2R_P}C$$

$$L_P = \frac{1}{(2\pi f_S)^2 C_P}$$



[GhaffariJSSC2013]

Benchmark

- [1] A. Bevilacqua et al., "A 0.13 um CMOS LNA with Integrated Balun and Notch Filter for 3-to-5 GHz UWB Receivers," IEEE ISSCC Dig. Tech. Papers, pp. 420–421, Feb. 2007

- [2] J. Y. Lin, H. K. Chiou, " Power –Constrained Third-Order Active Notch Filter Applied in IR-LNA for UWB Standards," IEEE Trans. Circuits Syst. II, vol. 58, no. 1, pp. 11-15, Jan. 2011.

Q-enhanced LC resonator embedded in an LNA

Comparison (I)

	Differential	Single-Ended	[1]	[2]
Technology	CMOS 65nm	CMOS 65nm	CMOS 0.13um	CMOS 0.18um
Active Area	$0.87mm^2$	$0.87mm^2$	$1.6mm^{2(*)}$	$0.51mm^{2(*)}$
Power	3.5mW-30mW	2mW-16mW	7.5mW	1.8mW
Max. Rejection	21dB	22dB	44dB	35.7dB
Rejection	**>18dB over 6MHz**	**>18dB @ over 6MHz**	>10dB over 20MHz	NA

(*) Notch Filter + LNA

5dB with -10dBm Blocker

Comparison (II)

	This Work Differential	This Work Sngl-ended	[1]	[2]
Gain	-1.4 to -2.8dB	-1.4 to -2.5dB	19.4dB(*)	14.7dB(*)
NF(dB)	**1.6-2.5dB**	**1.2-2.8dB**	3.5dB(*)	5.3dB(*)
P_{1dB}(dBm)	**6**	**2-6**	-9.4(*)	NA
IIP3(dBm)	**> +17**	**> +18**	-2.9(*)	-2.5(*)
LO Leakage (dBm)	< -60	<-75	-	-
Tuning Range	**0.1-1.2GHz**	**0.1-1.2GHz**	4.7-5.4GHz	5.4-6GHz

(*) Notch Filter + LNA

ISSCC '15 / JSSC Dec'15:
A Self-Interference Cancelling Receiver for In-Band Full-Duplex Wireless with Low Distortion under Cancellation of Strong TX Leakage

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IC-Design group, University of Twente, the Netherlands

ICO Integrated Circuit Design

UNIVERSITY OF TWENTE.

In-band full-duplex wireless

- TX and RX *simultaneously* at *same* frequency
- Why?
  - Up to 2x spectral efficiency

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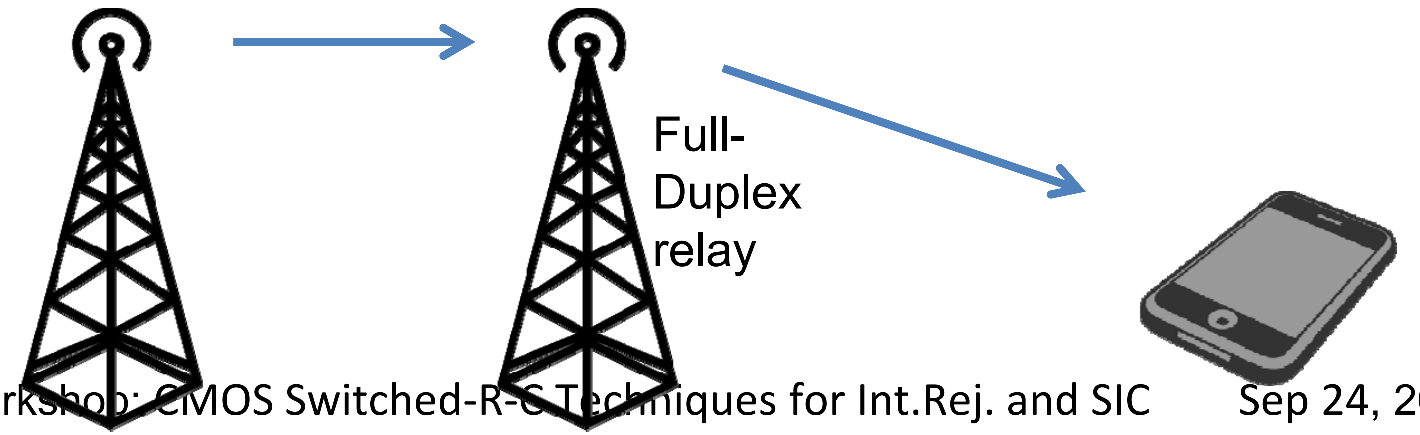
  - Simplified / flexible frequency planning
  - Reduced air interface delay (e.g. FD relaying)



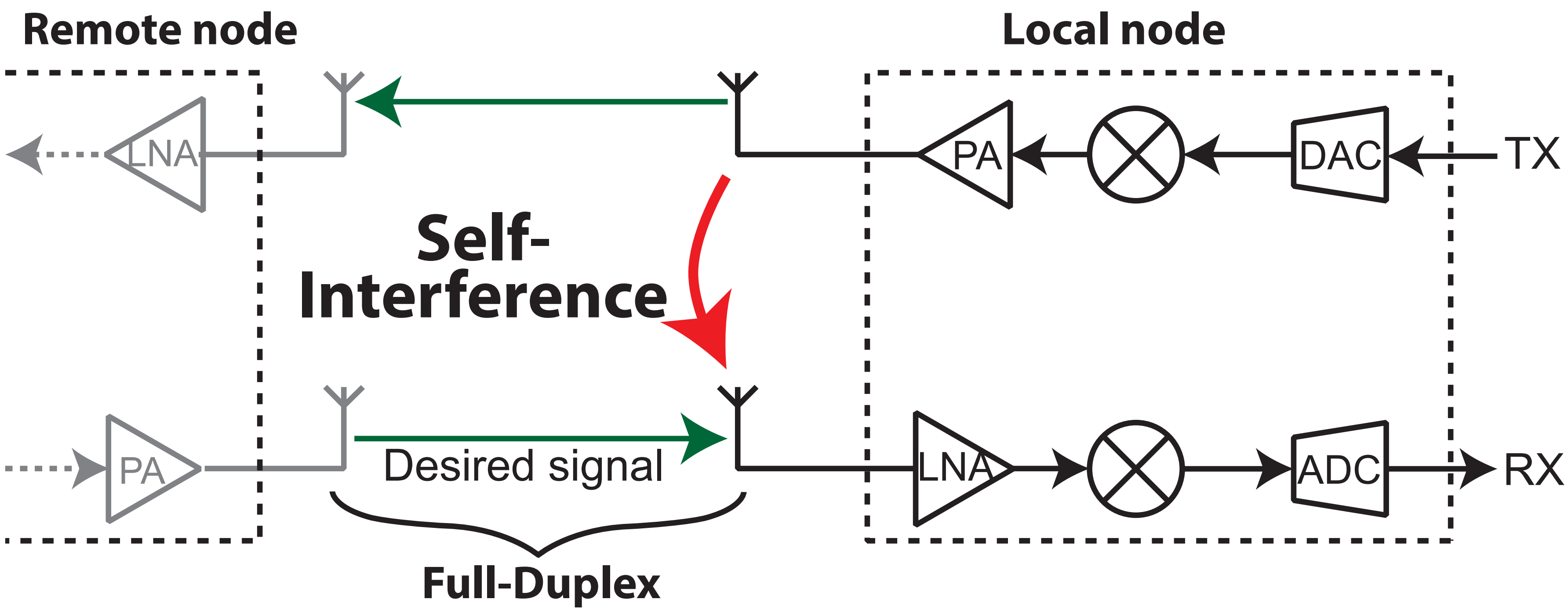
In-band full-duplex wireless

- TX and RX *simultaneously* at *same* frequency

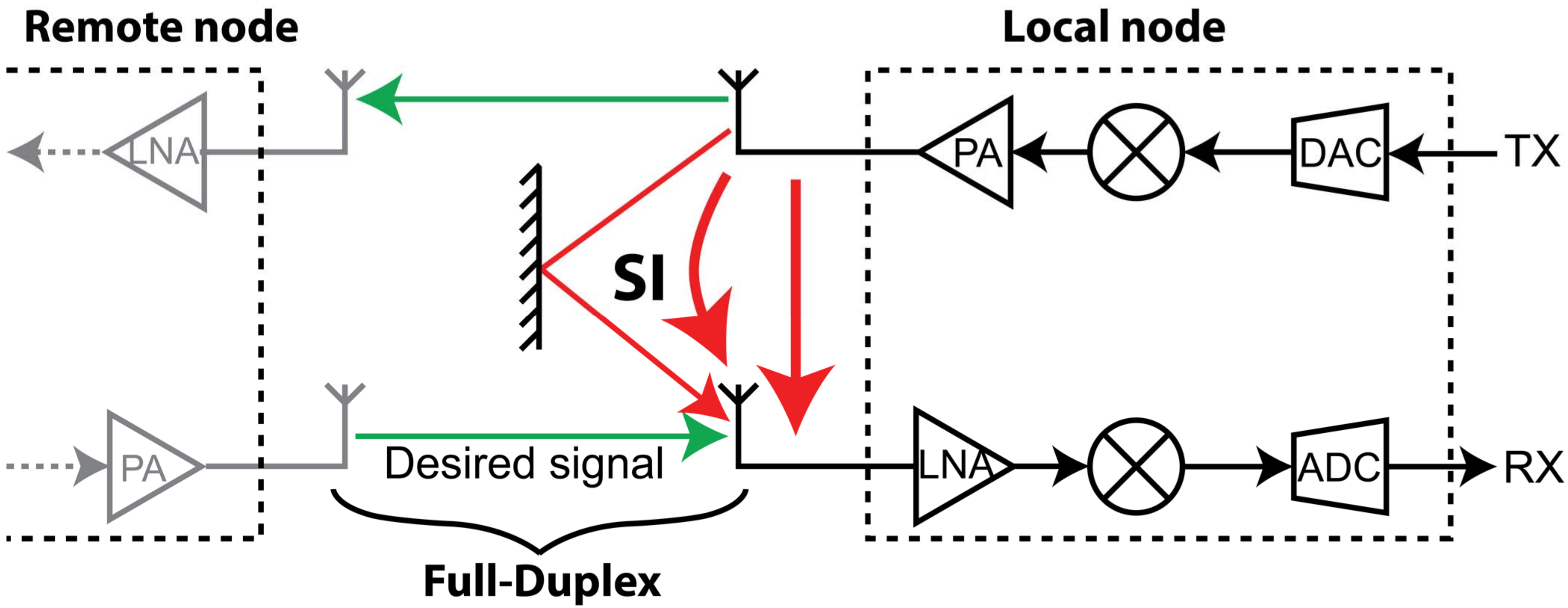
- Why?
  - Up to 2x spectral efficiency
  - Simplified / flexible frequency planning
  - Reduced air interface delay
  - Benefits / applications in higher layers
    - Simultaneous data & control
    - Reciprocal channel
    - …?

In-band full-duplex wireless

- Why not? (1)



Challenge: Self-interference (SI)



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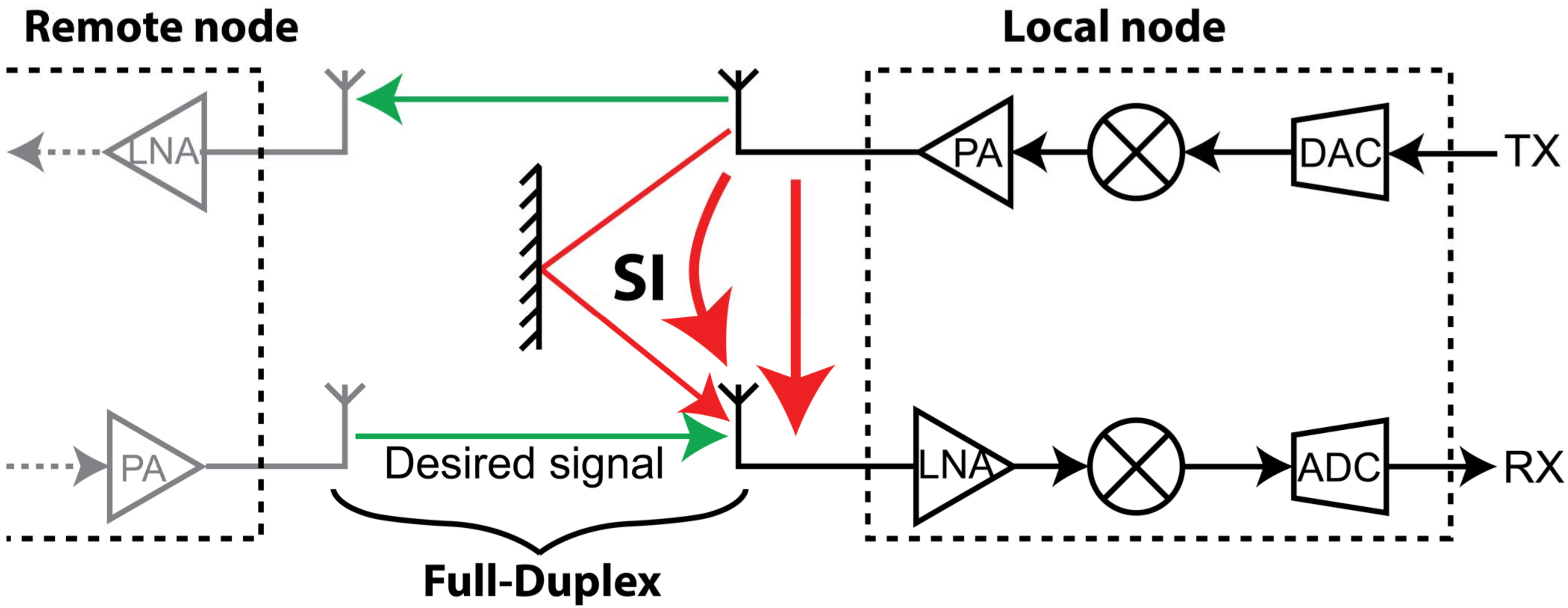
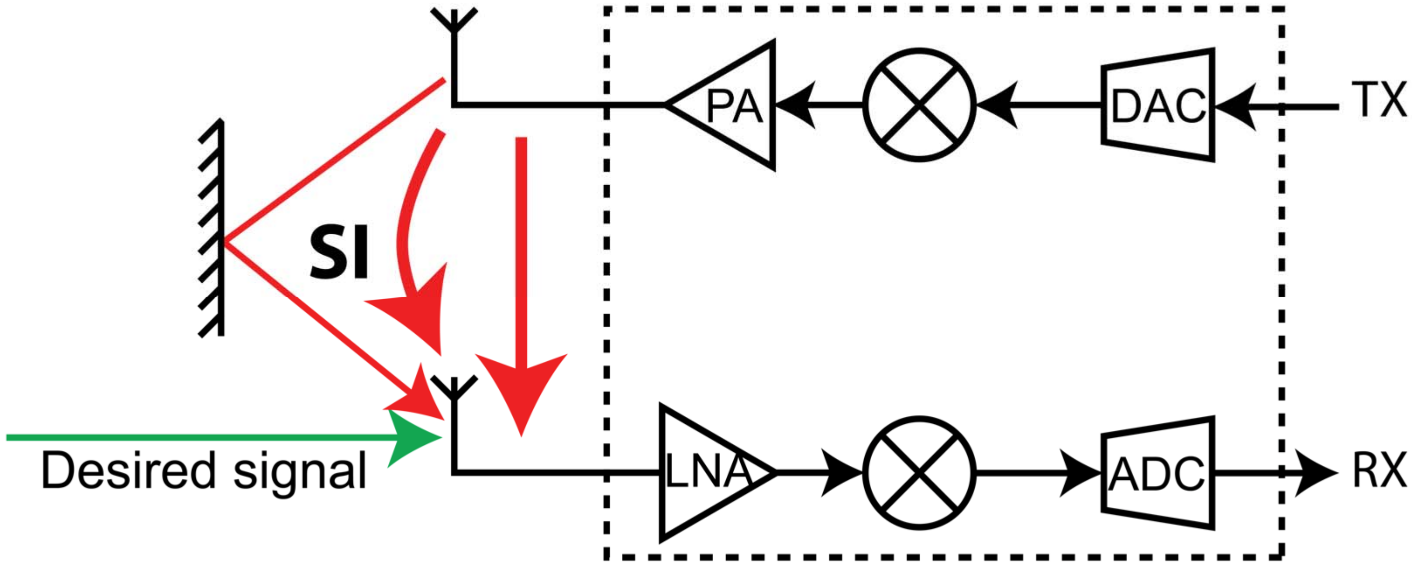


Short-range, relaxed low-power link:

16 MHz BW [WLAN], 10 dB NF → -90 dBm noise floor

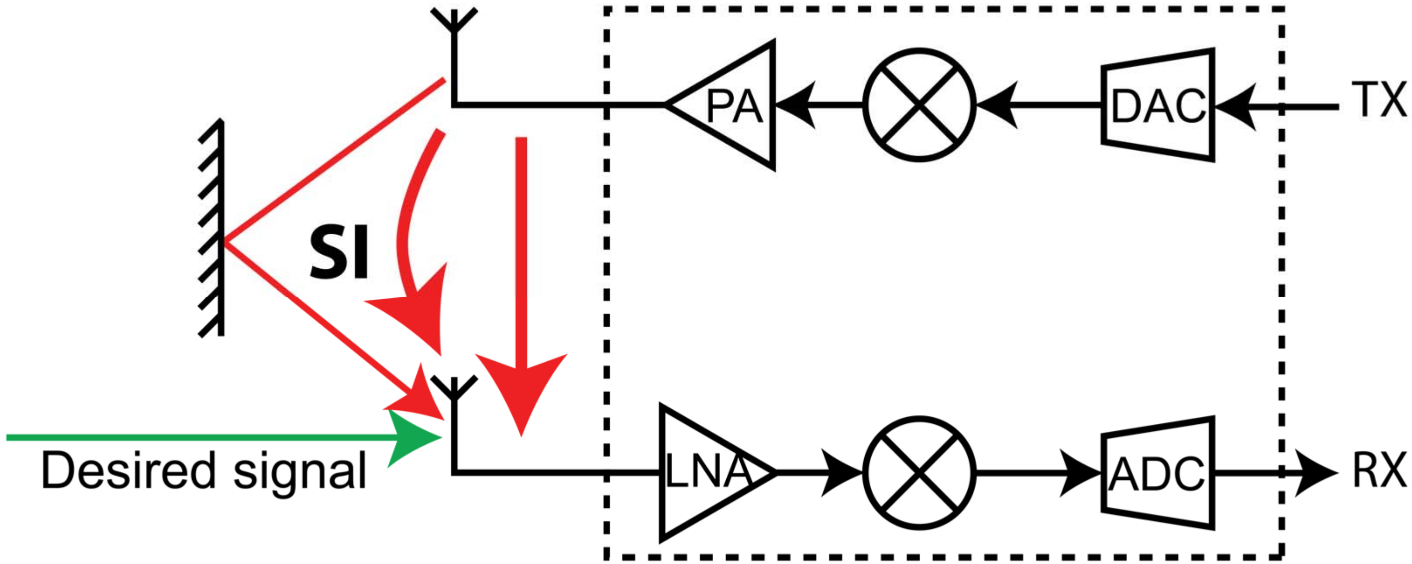
0 dBm TX power: <u>~90 dB total SI rejection desired</u>

Self-interference Contributions



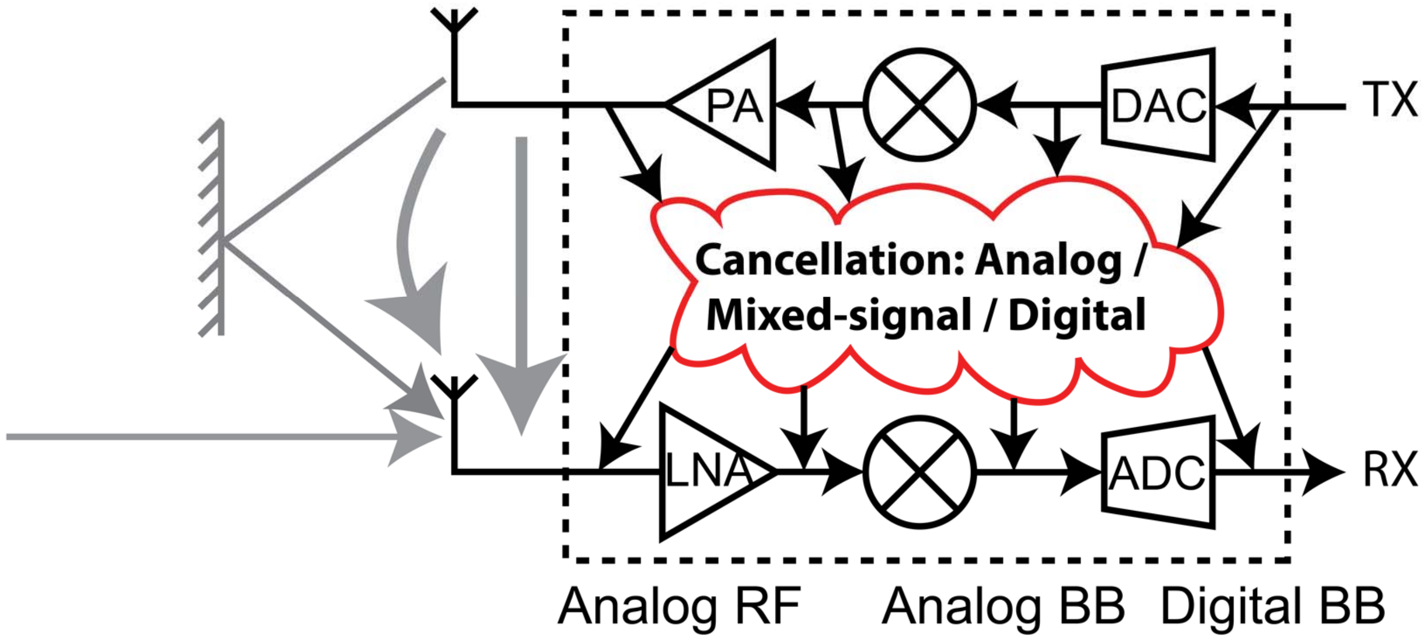
Focus on <u>one full-duplex node</u>
and its SI-rejection

Self-Interference Cancellation (SIC



Handheld device → varying antenna isolation
→ e.g. 20 dB worst-case *isolation*
→ 90 – 20 = 70 dB *cancellation* required

Self-Interference Cancellation



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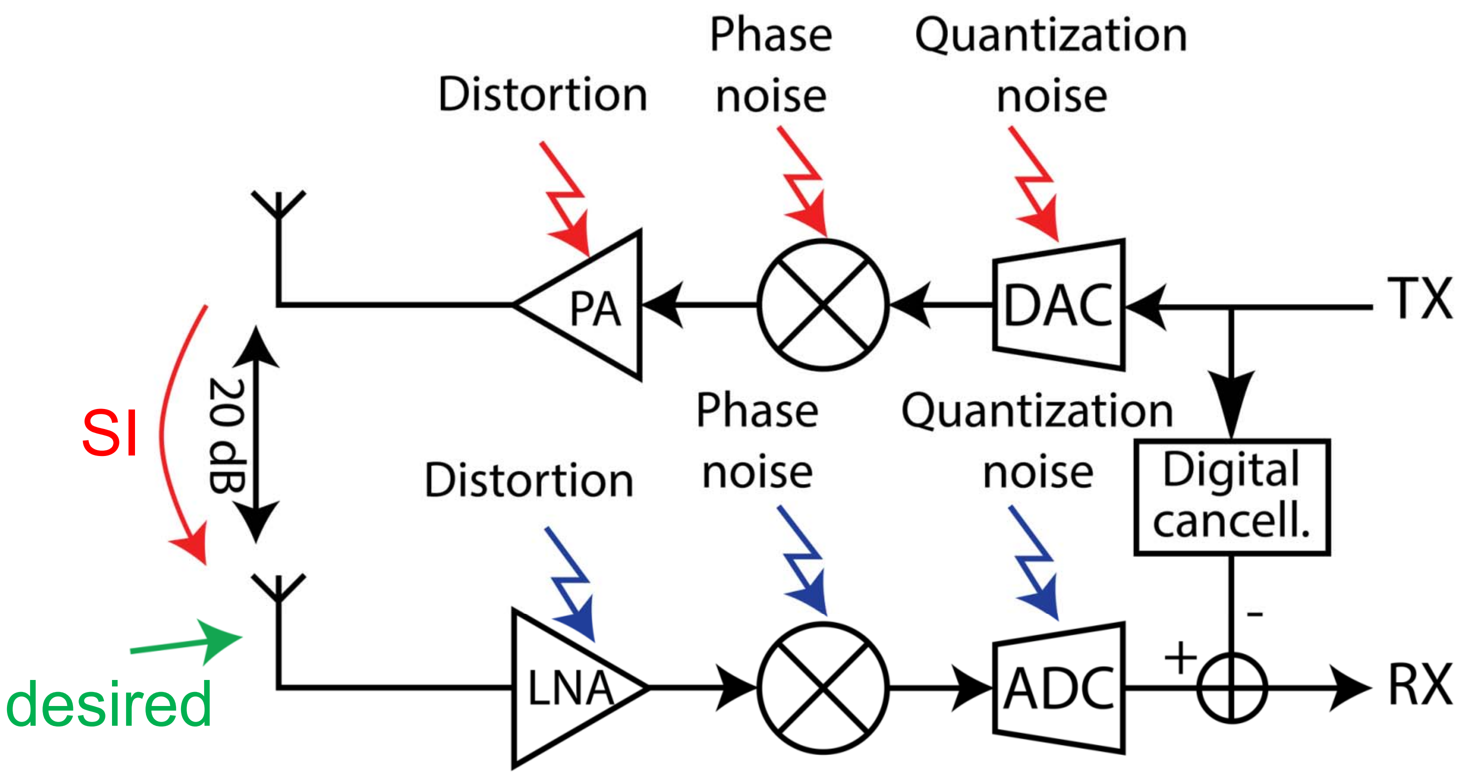
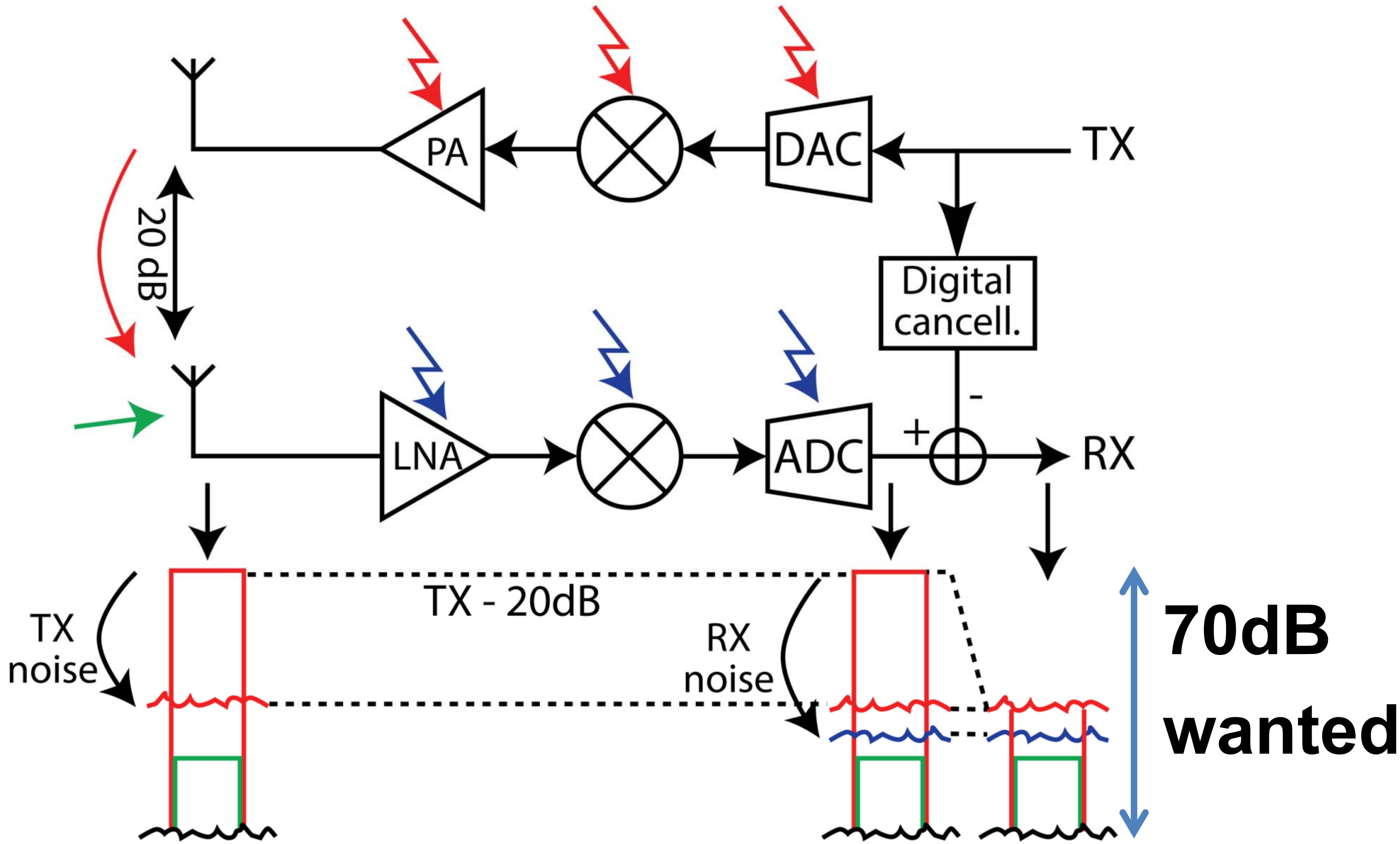
Digital-only SI-Cancellation



Deterministic components → cancel in digital

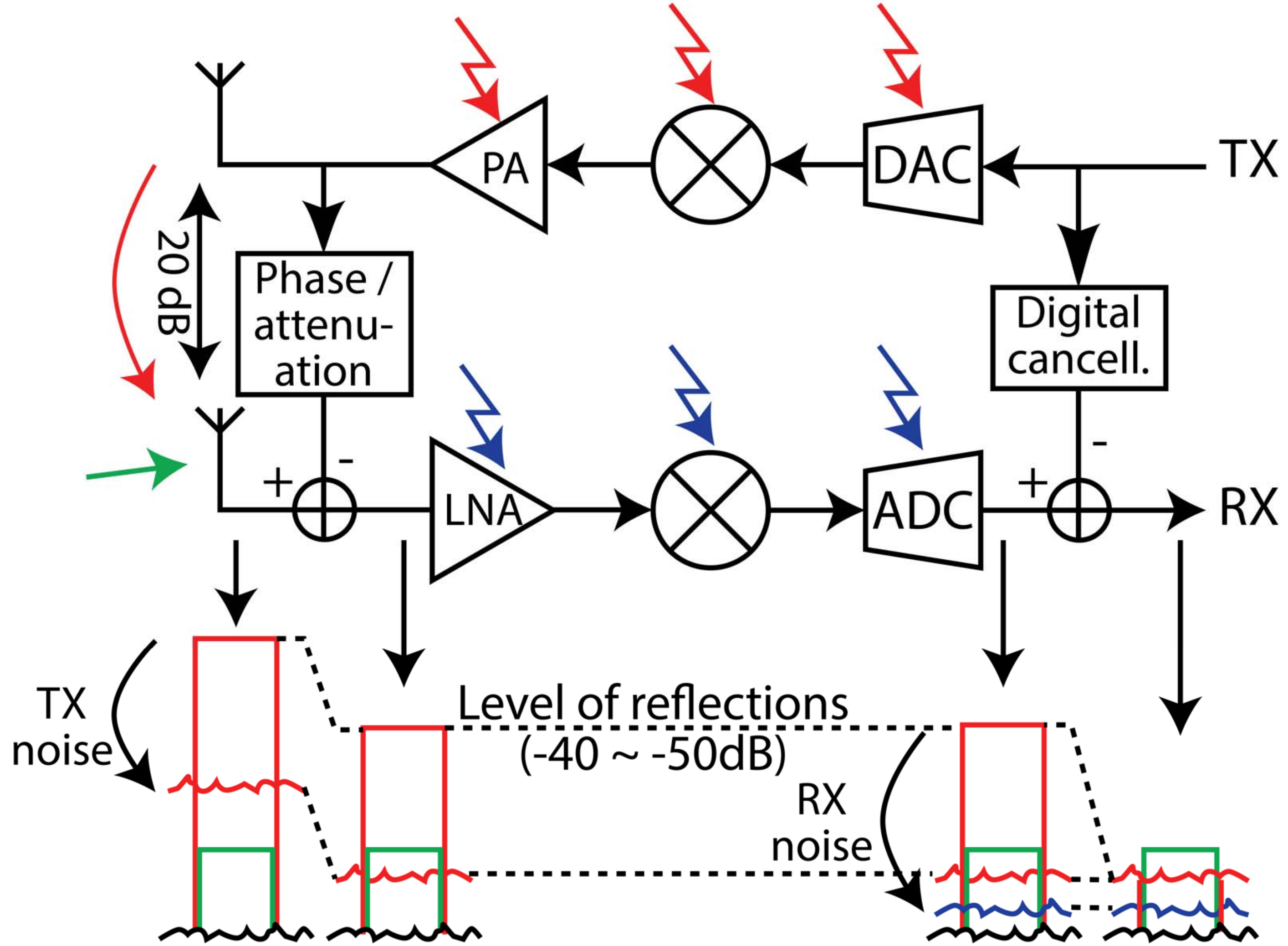
Noisy components must be 90dB down before digital!!

Digital-only SI-Cancellation



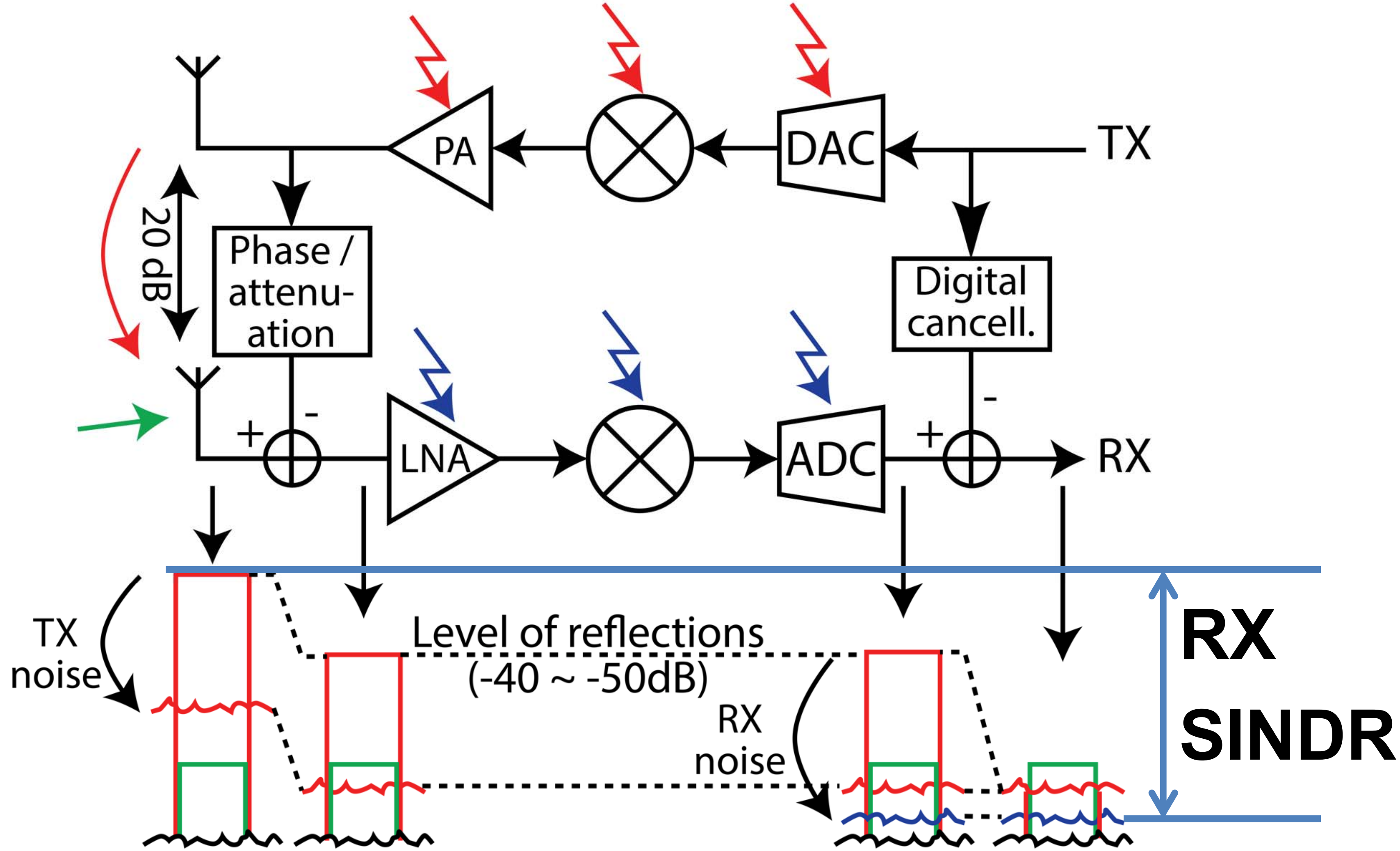
70dB TX EVM & RX dynamic range required

RF + digital SI-Cancellation



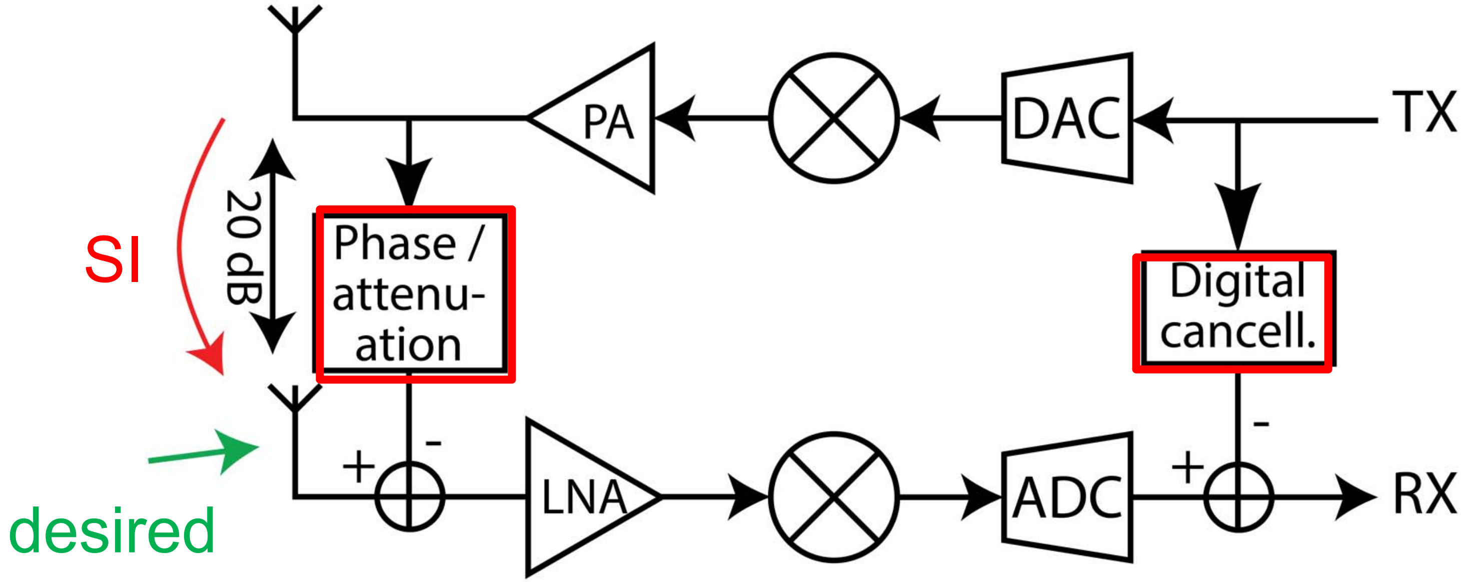
40-50 dB TX EVM & RX dynamic range required

RF + Digital SI-Cancellation

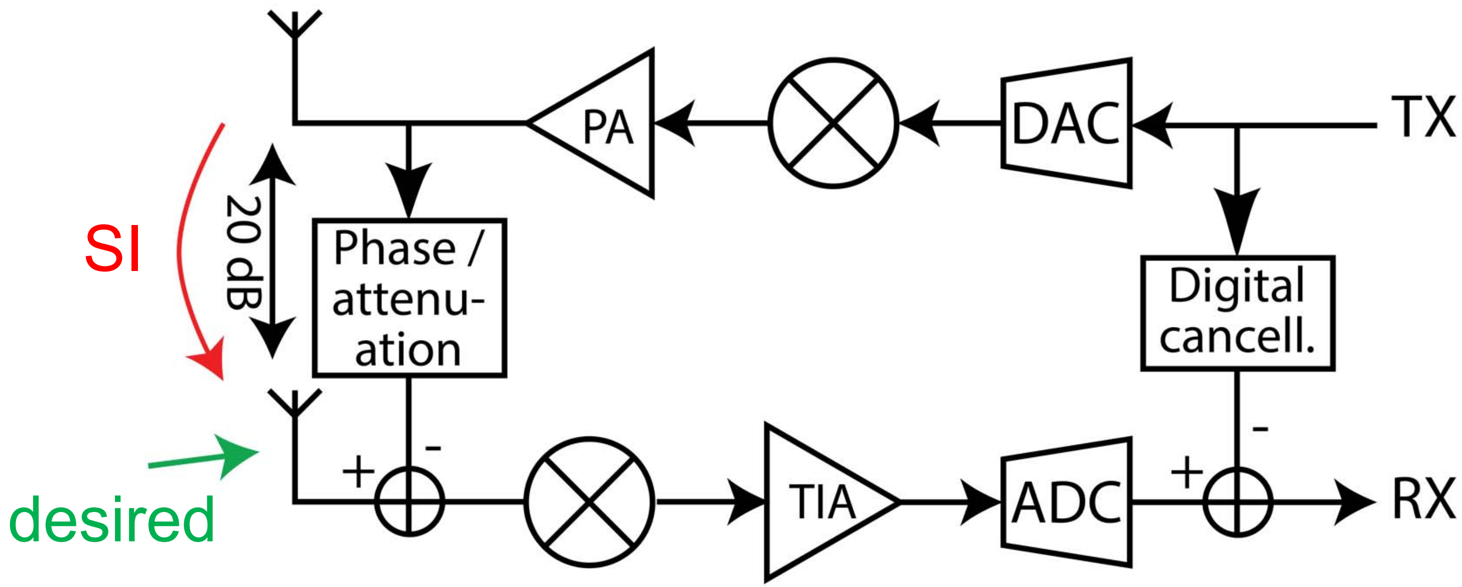


Self-interference-to-Noise-and-Distortion ratio

RF + Digital SI-Cancellation

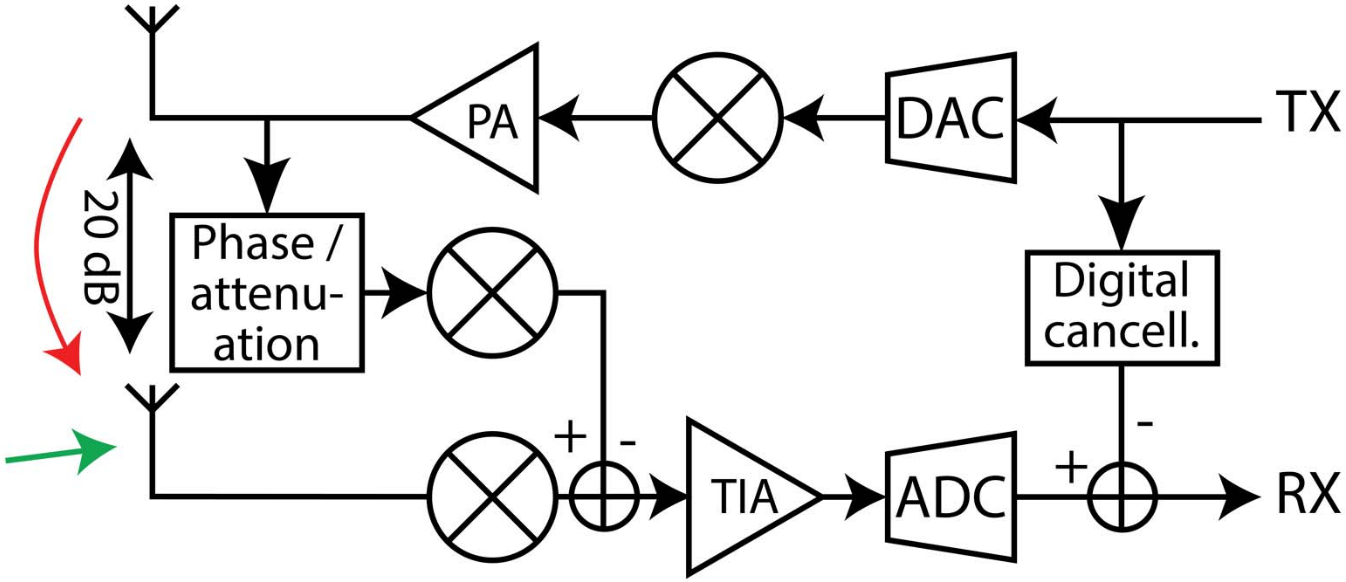


RF + digital SI-Cancellation



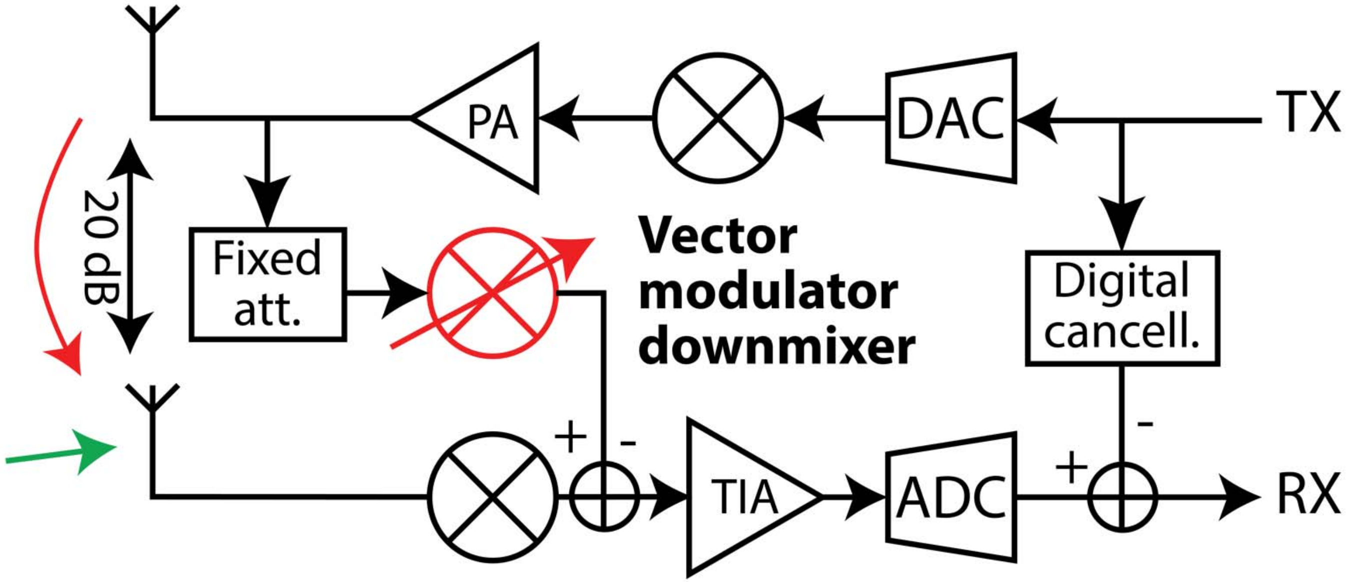
Mixer-first architecture for good linearity

Cross-domain cancellation



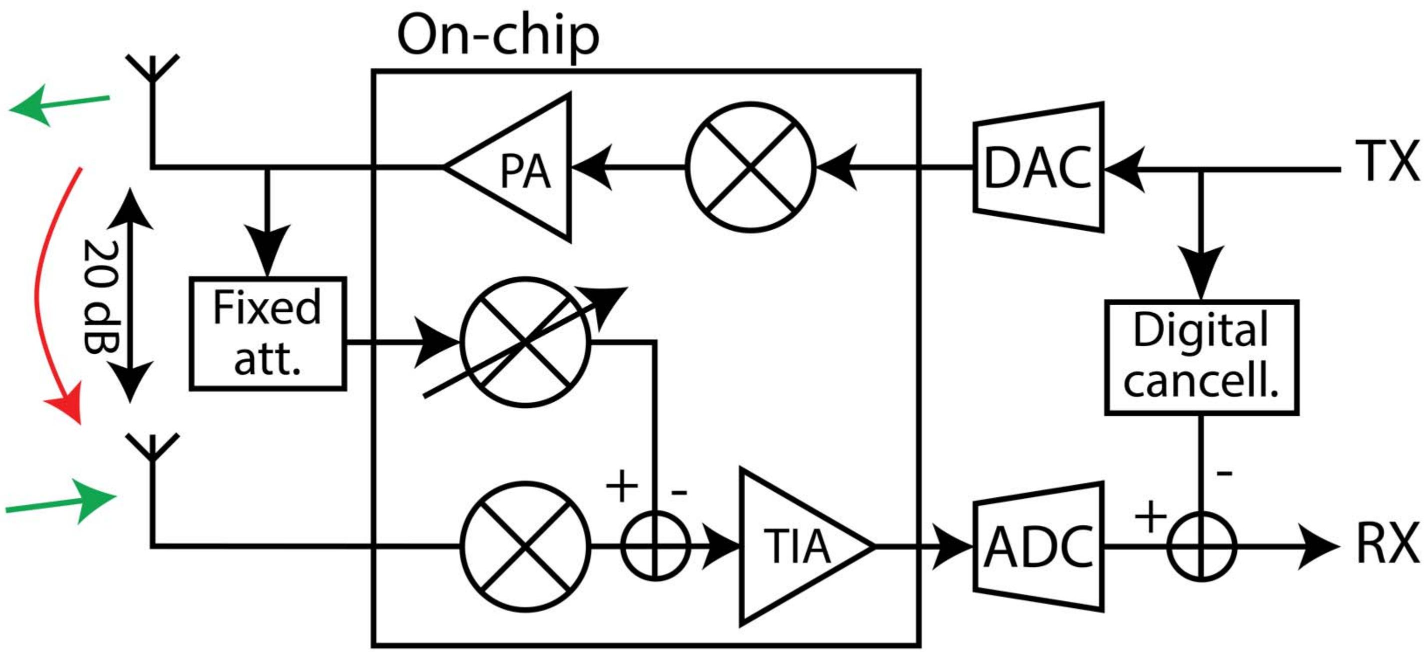
Cancellation TX RF → RX analog BB

Cross-domain cancellation



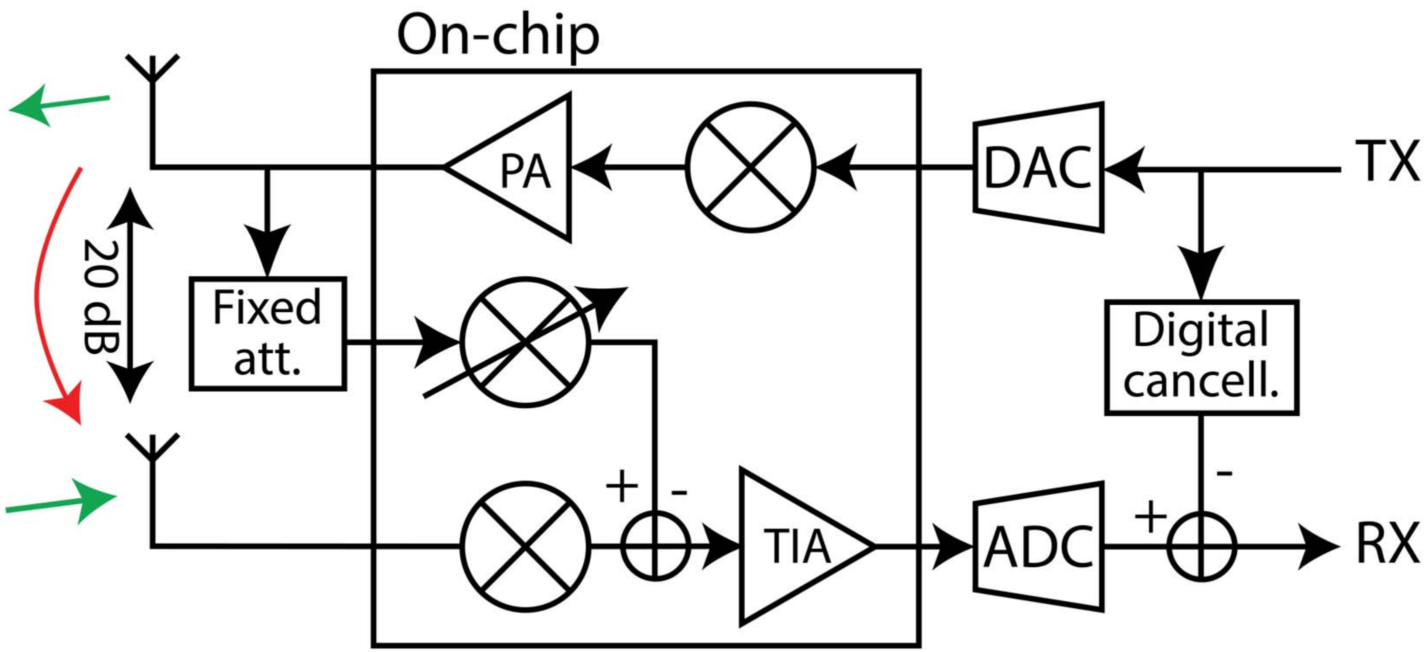
Combine phase, attenuation & downmixing

Prototype front-end



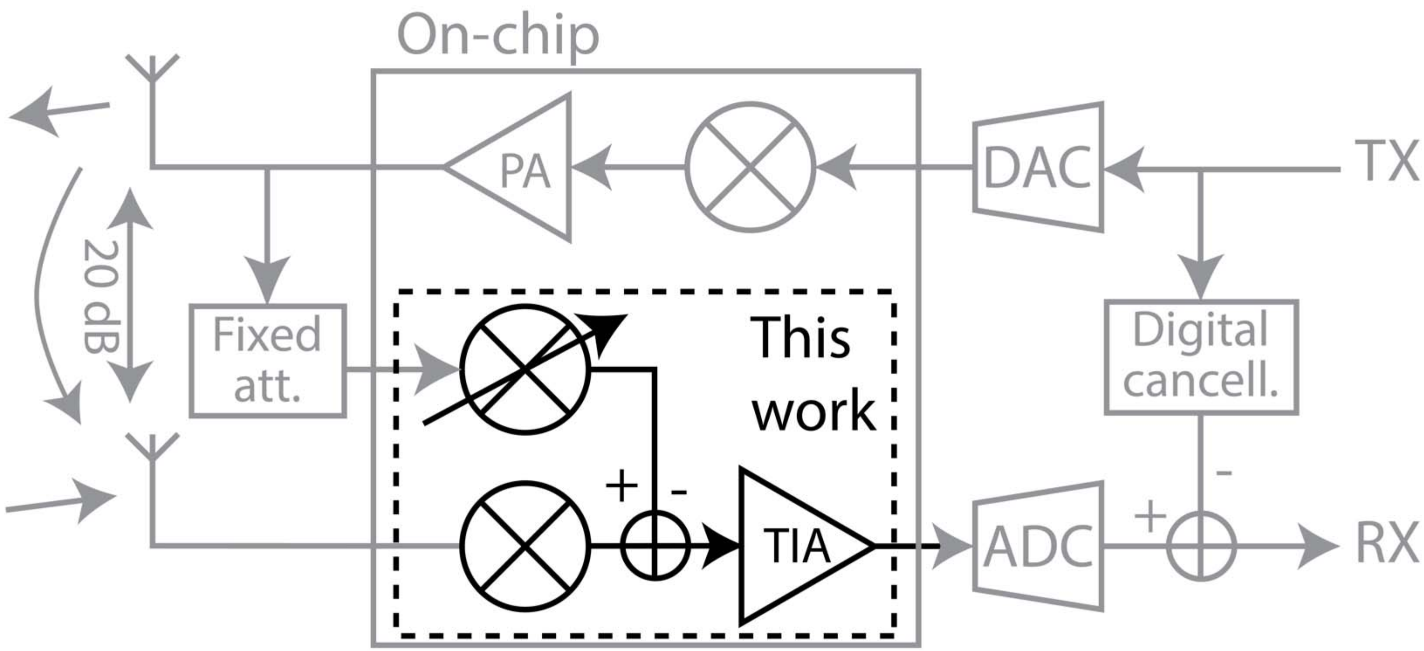
Short-range, low-power full-duplex
High integration potential

Prototype front-end

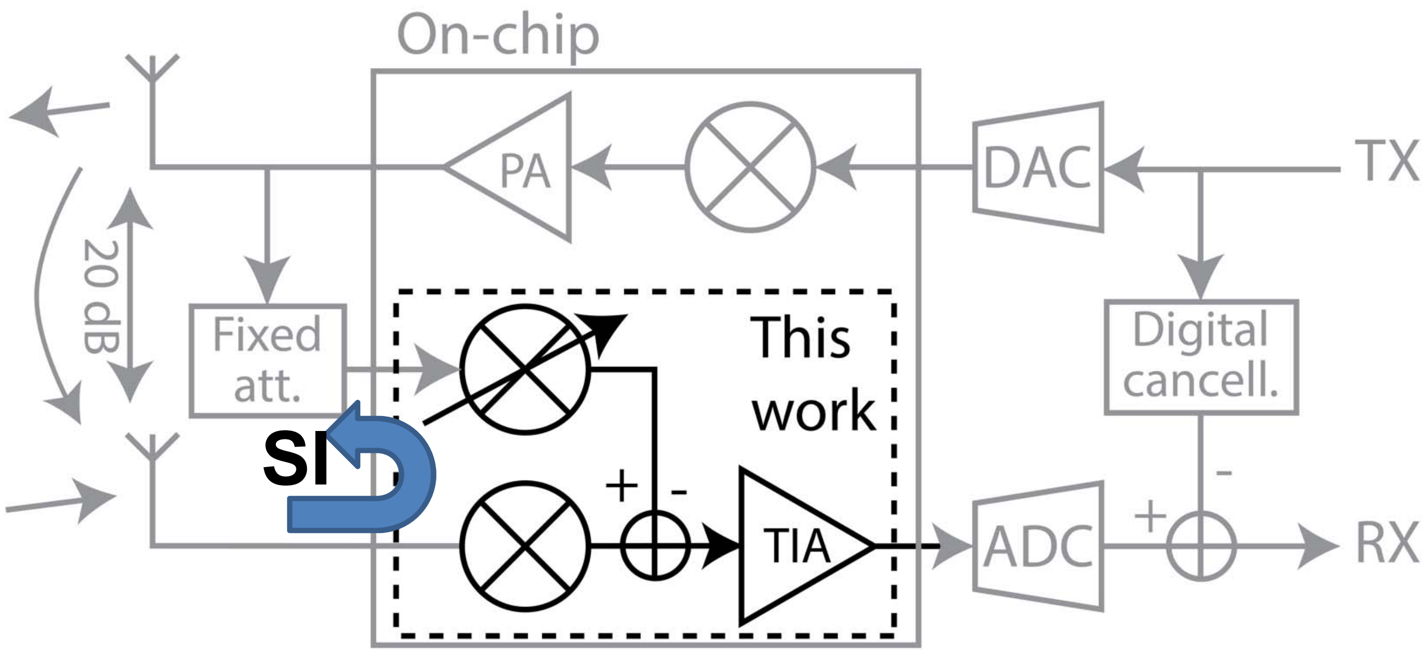


- VM → robust cancellation for changing near-field
- Attenuator sets VM range to worst-case SI

Prototype front-end



Prototype front-end

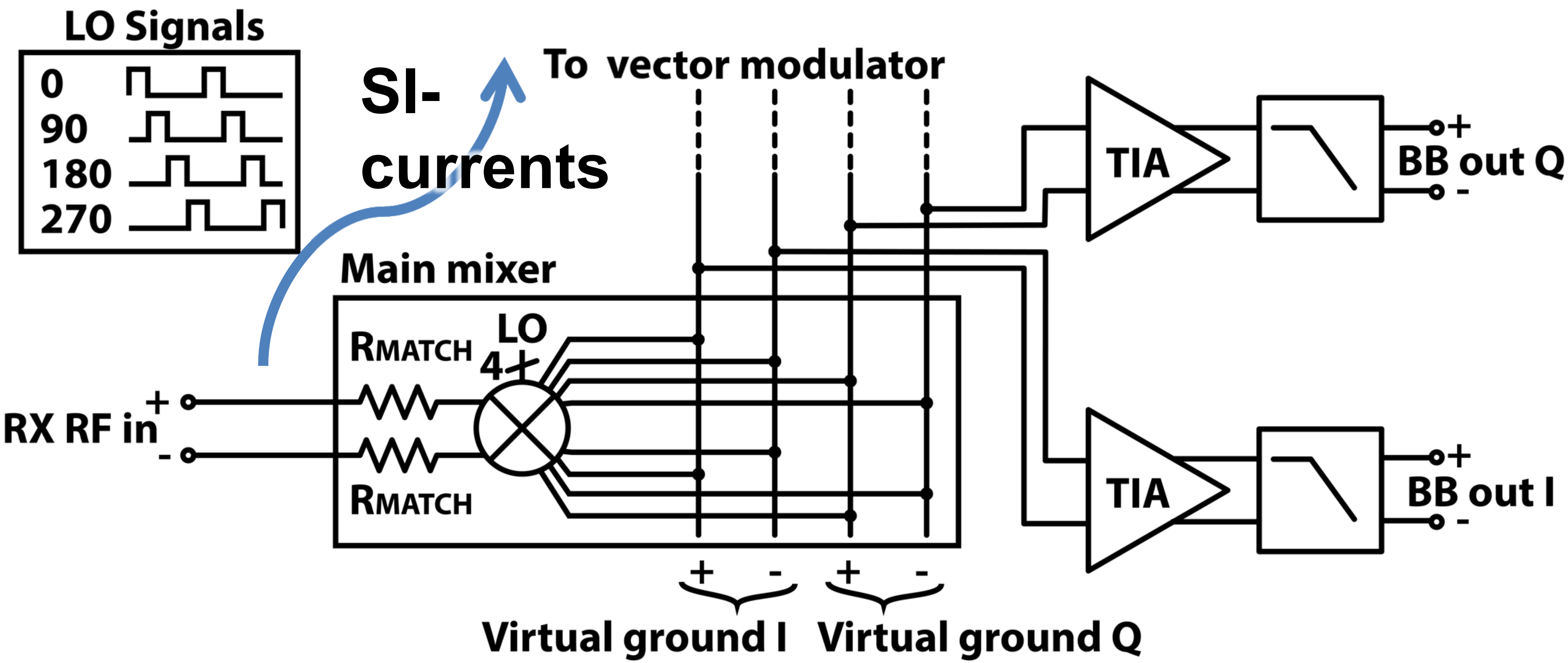


Mixers process full SI power:

Linearity crucial for high SINDR → <u>Passive mixers</u>

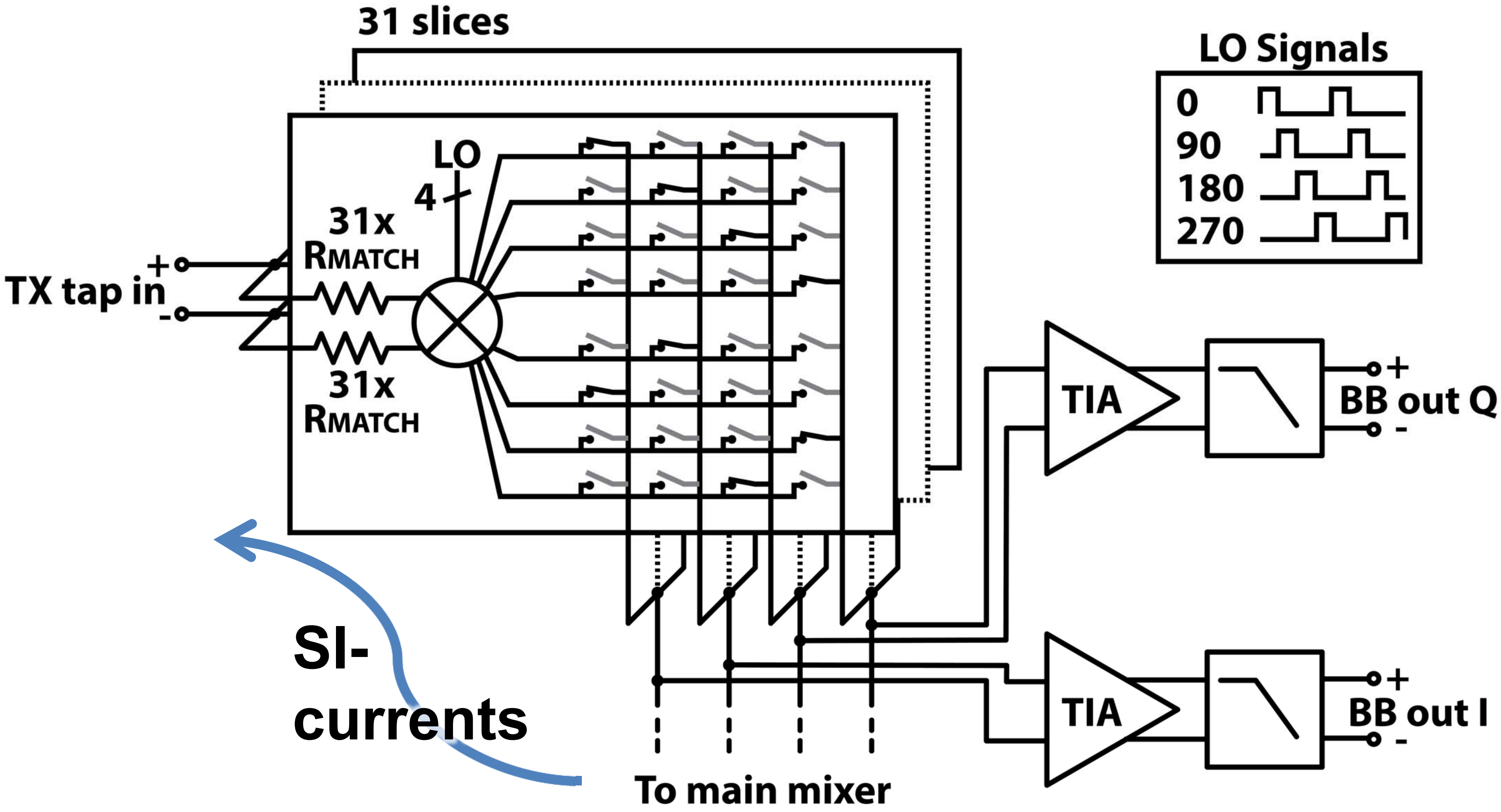
TIA and ADC after cancellation: relaxed

Main RX



Switched resistor to virtual ground

Vector modulator



SI-currents diverted through passive networks

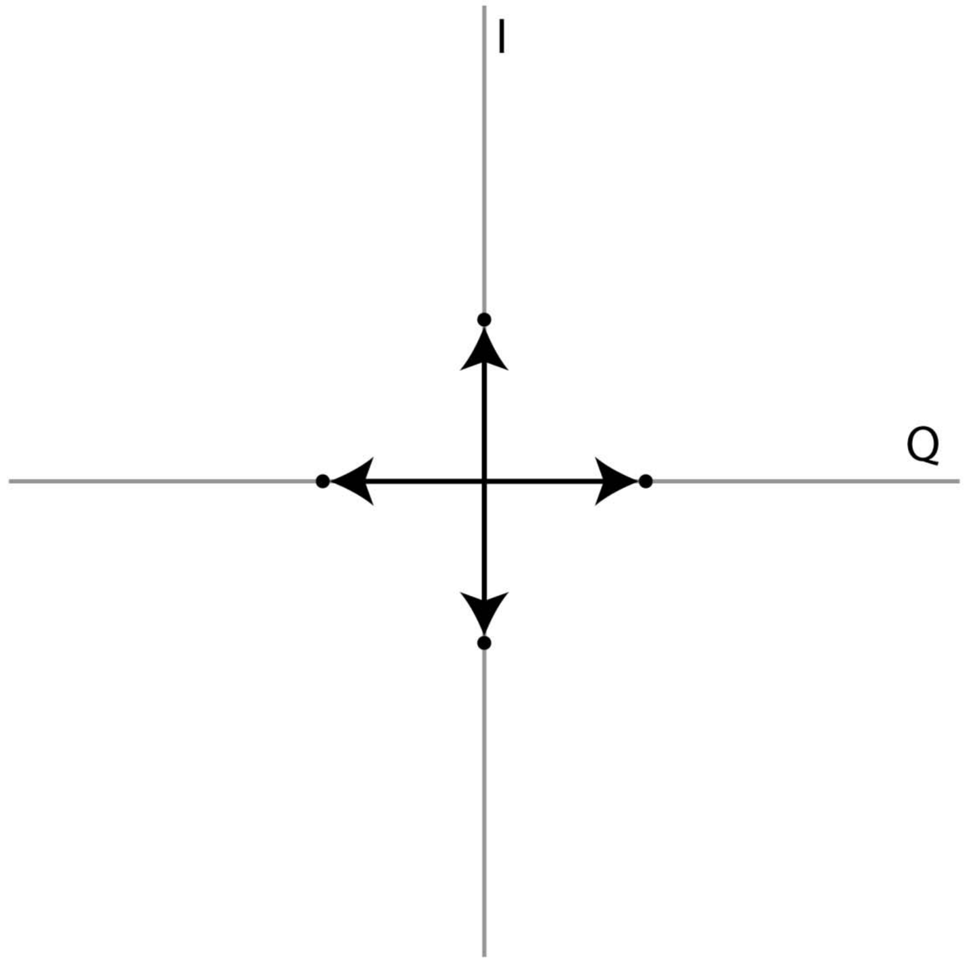
Vector modulator

- VM = sliced main mixer + static phase rotator

- Principle:

1 slice:

- 2x2 grid
- 4 points (I / Q)



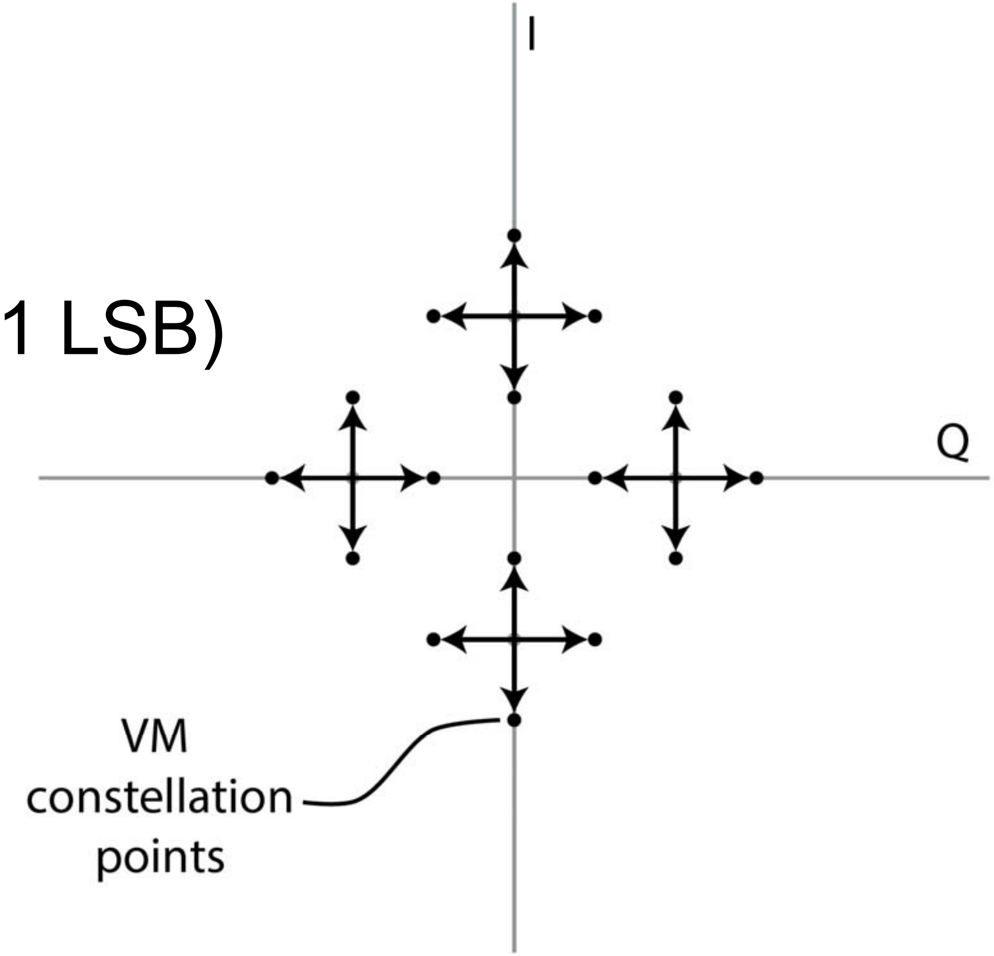
Vector modulator

- VM = sliced main mixer + static phase rotator

- Principle:

3 slices: (2 MSB + 1 LSB)
- 4x4 grid
- 16 points

[Soer, ISSCC'14]
(sliced Gm-mixer
instead of sliced-R)



Vector modulator

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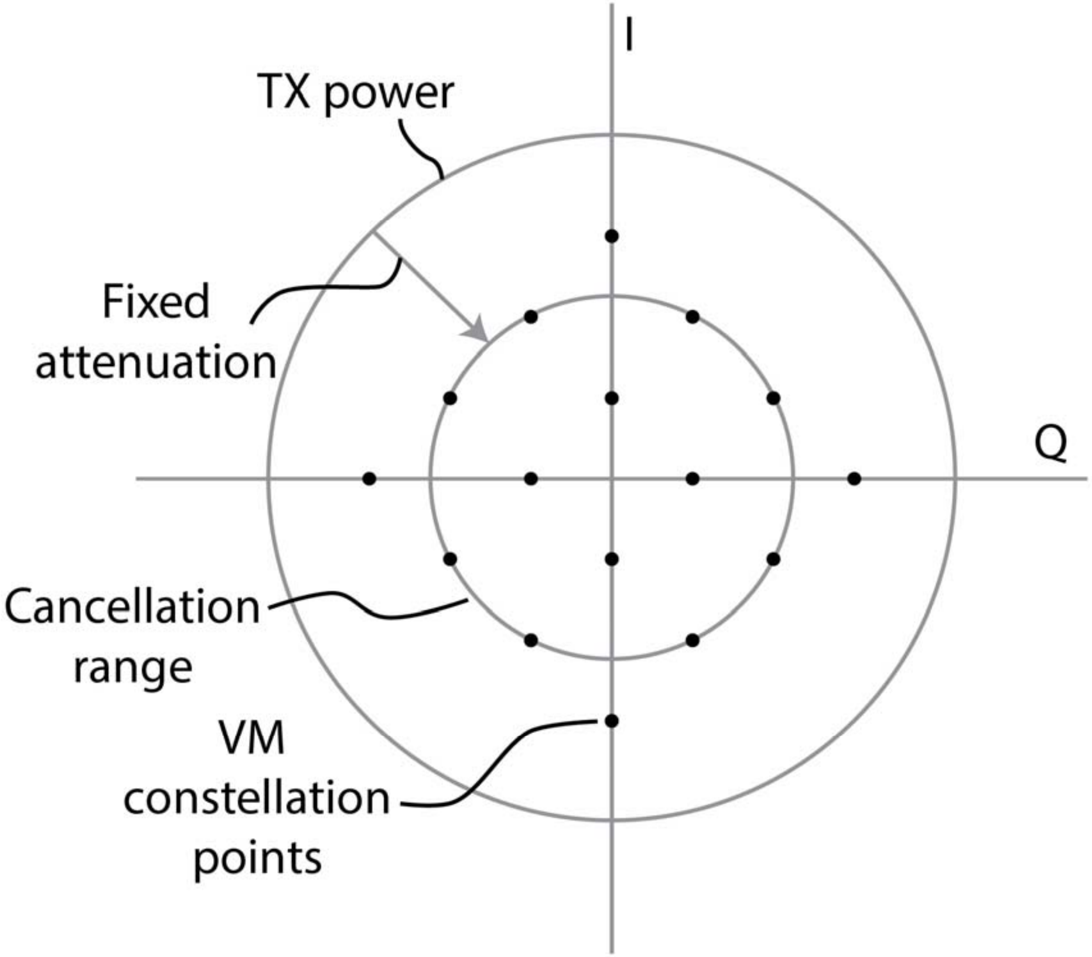

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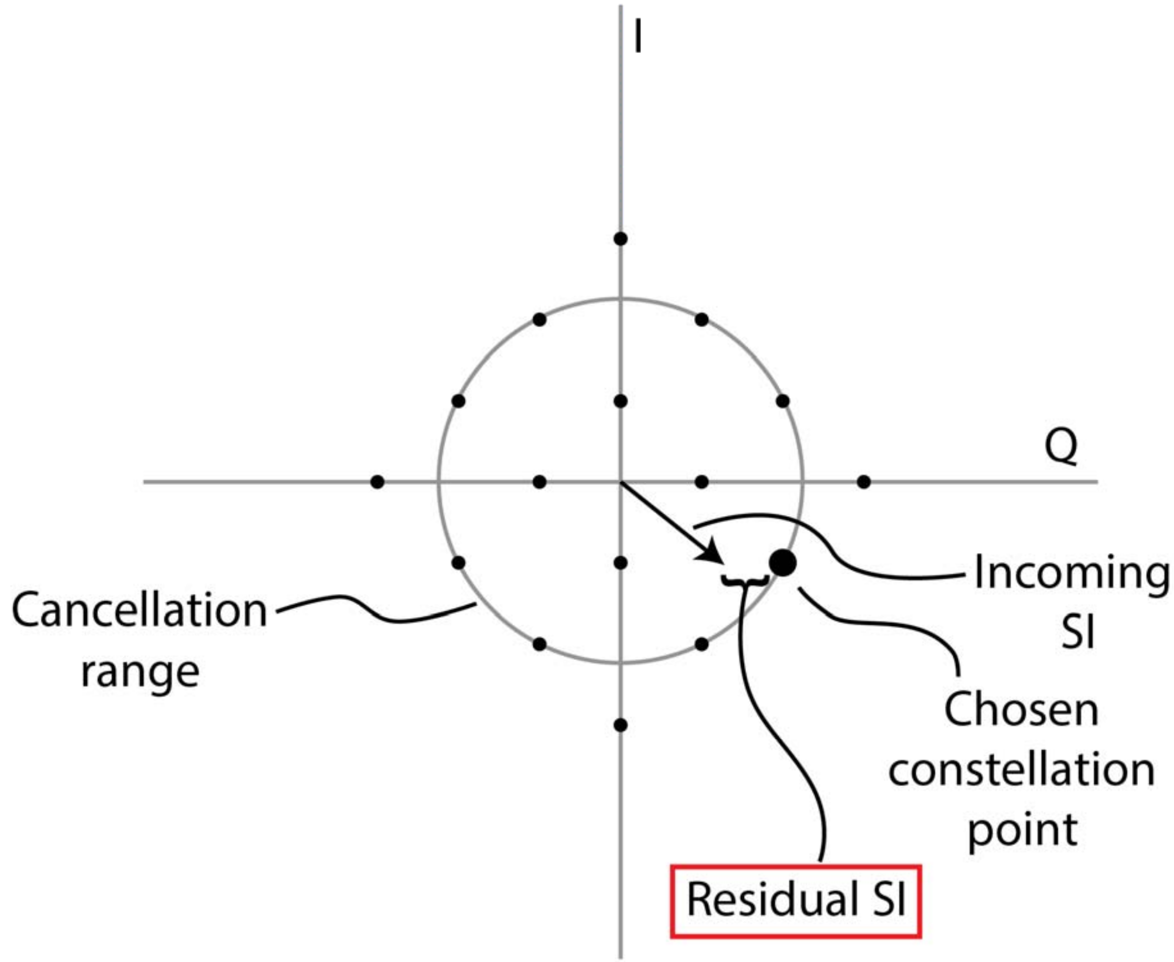


Vector modulator

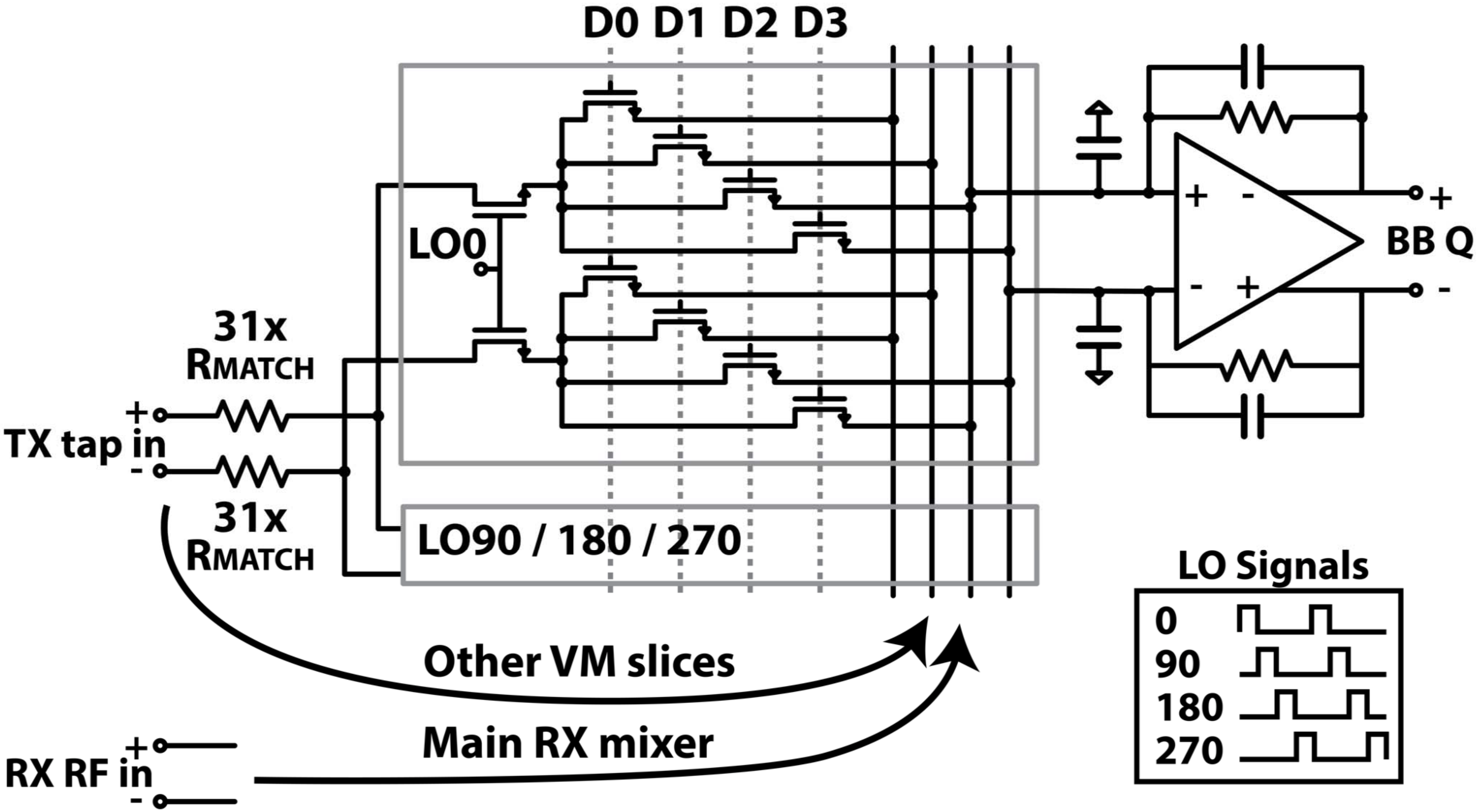
- VM = sliced main mixer + static phase rotator

31 slices: ("5 bits")

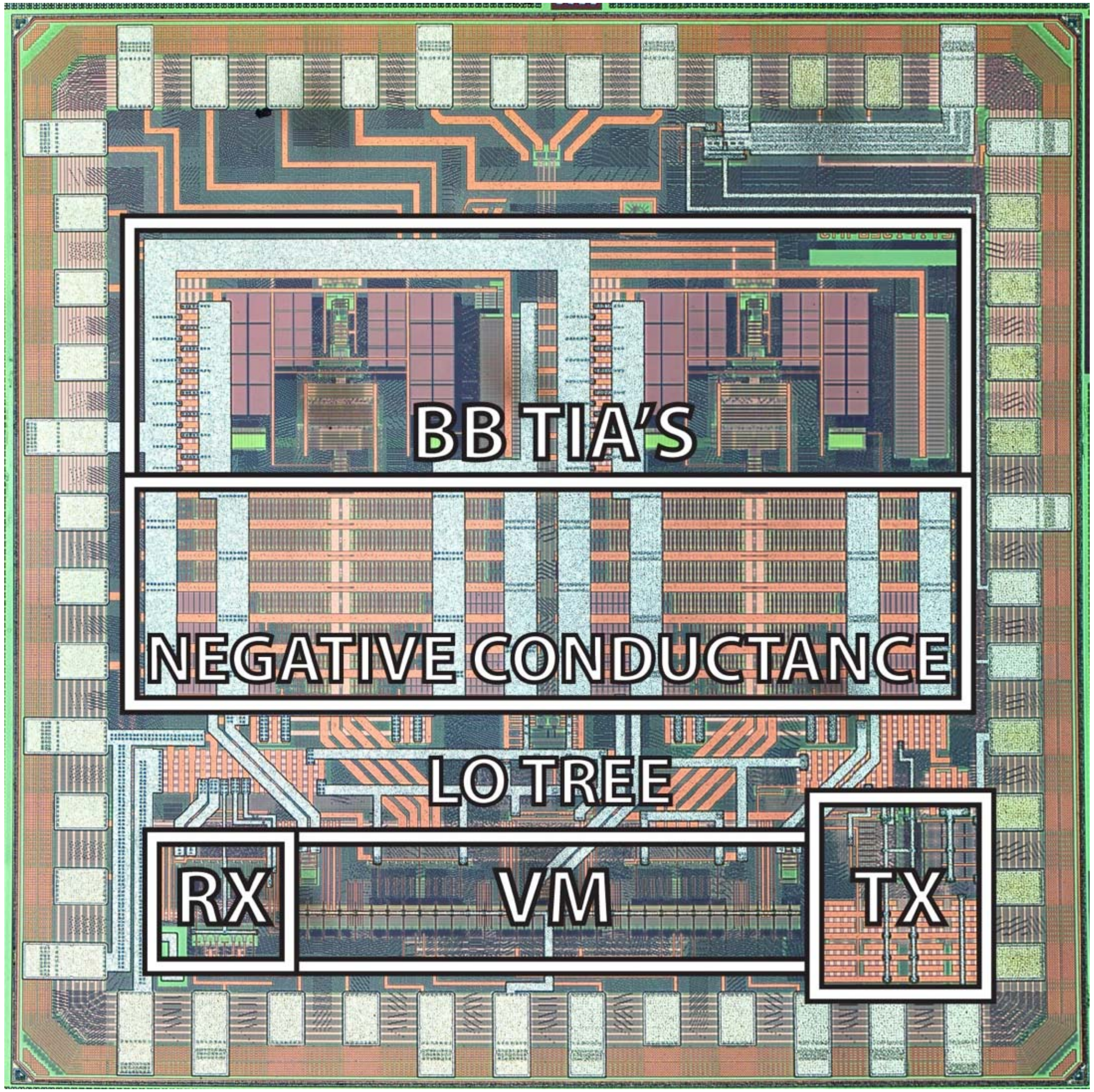
- 32x32 grid
- 1024 points

→ 28.5 dB worst-case cancellation

Single VM slice



Chip photograph



65nm CMOS

1.2V supply

1.4x1.4mm

Measured: Cancellation

- 20 tones in 16.25 MHz BW @ 2.5 GHz (WLAN-like)
- Emulated SI channel: arbitrary phase & amplitude
- On-chip VM finds best cancellation point
  - Search algorithm: power minimization

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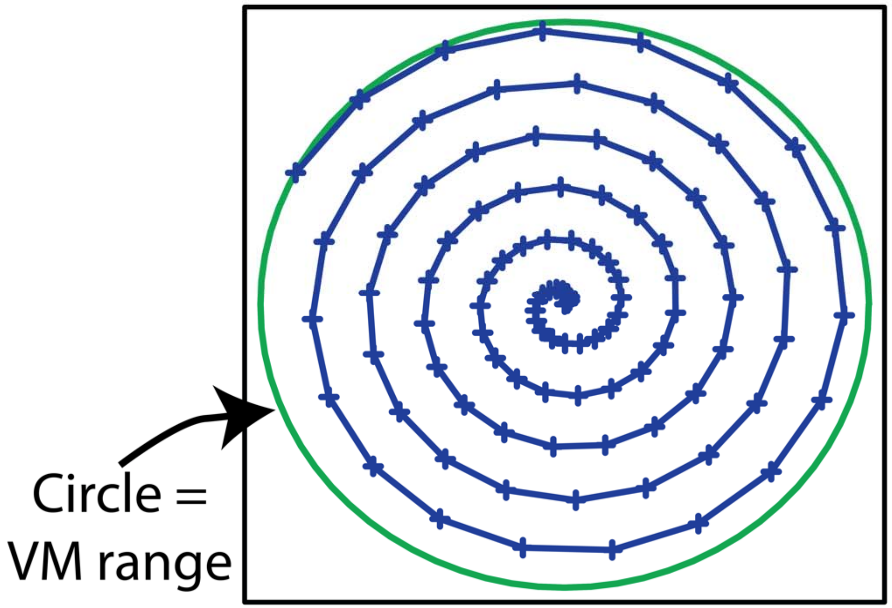
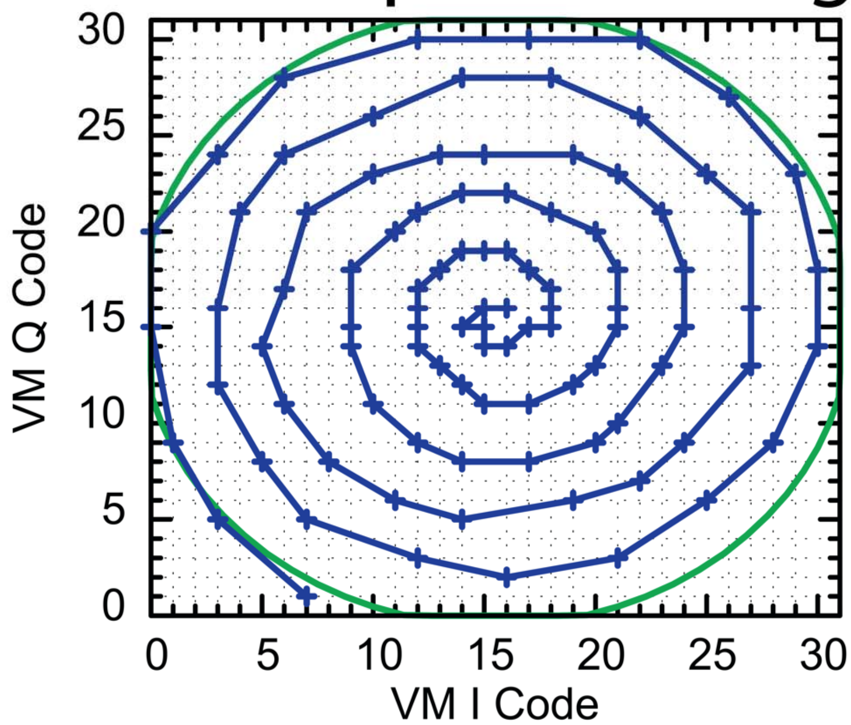
Emulated SI-channel



>100 phase/amplitude points

On-chip VM setting



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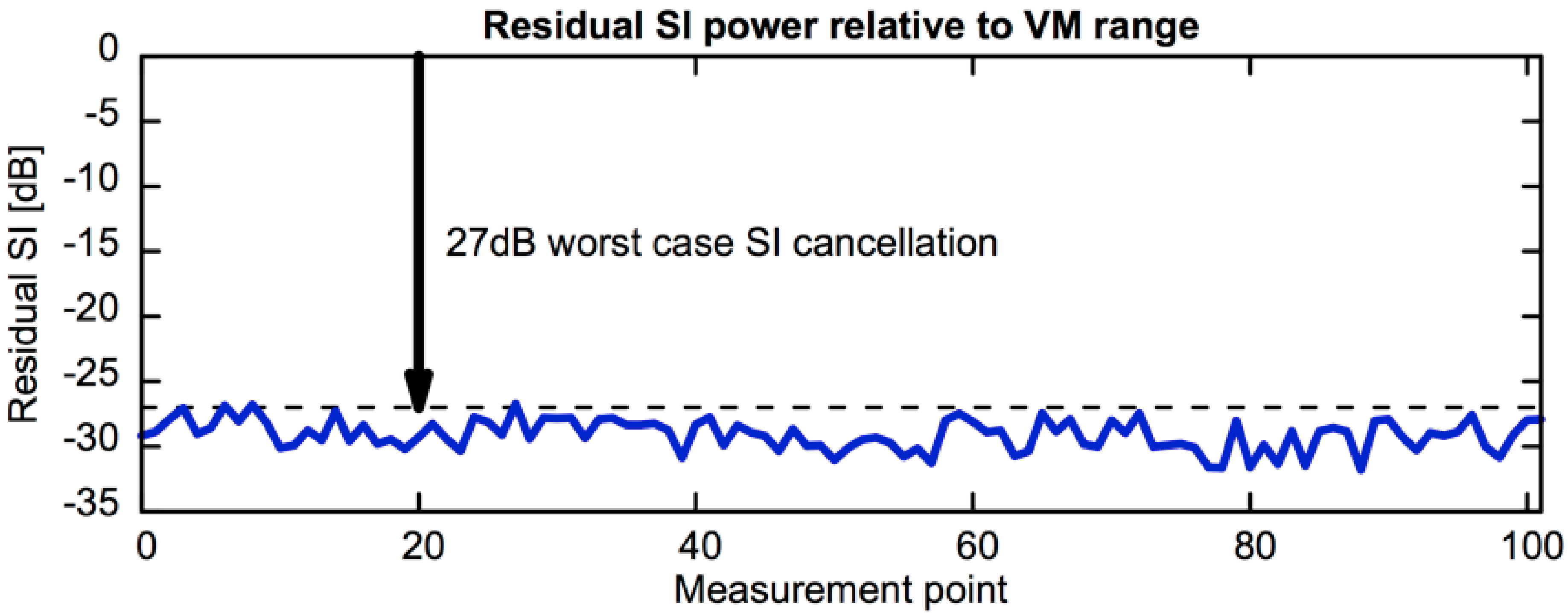
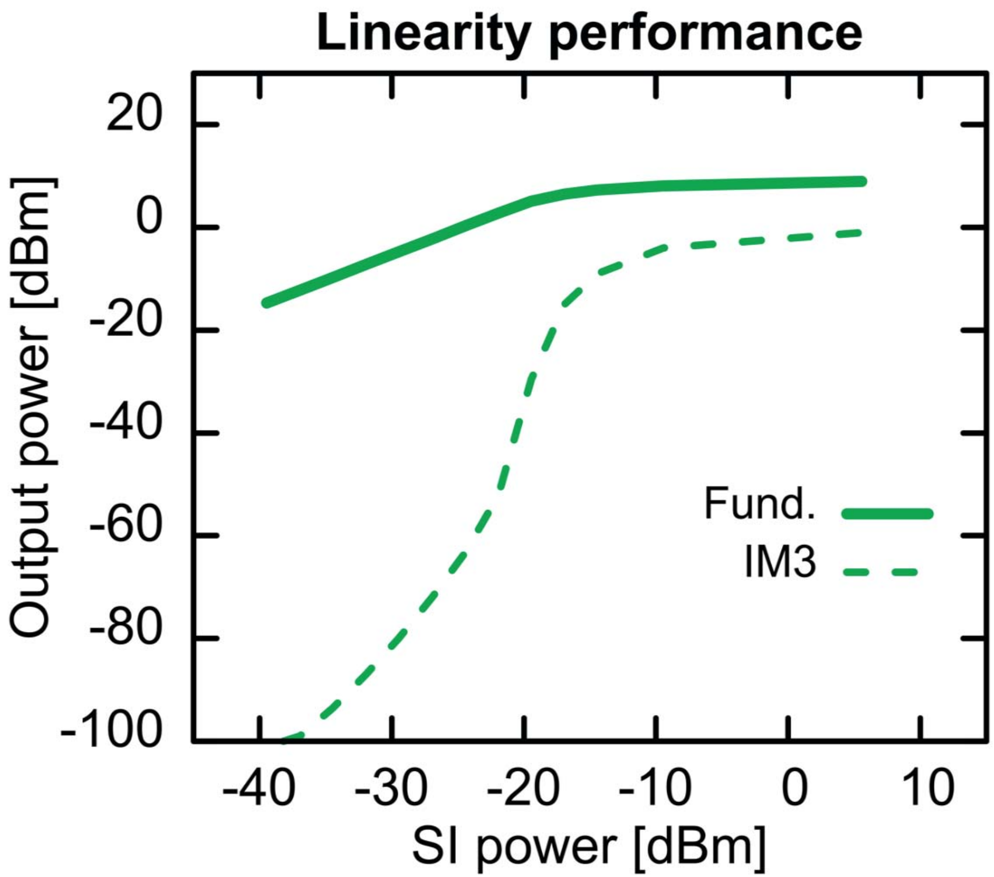


>27dB cancellation for all points

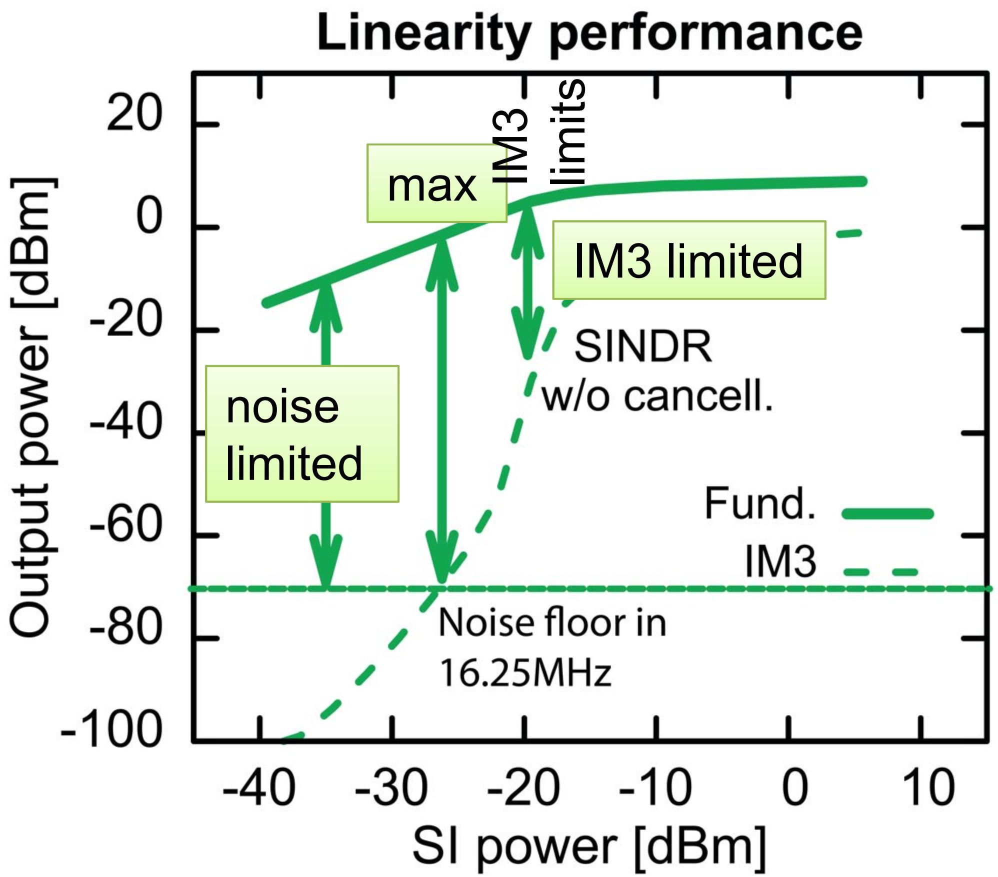
Measured IM3 without SIC

- 2-tone self-interferer
- 2.5 GHz



Resulting SINDR without SIC

- 2-tone self-interferer
- 2.5 GHz



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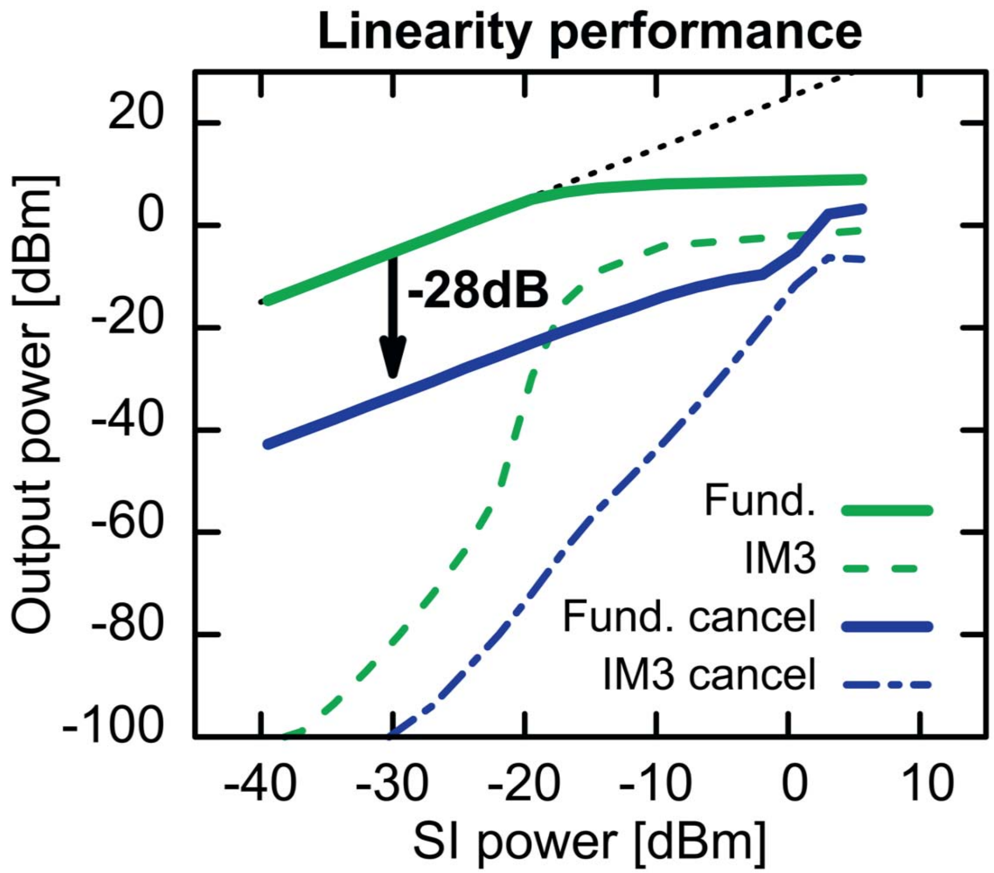

Resulting SINDR with SIC

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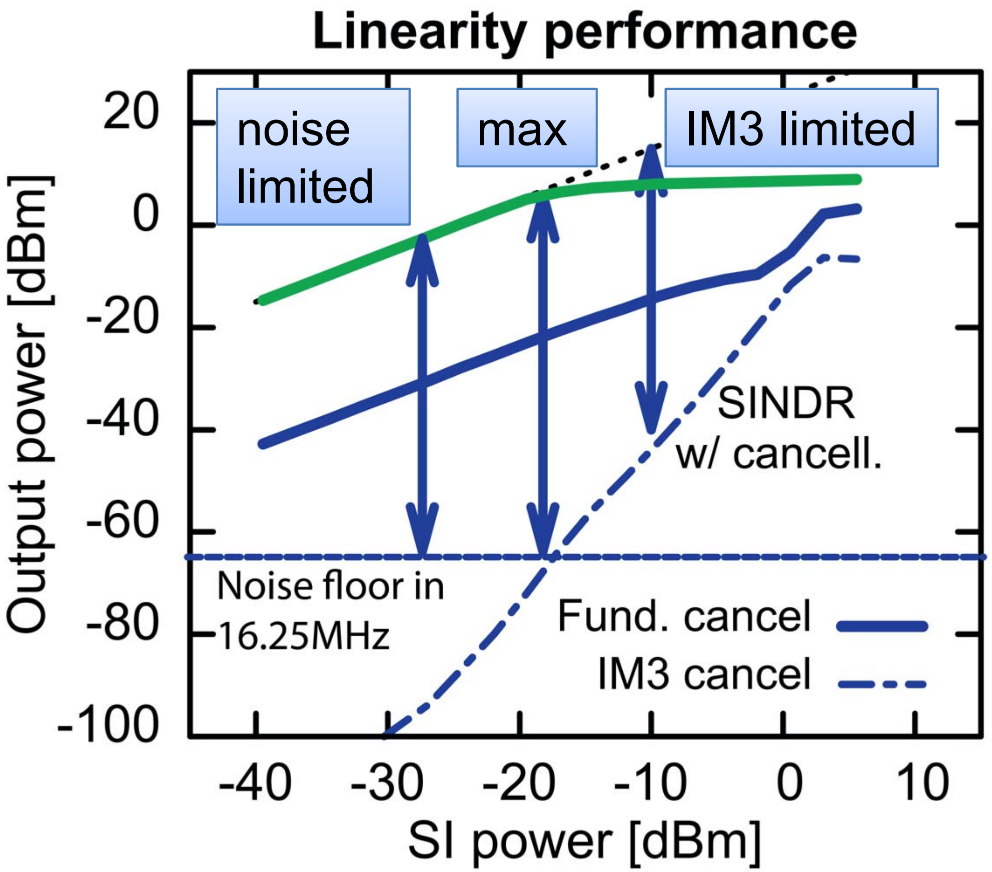
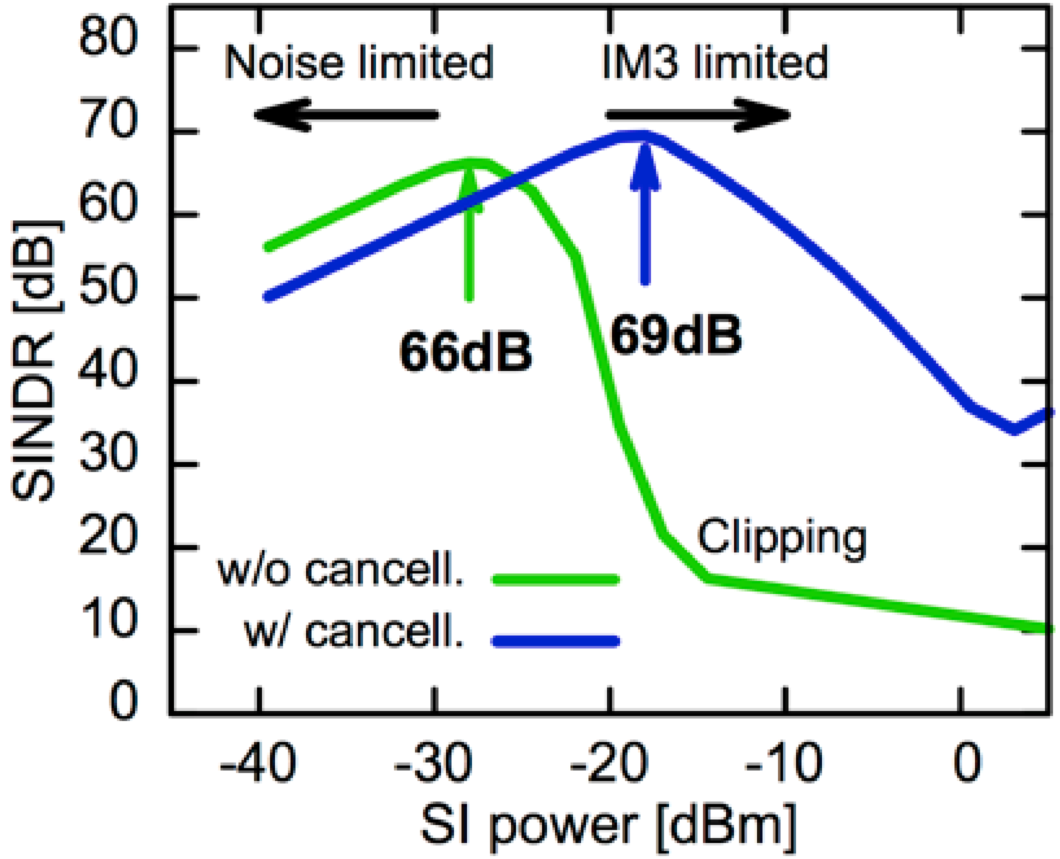


SINDR Comparison

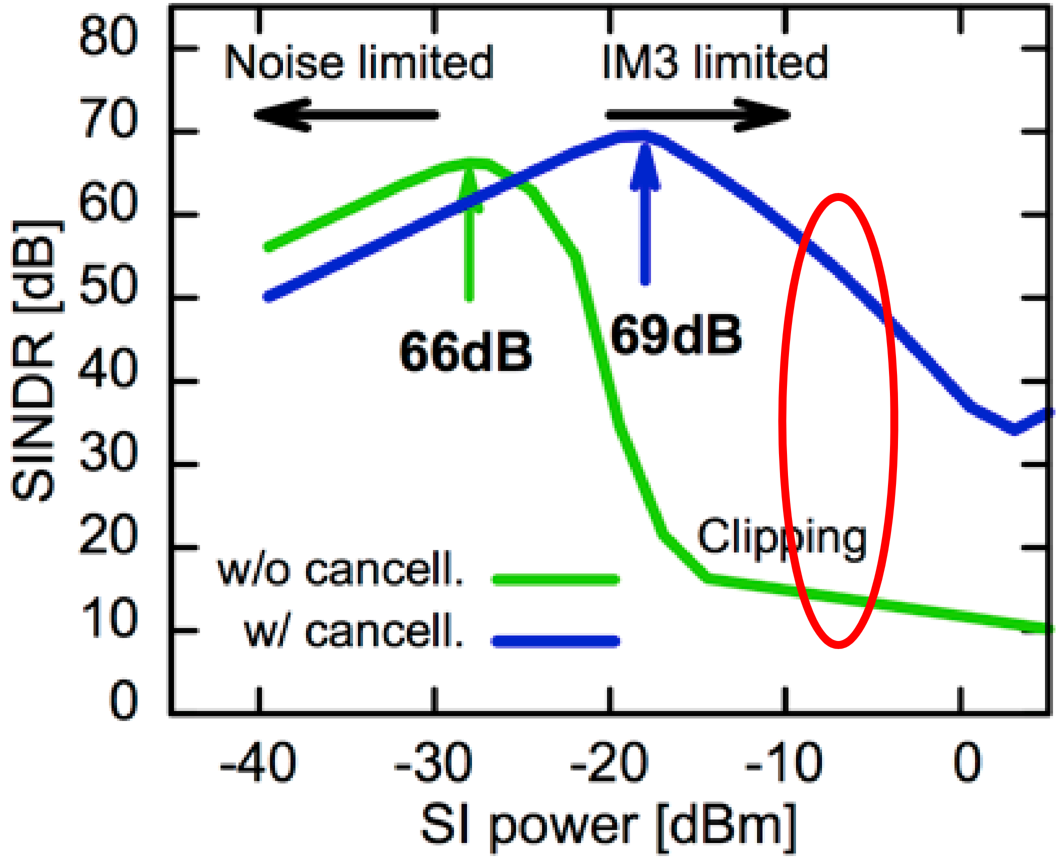
- In 16.25 MHz BW



3dB higher SINDR @ 10dB higher SI

Derived SINDR

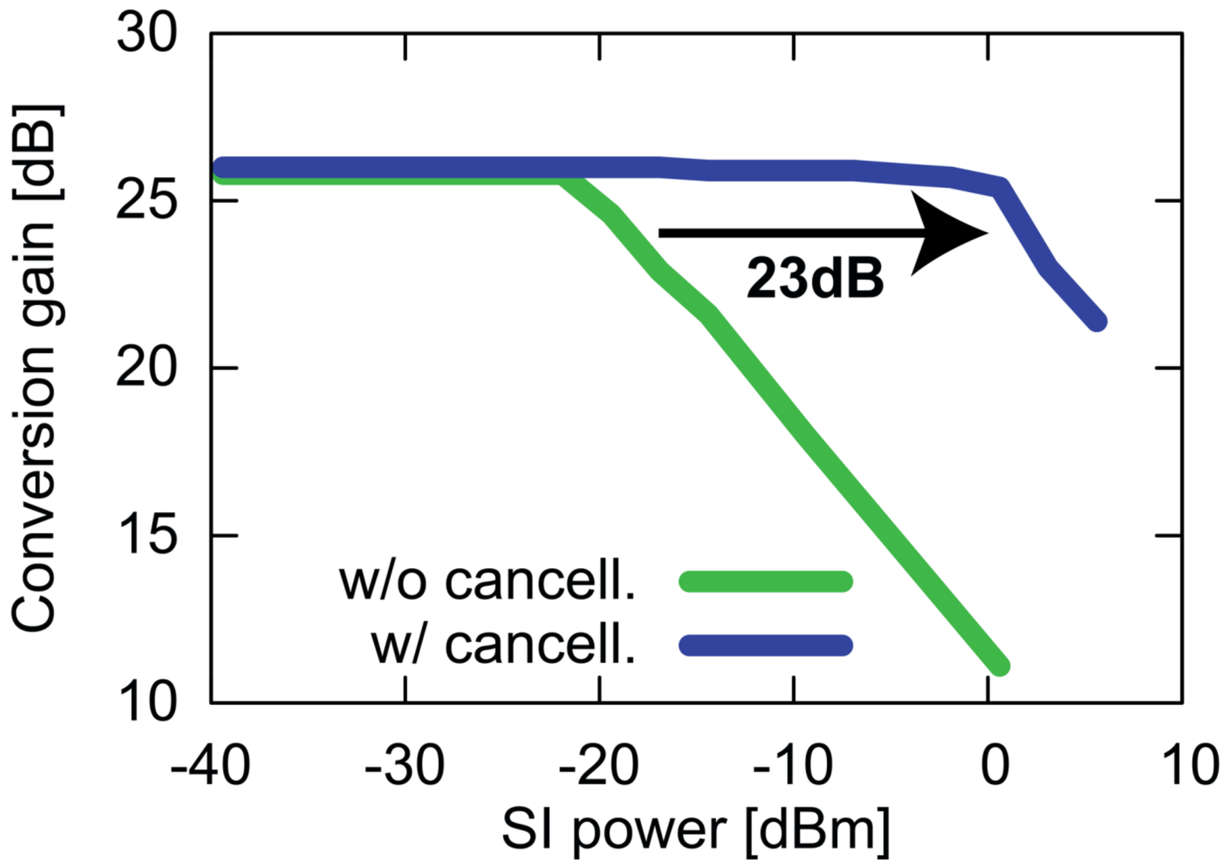
- In 16.25 MHz BW



Stronger SI: Smooth degradation of SINDR, no clipping

3dB higher SINDR @ 10dB higher SI

Conversion gain under SI



Desired signal only compressed at >0 dBm SI

Linearity & cancellation: Summary

Assuming 20 dB antenna-isolation

	w/o cancell.	w/ cancell.
Maximum link budget (SINDR + isolation)	66+20 = **86dB**	69+20 = **89dB**

Linearity & cancellation: Summary

Assuming 20 dB antenna-isolation

	w/o cancell.	w/ cancell.
Maximum link budget (SINDR + isolation)	**86 dB** **20dB isol.**	**89 dB** **20dB isol. + 27dB canc.**
Digital cancellation requirement (SINDR – cancellation)	**66 dB**	69–27 = **42 dB**

ADC and TX EVM requirements:
reduced to feasible levels

Linearity & cancellation: Summary

Assuming 20 dB antenna-isolation

	w/o cancell.	w/ cancell.
Maximum link budget (SINDR + isolation)	**86 dB**	**89 dB**
Digital cancellation requirement (SINDR – cancellation)	**66 dB**	**42 dB**
TX power @ max. link budget (SI + isolation)	-28+20 = **-8 dBm**	-18+20 = **2 dBm**

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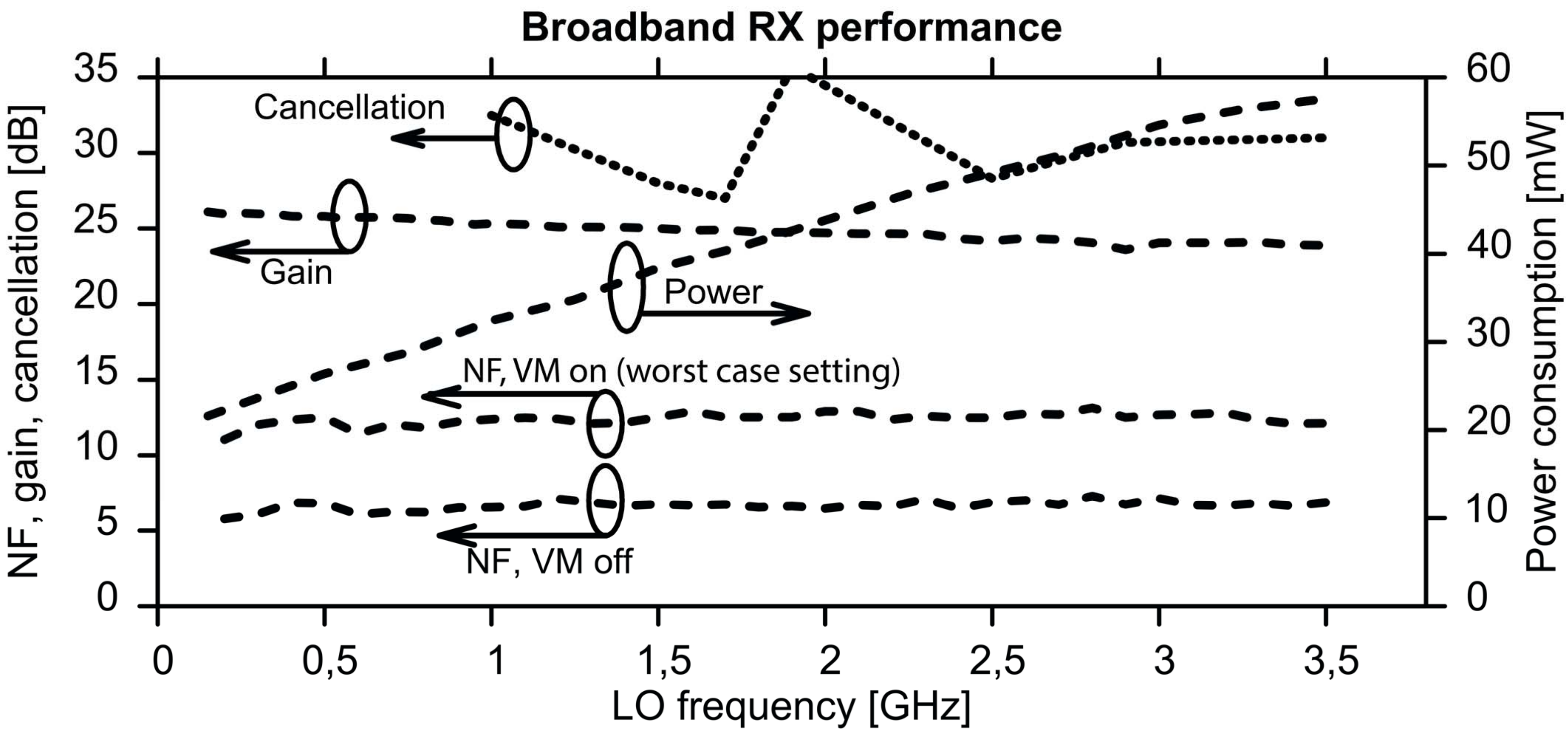
Short-range full-duplex achievable

Broadband RX performance



Frequency-flexible operation & cancellation

Performance summary

	Molnar, RFIC2014	This work
Topology	Duplexer LNA's	SI-cancelling VM
Technology	65nm CMOS 1.2/2.5V	65nm CMOS 1.2V
Operating freq.	0.1 - 1.5 GHz	0.15 - 3.5 GHz
Power cons.	43-56mW	23-56mW
Noise figure	5-8dB	10.3-12.3dB (HD: 6.3)
Baseband BW	-	24 MHz (2x12)
TX/RX isolation	33dB	27dB
SINDR in 16.25MHz	57 dB peak @ -38 dBm SI*	69.5 dB peak @ -18 dBm SI
Effective in-band IIP3	-7.2 dBm*	+19 dBm

No antenna isolation assumed for fair comparison
* Derived from reported IIP3's and NF

Conclusions

- Cancel strong interference by Passive switch-R-C
- Notch N-path filter: rejection at clock frequency
- SI-cancelling receiver in 65nm CMOS:
  - Phase / amplitude / downmixing: Vector Modulator
  - Frequency-flexible operation & cancellation
  - Mixer-first → Divert SI by passive networks → Good in-band linearity → high SINDR
  - Relaxed ADC and TX EVM requirements
- Total ~89 dB link budget potential in 16.25 MHz
  - <u>Enables low-power, short-range full-duplex wireless</u>