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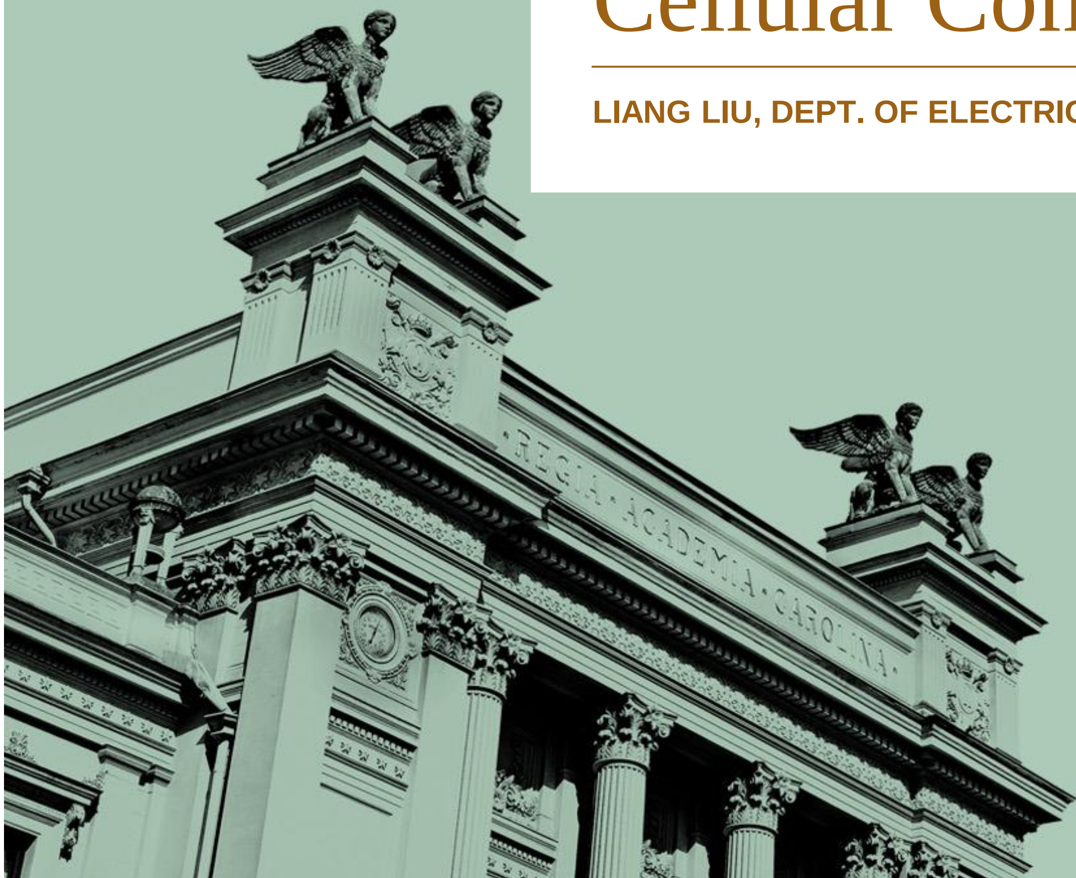
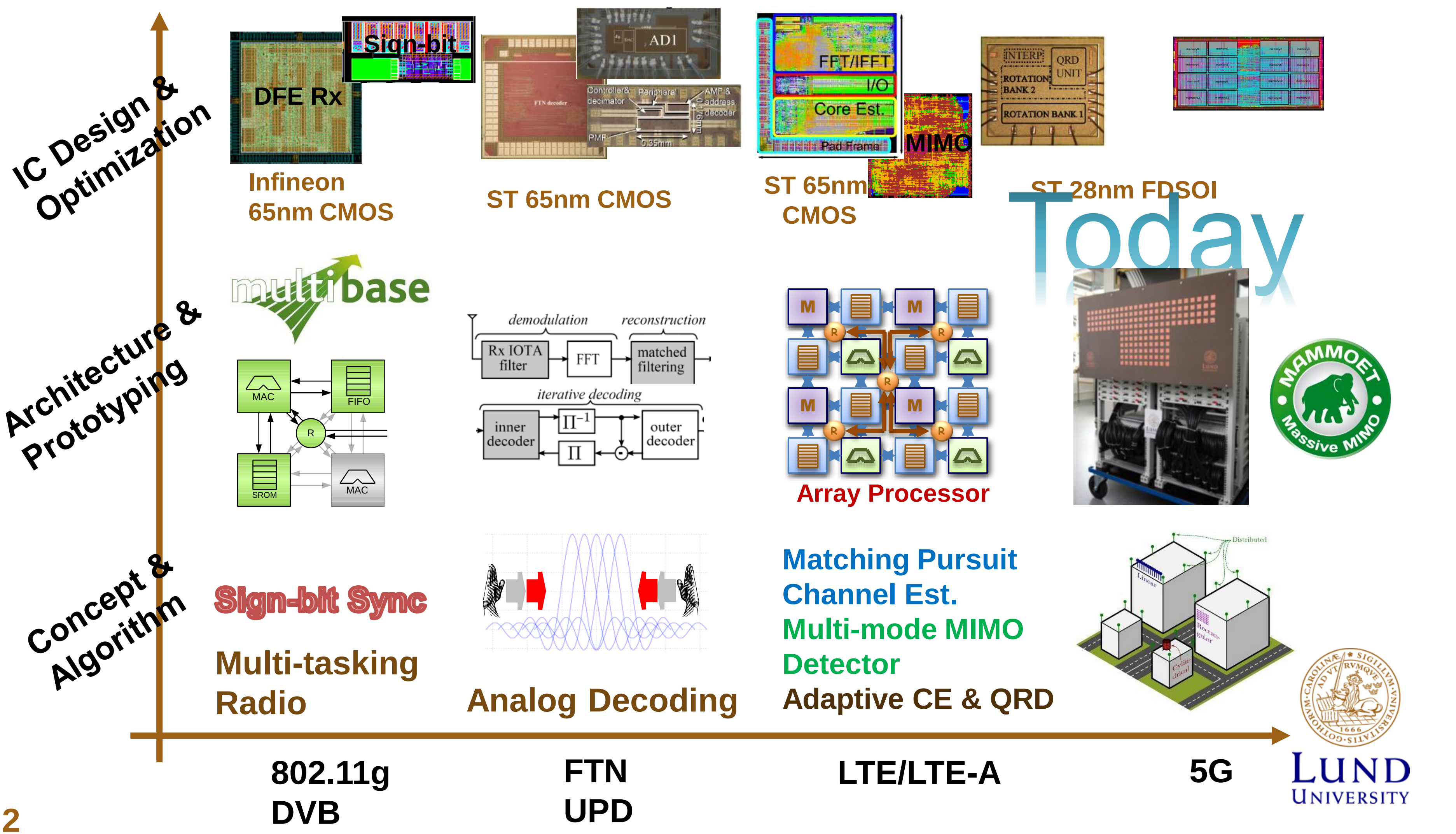
Baseband Processing for Cellular Communication

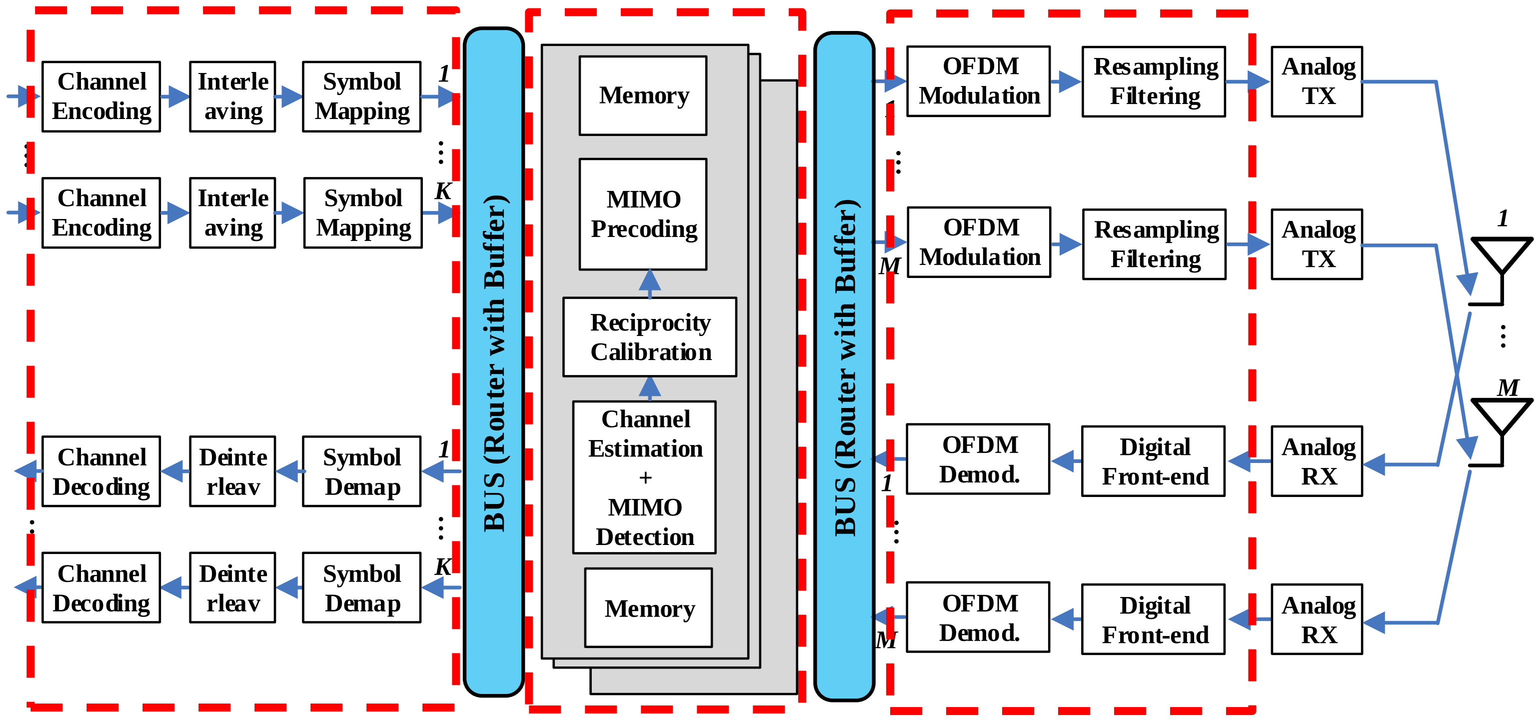
LIANG LIU, DEPT. OF ELECTRICAL AND INFORMATION TECHNOLOGY



Our Research (2009-2016)



Massive MIMO (OFDM-based TDD) baseband processing

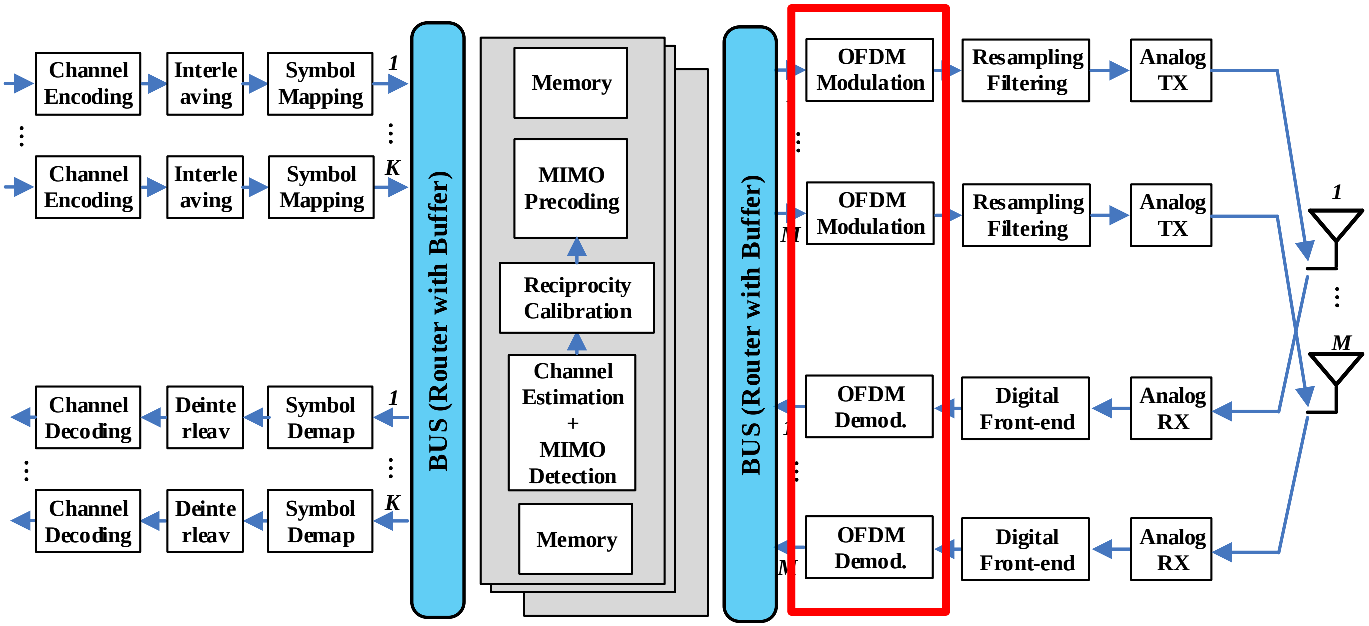


Design challenges

128 × 16 massive MIMO system with 20MHz

- High computation count:
  - 190×10^9 multiplication/s for ZF-based MIMO processing
- Low processing latency:
  - 285μs RX-TX turnaround time for moderate mobility
- Large data storage:
  - 9.8MB memory for channel matrix
- Complicated data shuffling:
  - 11GB/s information exchange for 16-bit wordlength

OFDM processing



➢ Low-latency and area-efficient FFT/IFFT processor for Massive MIMO

Mojtaba Mahdavi

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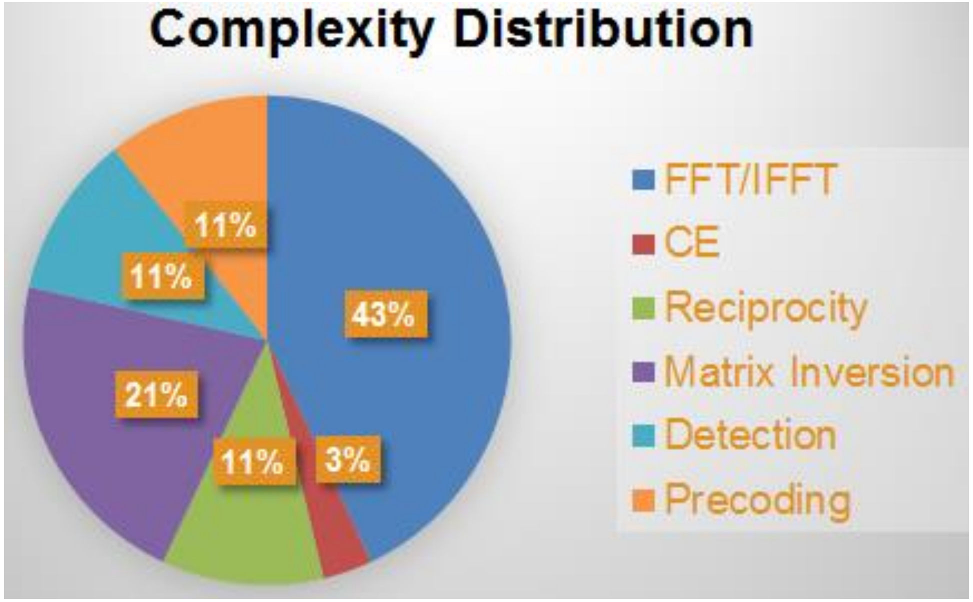
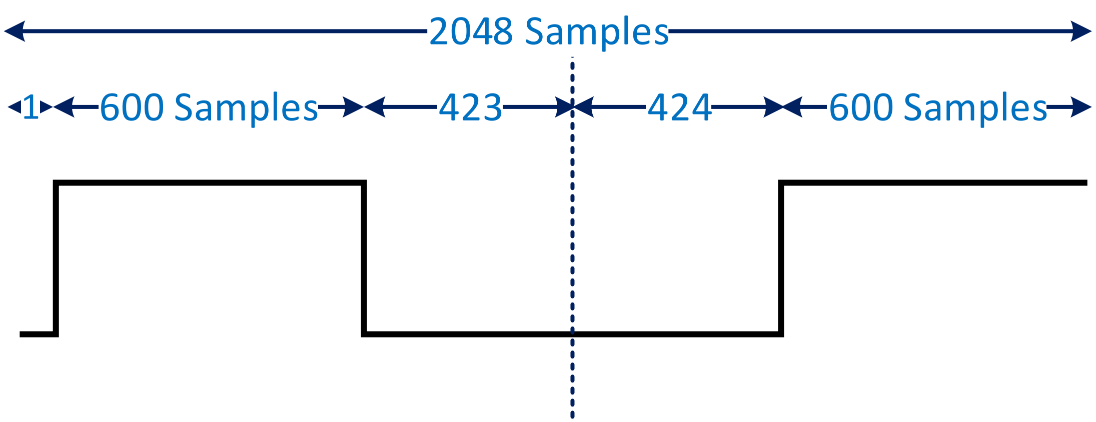
OFDM processing in Massive MIMO

- Design Challenges
  - High complexity ~ *M*
  - Low latency ~ Rx-Tx path

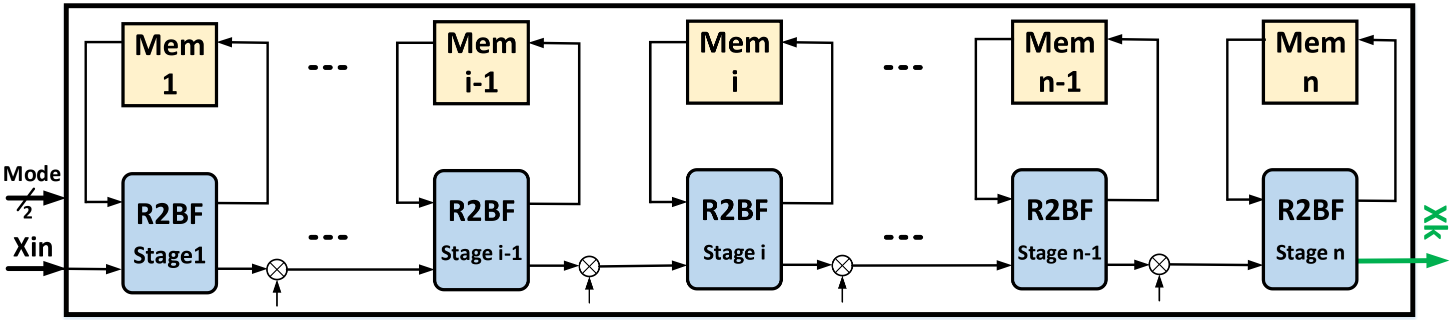


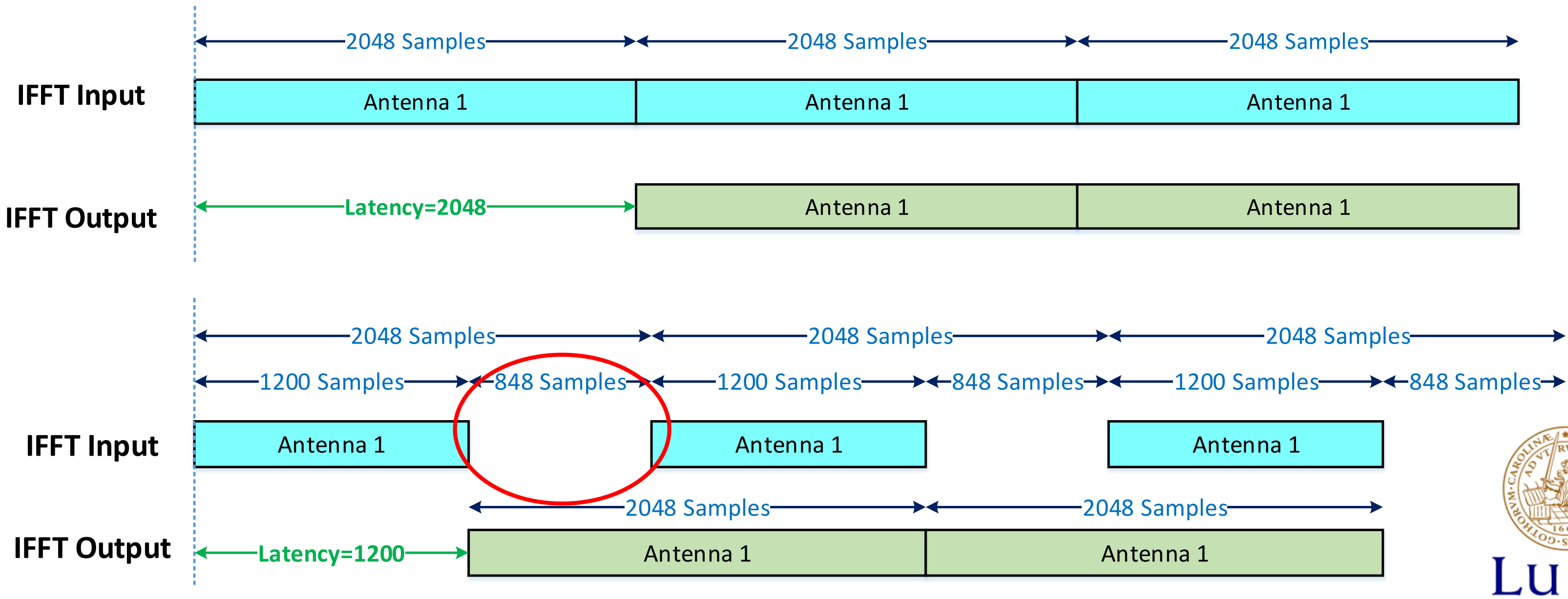
OFDM processing in Massive MIMO

- Design Challenges
  - High complexity ~ *M*
  - Low latency ~ Rx-Tx path
- Design Strategy: Utilize the guard-band (zeros) in OFDM
  - Reduce latency
  - Enable Extensive hardware sharing: OFDM (de)modulation/Multiple antennas



IFFT/FFT architecture (pipeline)





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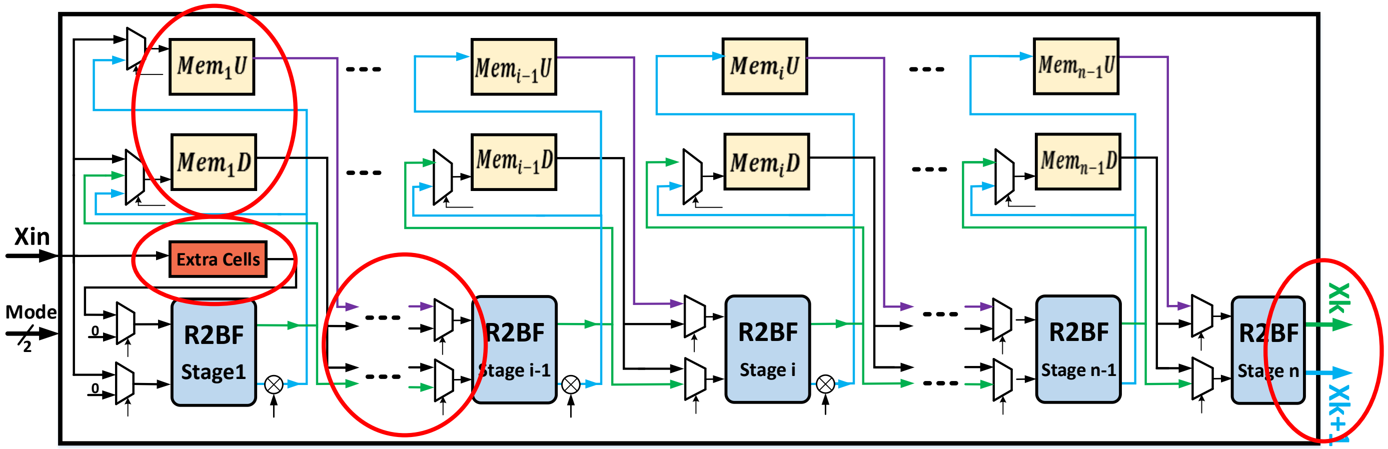
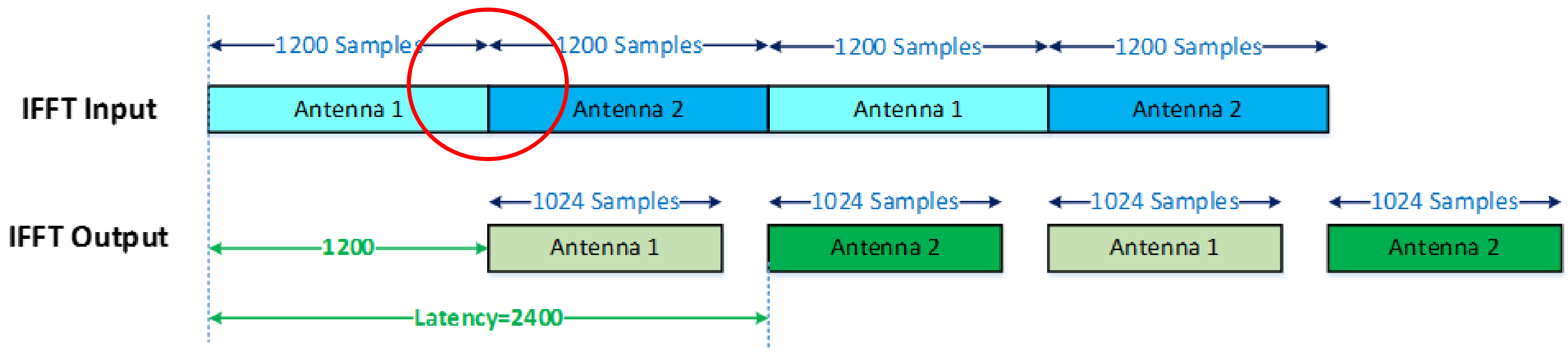
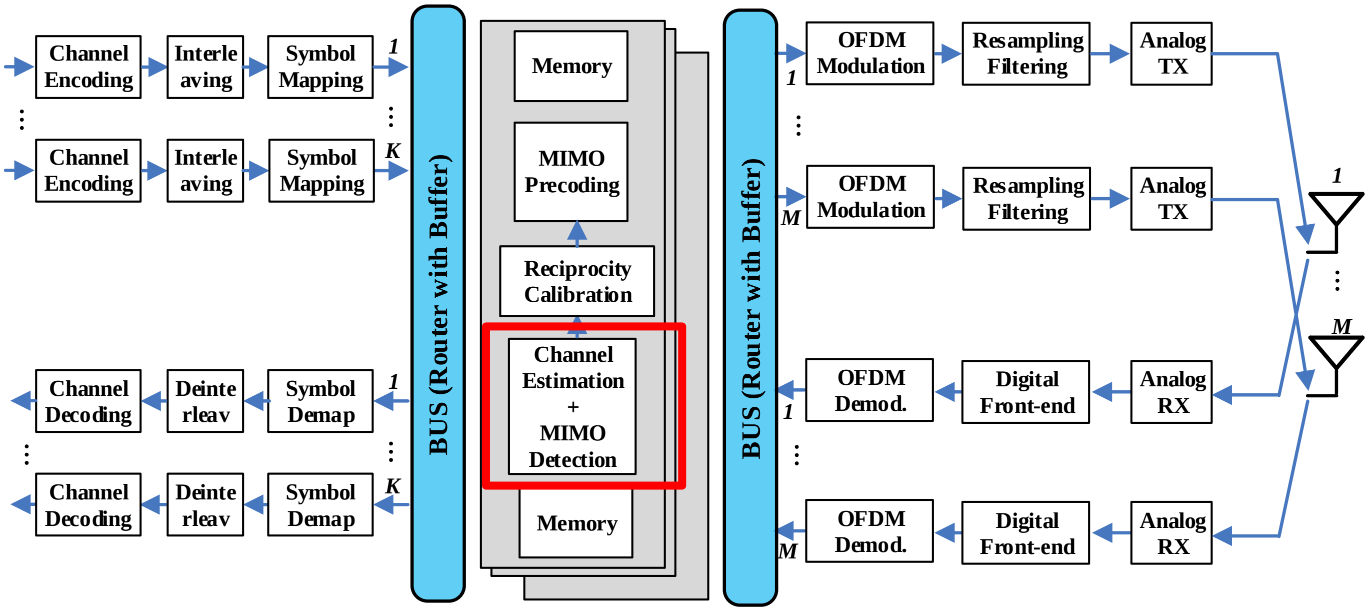
IFFT/FFT architecture (modified)





Multi-user MIMO detection

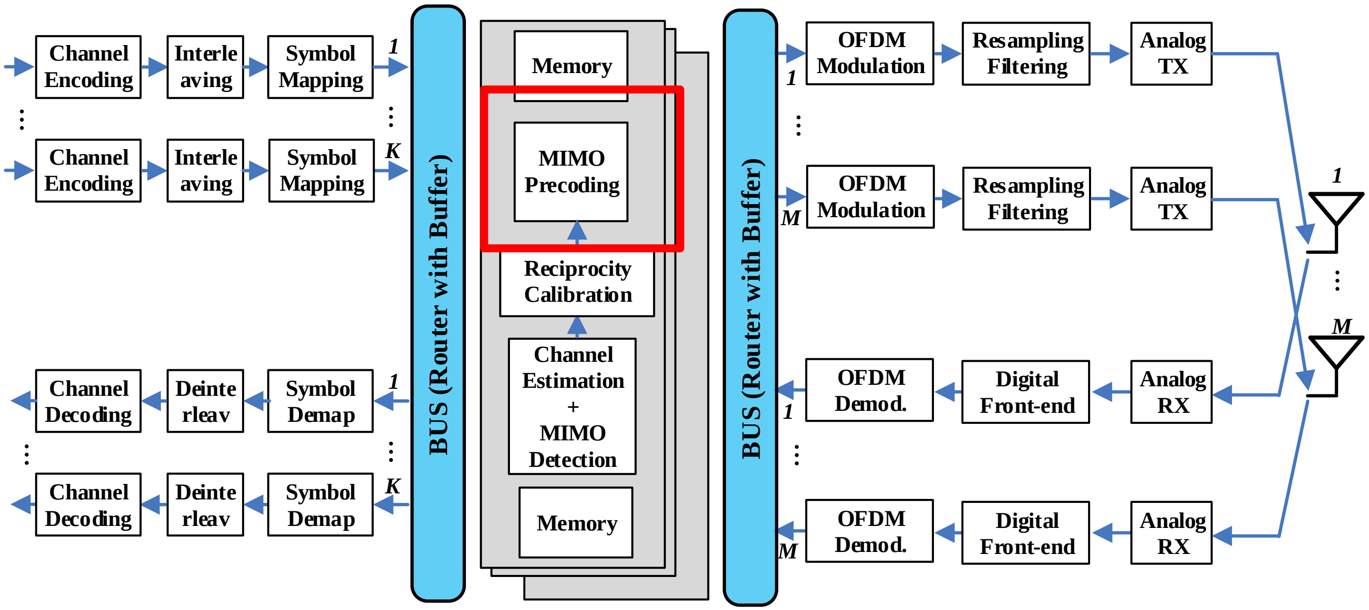


➢ Massive MIMO detector with flexible performance-complexity tradeoff

Hemanth Prabhu

Wei Tang (University of Michigan)

Downlink precoding



➢ Low PAPR massive MIMO precoding using antenna reservation and modified QRD

Hemanth Prabhu

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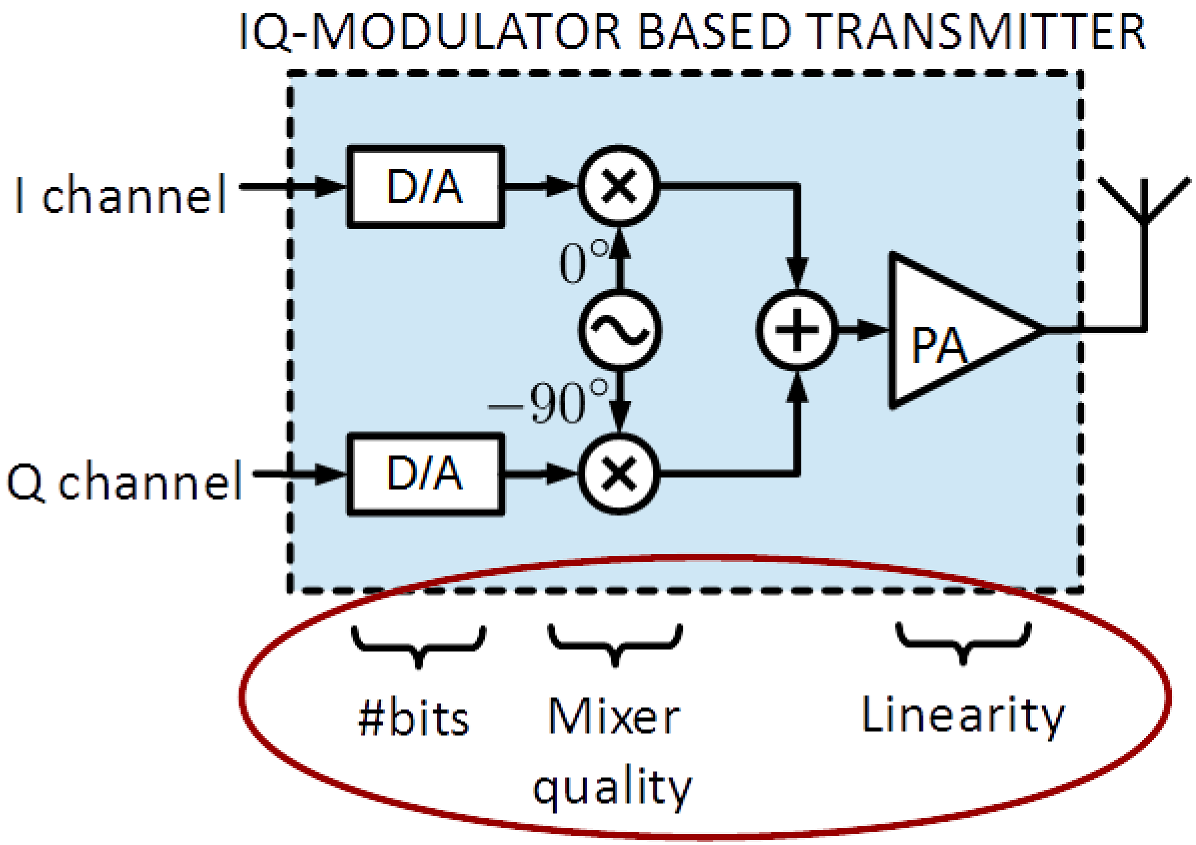
Enable low-cost analog components



Keep these as inexpensive as possible

How can we reduce the requirement on amplifier dynamic range?

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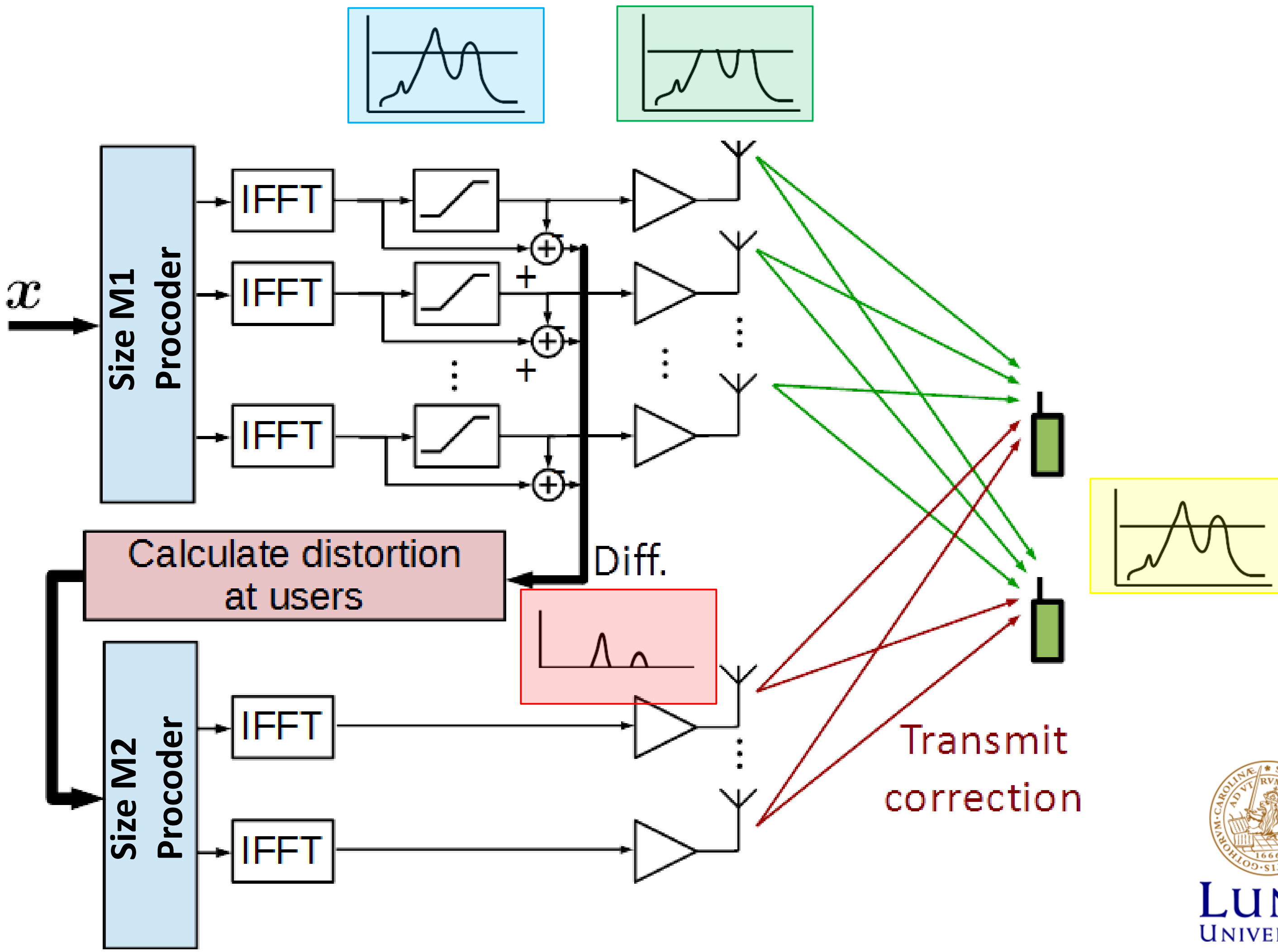
Reducing PA dynamic range with antenna reservation (concept)



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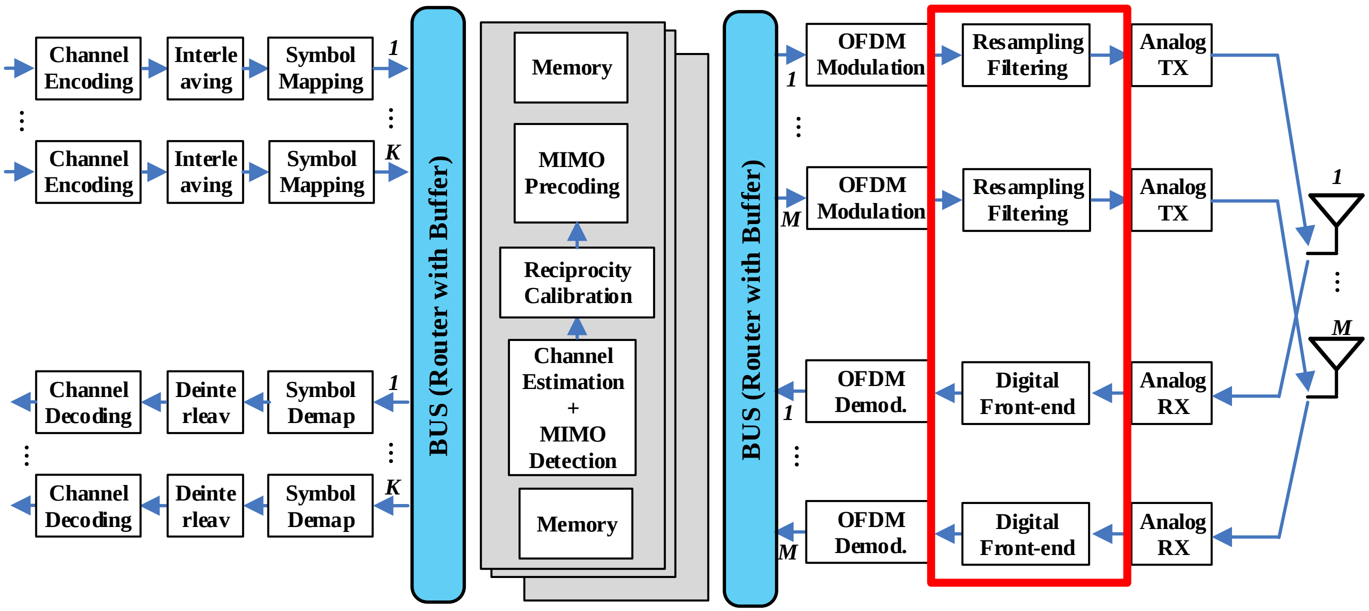
Digital front-end



➢ Pre-compensating I/Q imbalance for massive MIMO

Hemanth Prabhu

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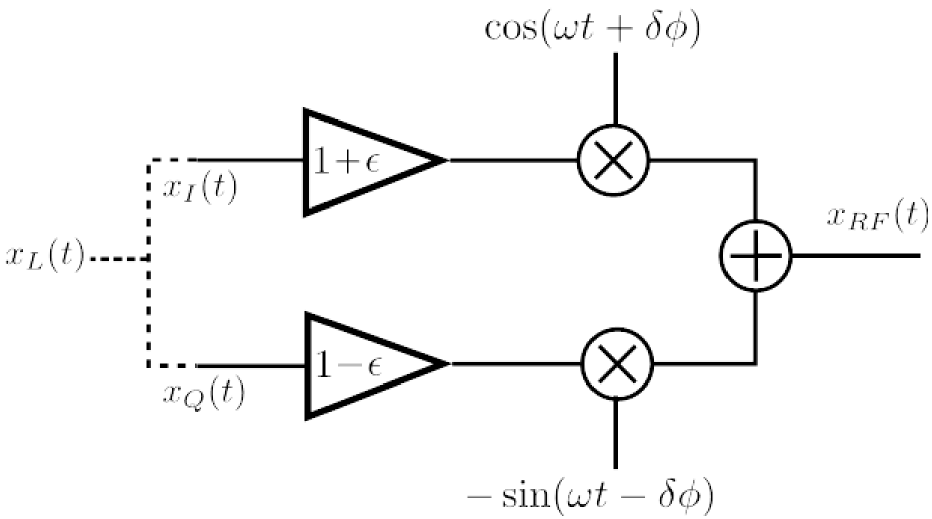
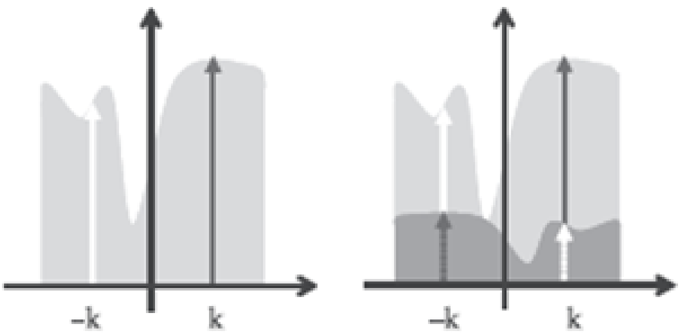
Model of IQ imbalance



Assuming perfect receiver (Rx) chain

$$X_{Rx}(f) = aX_L(f) + bX_L^*(-f)$$



1. How dose IQ imbalance affect massive MIMO system?
2. Can we mitigate IQ imbalance in an efficient way?

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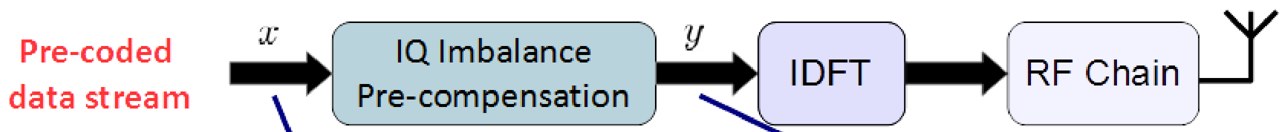
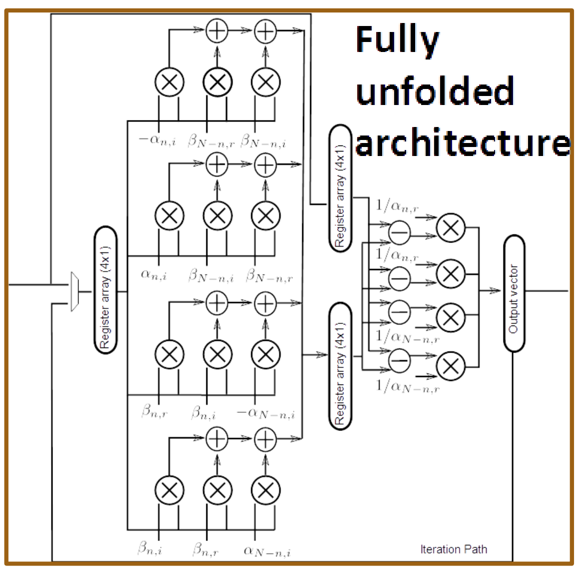
Compensating IQ-imbalance



$$\begin{bmatrix} x_r^n \\ x_i^n \\ x_r^{N-n} \\ x_i^{N-n} \end{bmatrix} = \begin{bmatrix} a_r^n & -a_i & b_r^{N-n} & b_i^{N-n} \\ a_i^n & a_r & b_i^{N-n} & -b_r^{N-n} \\ b_r^n & b_i & a_r^{N-n} & -a_i^{N-n} \\ b_i^n & -b_r & a_i^{N-n} & a_r^{N-n} \end{bmatrix} \begin{bmatrix} y_r^n \\ y_i^n \\ y_r^{N-n} \\ y_i^{N-n} \end{bmatrix}$$

Large diagonal elements. Can be efficiently implemented as a **Jacobi iterative solver**

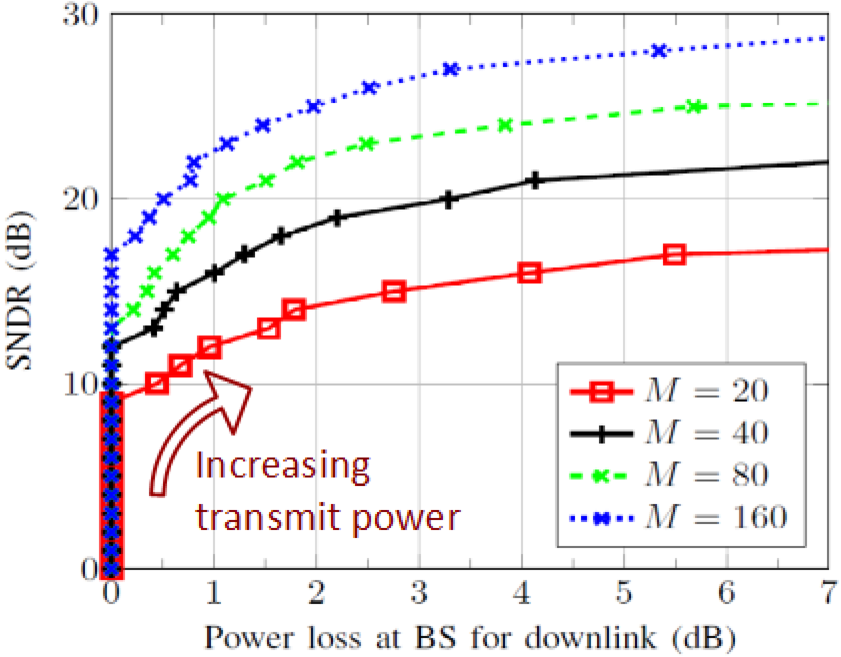


Item	Value
Process	ST 28nm
Power	0.61mW
Latency	2clk @ 200MHz
Gate count	24k

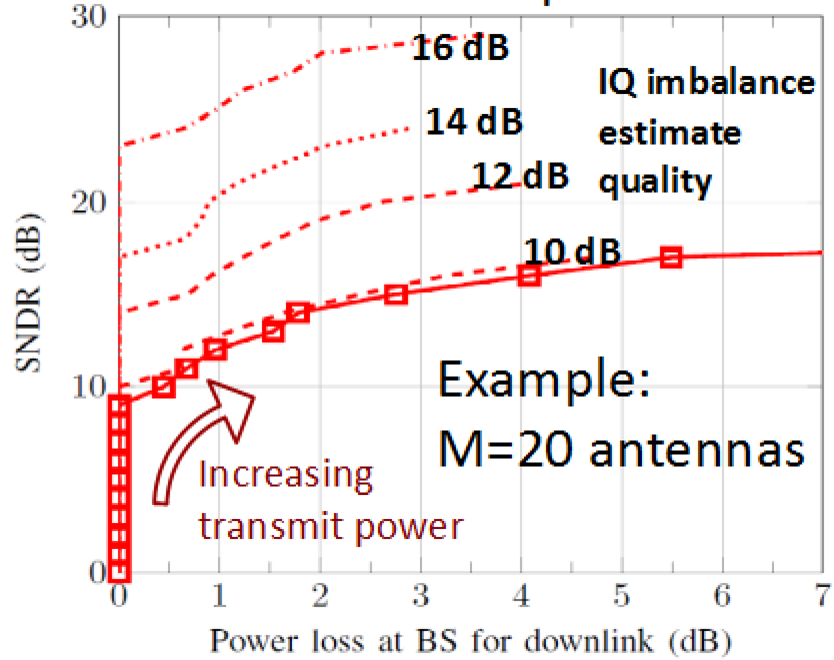
One instance per antenna

Compensating IQ-imbalance

SNDR without compensation



SNDR with compensation



Simulated IQ imbalance with mean value
6% amplitude and 6 degree phase imbalance
(random on antennas)

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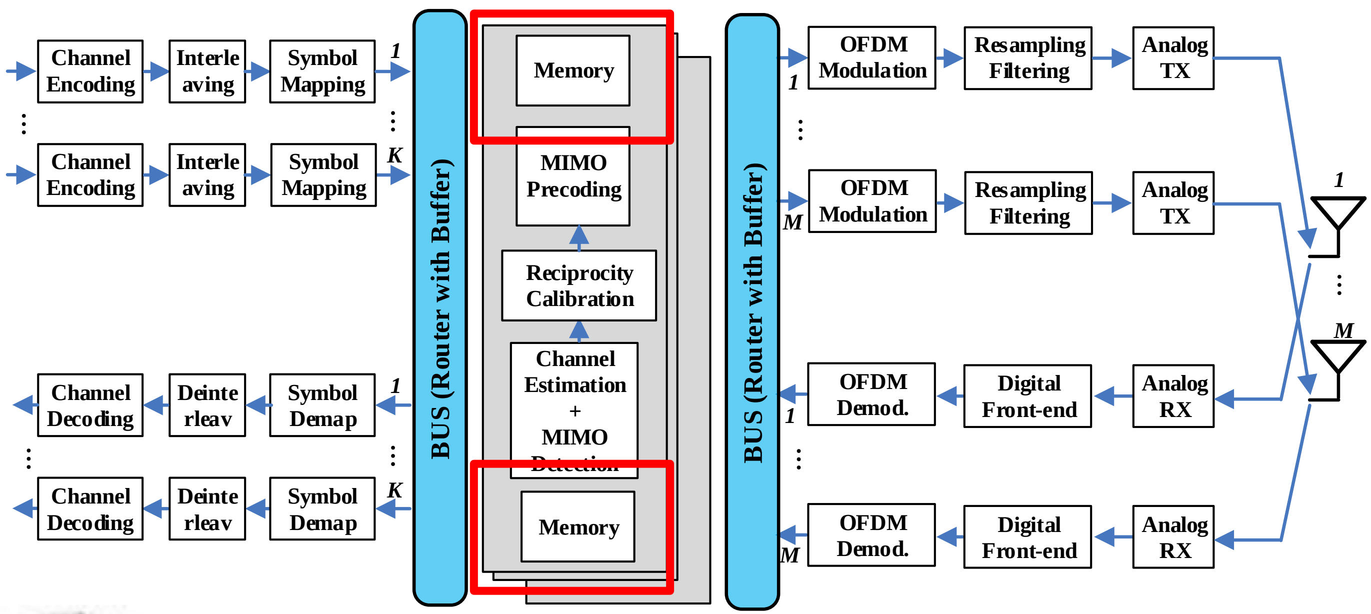
Memory subsystem



➢ Parallel memory for massive MIMO with data compression technique

Yangxurui Liu

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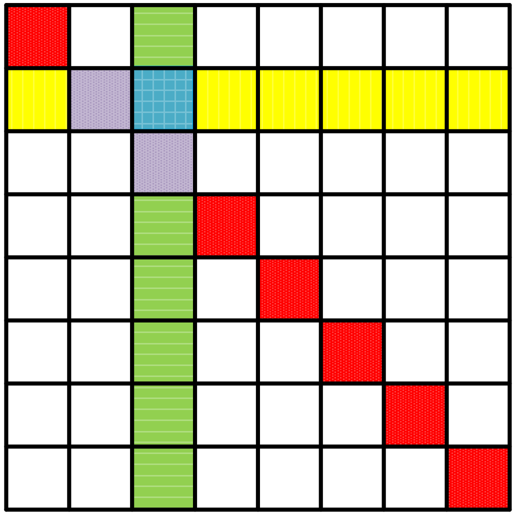
Memory subsystem in Massive MIMO

- High capacity and throughput
  - Channel matrix **128 × 16** in massive MIMO v.s. **4 × 4** in LTE-A
- Multiple access patterns
  - Column wise : $\boldsymbol{H}^{\mathrm{H}}\boldsymbol{H}$
  - Row wise: $\boldsymbol{Hy}$
  - Diagonal wise: $\boldsymbol{H}^{\mathrm{H}}\boldsymbol{H}+\alpha\boldsymbol{I}$
- Adjustable operand matrix size



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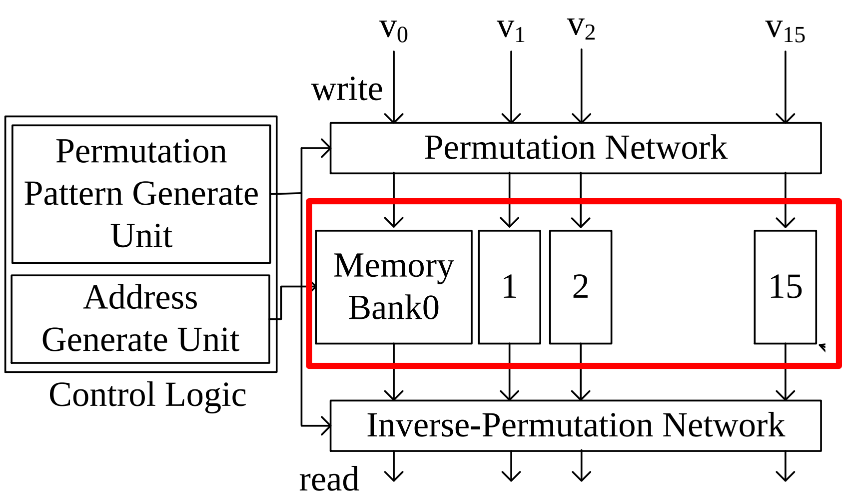
Conflict-free parallel memory scheme



column

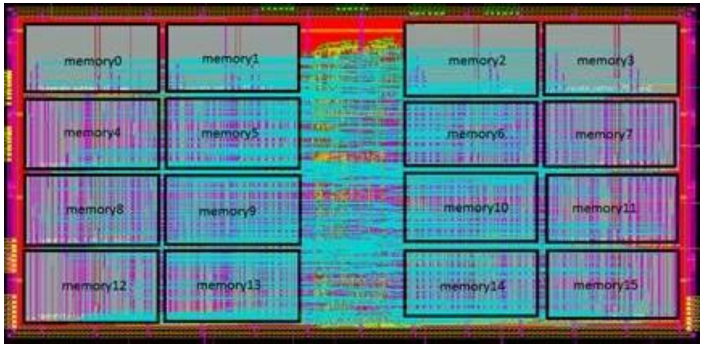
row

16	1	2	3	4	5	6	7	8	9
14	15	16	1	2	3	4	5	6	7
12	13	14	15	16	1	2	3	4	5
10	11	12	13	14	15	16	1	2	3
8	9	10	11	12	13	14	15	16	1
6	7	8	9	10	11	12	13	14	15
4	5	6	7	8	9	10	11	12	13
2	3	4	5	6	7	8	9	10	11
9	8	7	6	5	4	3	2	1	16
11	10	9	8	7	6	5	4	3	2
13	12	11	10	9	8	7	6	5	4
15	14	13	12	11	10	9	8	7	6
1	16	15	14	13	12	11	10	9	8
3	2	1	16	15	14	13	12	11	10
5	4	3	2	1	16	15	14	13	12
7	6	5	4	3	2	1	16	15	14

diagonal

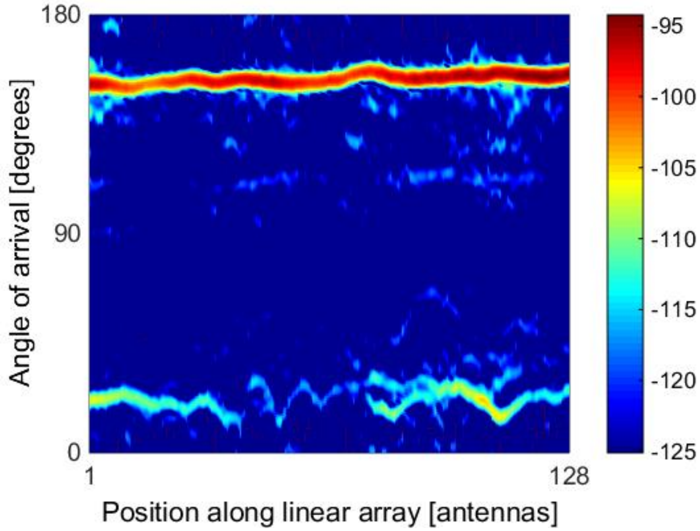
Case study: hardware implementation of a 16-bank architecture

- Capacity 128kB: 15 subcarriers of 128×16 MIMO system
- Row/Column/Diagonal (16 elements) access in one clock cycle
- 0.28 mm^2 in ST 28nm technique
- 64 GB/s Throughput@1 GHz Frequency
- Power consumption
  - 197mW @write
  - 246mW @fetch

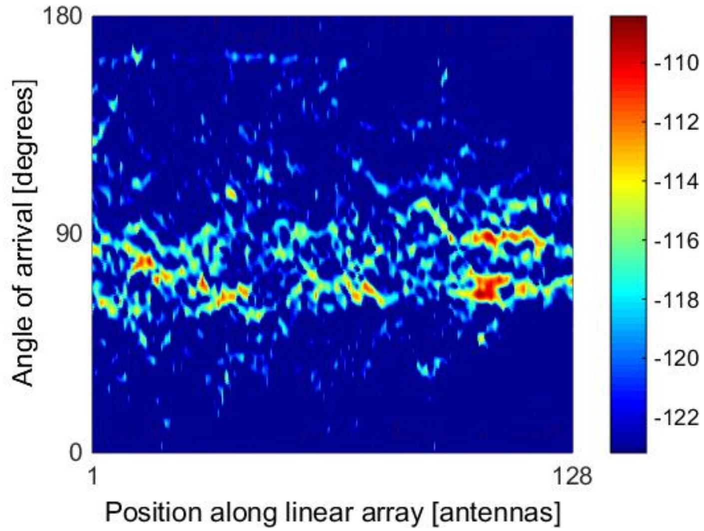


What can be done to reduce the memory area?

Exploiting the sparsity in massive MIMO channel



LOS scenario



NLOS scenario

Distribution of angle of arrival signals at base station
(Real measured result with linear array of 128 antenna elements)

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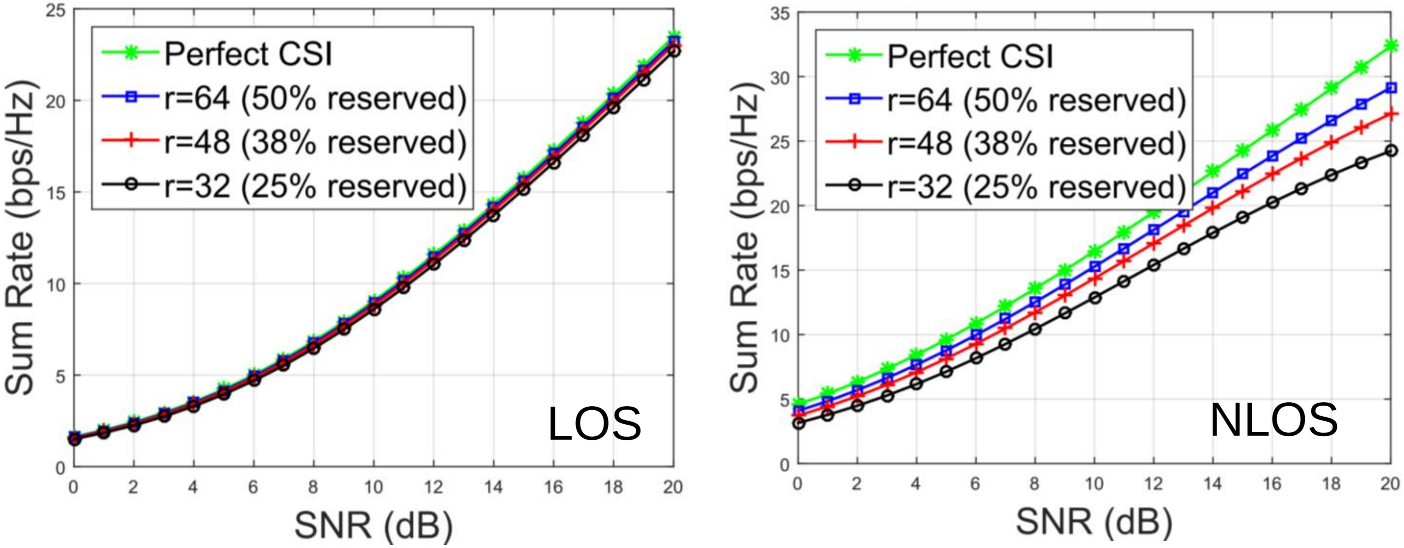
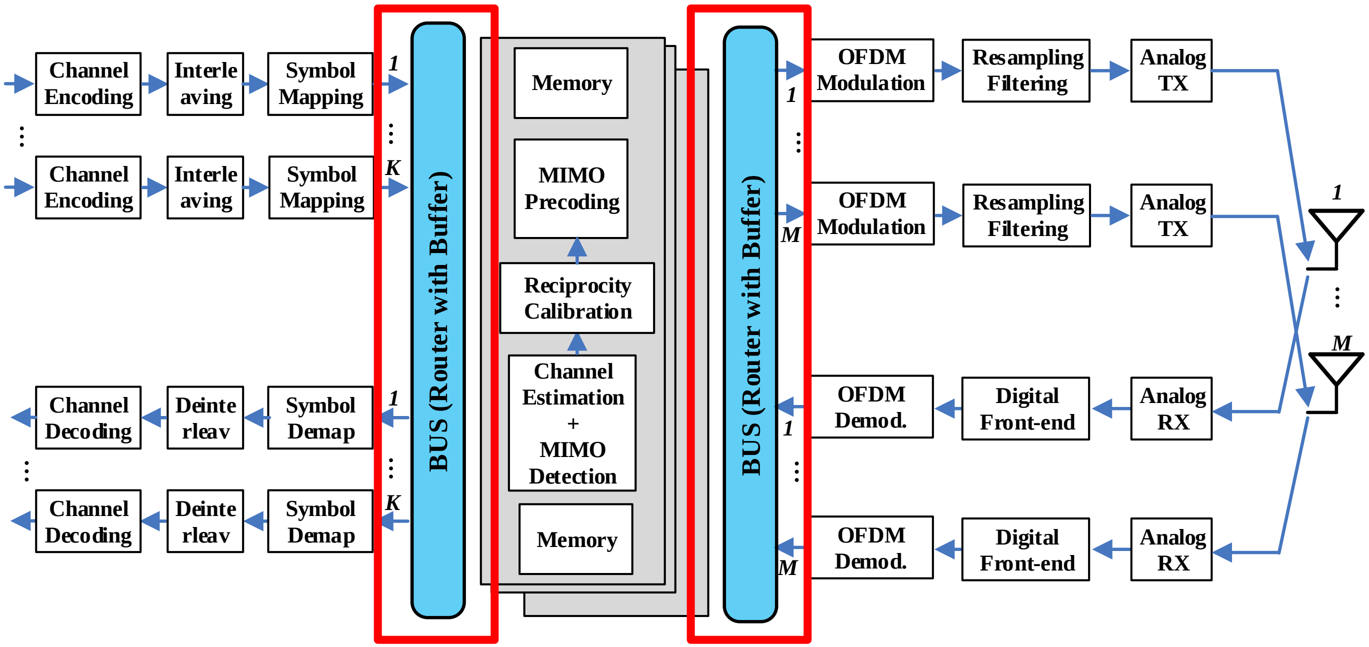
FFT-based channel data compression



Data shuffling network



Dimitar Nikolov

Steffen Malkowsky

➢ Data shuffling network with dedicated time scheduling

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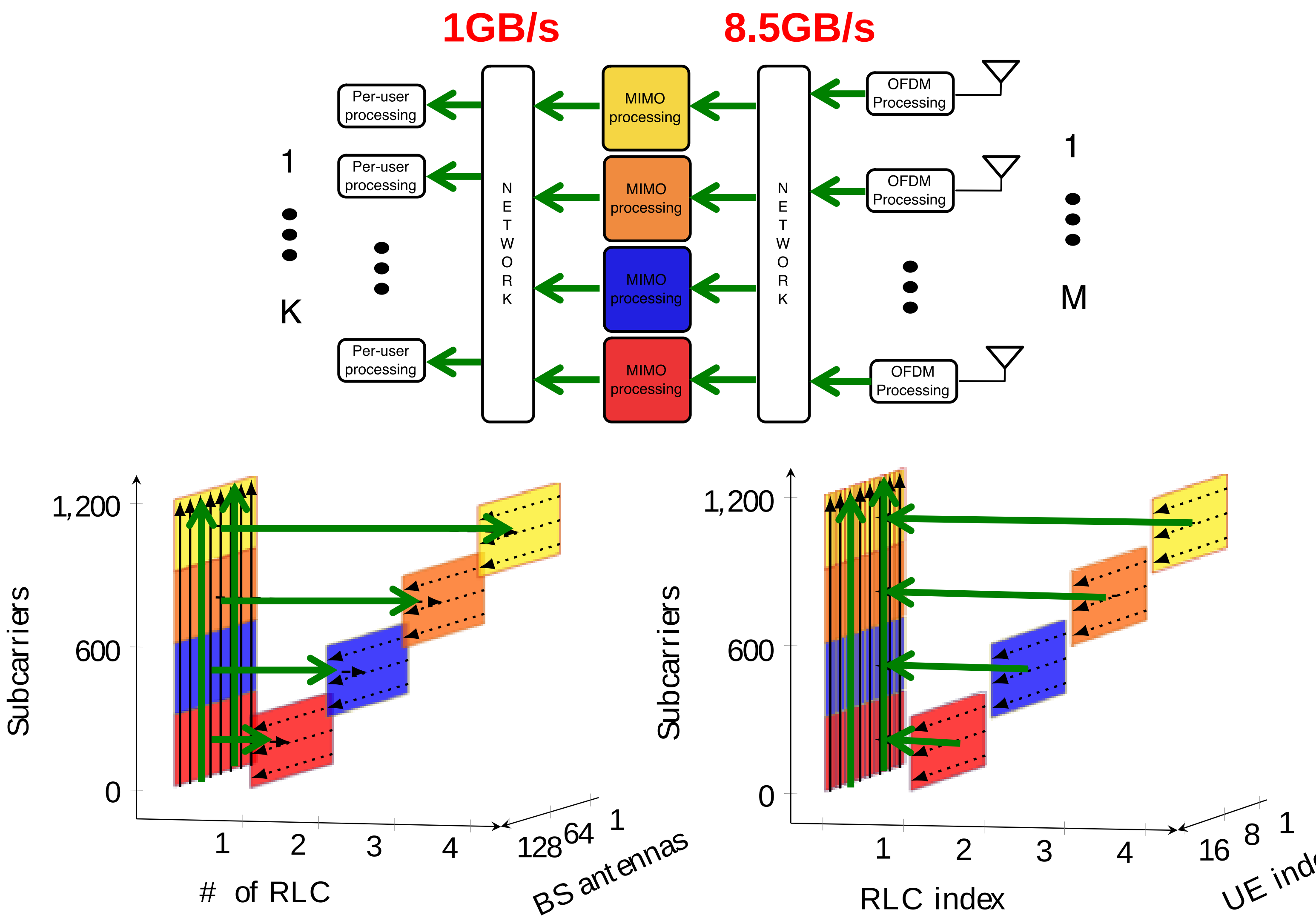
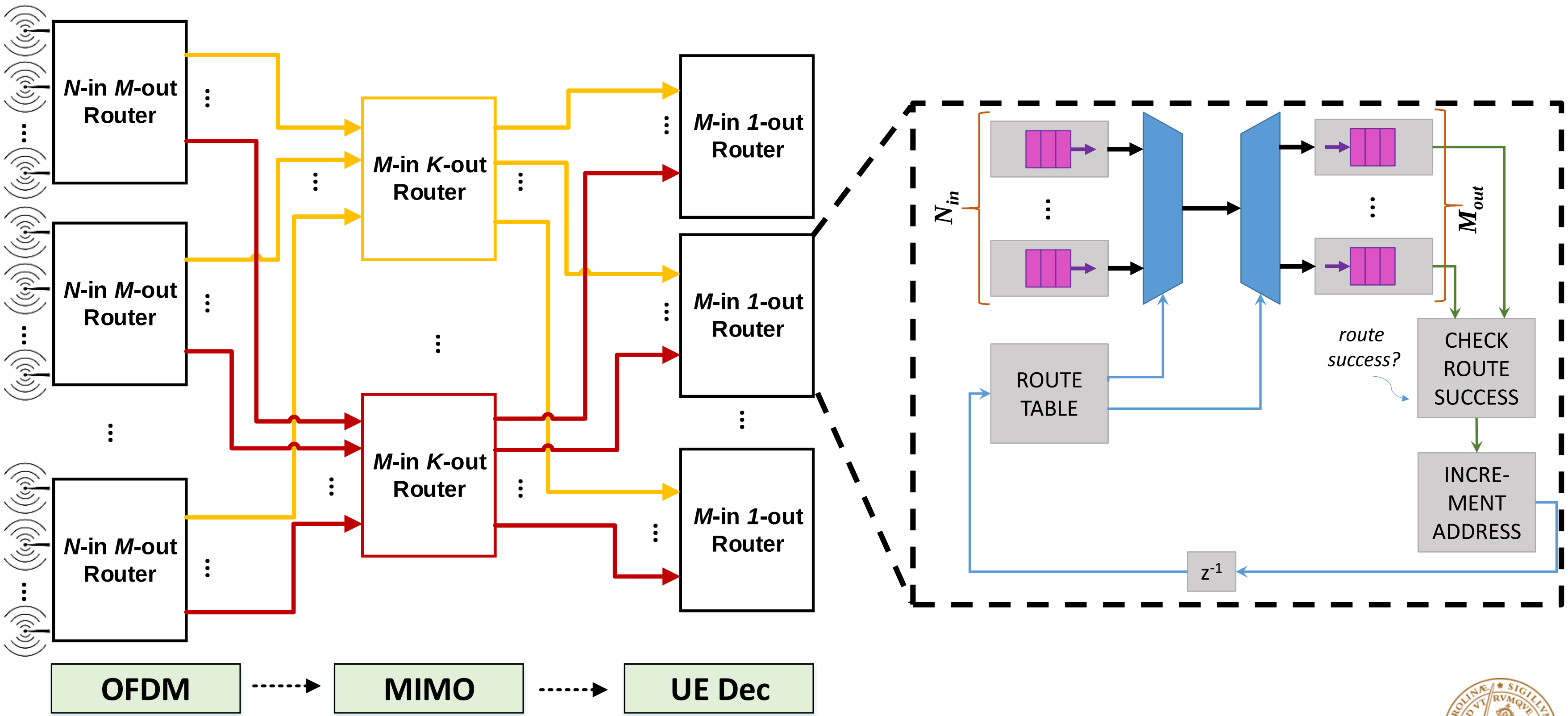
Data shuffling in Massive MIMO (uplink example)



Data shuffling network (uplink example)



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Conclusions

- Critical design challenge for massive MIMO baseband processor
- Low-latency FFT/IFFT
- Adaptive MIMO detection and low-complexity precoder
- Parallel memory with data compression
- DSP enables low-cost hardware
- Possible to have an integrated baseband processor

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Posters

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